QQ3002931911   13148878879

WK2132 multi-bus interface two-channel universal asynchronous transceiver lead-free package

1. Product overview

WK2132 is the first 2-channel UART device with low power consumption of 256-level FIFO and supports UART/SPITM/IIC interface. able to pass

Mode selection makes the chip work in any of the above main interface modes, and expands the selected main interface into two UARTs with enhanced functions.

The UART of the extended sub-channel has the following features:

- The baud rate, word length, and parity format of each sub-channel UART can be set independently, and the highest communication rate can be provided at 2Mbps.

- Each sub-channel can be independently set to work in IrDA infrared communication.

- Each sub-channel has an independent 256-level FIFO for receiving/transmitting, and the interrupt of the FIFO can be programmed according to the user's needs.

  Timeout interrupt function.

WK2132 adopts SSOP16 green lead-free package, can work in a wide working voltage range of 2.5 ~ 5.0V, with configurable

Automatic sleep/wake function.

[Note]: SPITM is a registered trademark of MOTOLORA.

2. Basic Features

2.1 General characteristics

- Support a variety of host interfaces: you can choose UART, SPI, IIC large

- hardware transceiver buffer, support 256-level FIFO low-power

- design, can configure automatic sleep, automatic wake-up mode (uS-level wake-up)

- Wide working voltage design, the working voltage is 2.5V ~ 5.0V

- Simplified configuration registers and control words, simple and reliable operation

- Provide industrial grade products

- High-speed CMOS process, sub-serial port rate up to 2Mbps@5V, 1.5Mbps@3.3V, 1Mbps@2.5V Adopt SSOP16 lead-free

- package in line with green environmental protection policy

2.2 Extended sub-channel UART features

- The sub-channel serial ports are independently configured, high-speed and flexible:

  Each sub-serial port is full-duplex, and each sub-serial port can be turned on/off by software

  The baud rate can be set independently, and the sub-serial port can reach up to 2M

  bps. The character format of each sub-serial port, including data length, stop digits, and parity check mode, can be set independently

  Perfect sub-serial status query function

  Can realize the software reset of a single sub-serial port

- FIFO function:

  Each sub-serial port has an independent 256-level send FIFO, and the trigger point of the send FIFO can be programmed

  Each sub-serial port has an independent 256-level receiving FIFO, and the receiving FIFO trigger point is programmable

  Software FIFO enable and clear

  FIFO status and counter output

- Error detection:

  Support parity error, data frame error, overflow error and Line-Break error detection

  Support start bit error detection

- Built-in IrDA infrared transceiver codec conforming to SIR standard, the transmission speed can reach 115.2K bit/s

Interrupt features:

With sub-serial port receiving FIFO timeout interrupt

Support Line-Break error interrupt

2.3 UART master interface characteristics

The main interface is a standard three-wire UART serial port (RX, TX, GND), without other address signals and control signal lines

Baud rate adaptive technology, the highest speed can reach 2M bit/s Optional odd

parity, even parity and no parity mode

The serial port expansion method without address line control realizes multi-serial port expansion through the built-in protocol processor of the chip

UART master interface can be set to infrared mode by pin

Support up to 16 bytes of continuous sending and receiving

2.4 SPI master interface characteristics

Maximum speed 10M bit/s only

supports SPI slave mode

SPI mode 0

supports continuous sending and receiving up to 256 bytes

2.5 IIC main interface characteristics

Support IIC bus interface

Maximum speed 1M bit/s only

supports IIC slave mode

Support up to 256 bytes of continuous sending and receiving

3. Application field

Multi-serial server/multi-serial card

Industrial/automated field RS-485 control

Wireless data transmission via 2G/3G/4G

Vehicle information platform/vehicle GPS positioning system

Remote automatic meter reading (AMR) system

POS/tax control POS/financial equipment

DSP/embedded system

4. Ordering information

Table 4.1 WK2132 Ordering Information

| Product number	encapsulation	illustrate
WK2132-ISSG	SSOP16 lead-free package	General industrial grade; working temperature -45ÿÿ+85ÿ

5. Block Diagram

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Figure 5.1 Block Diagram of WK2132
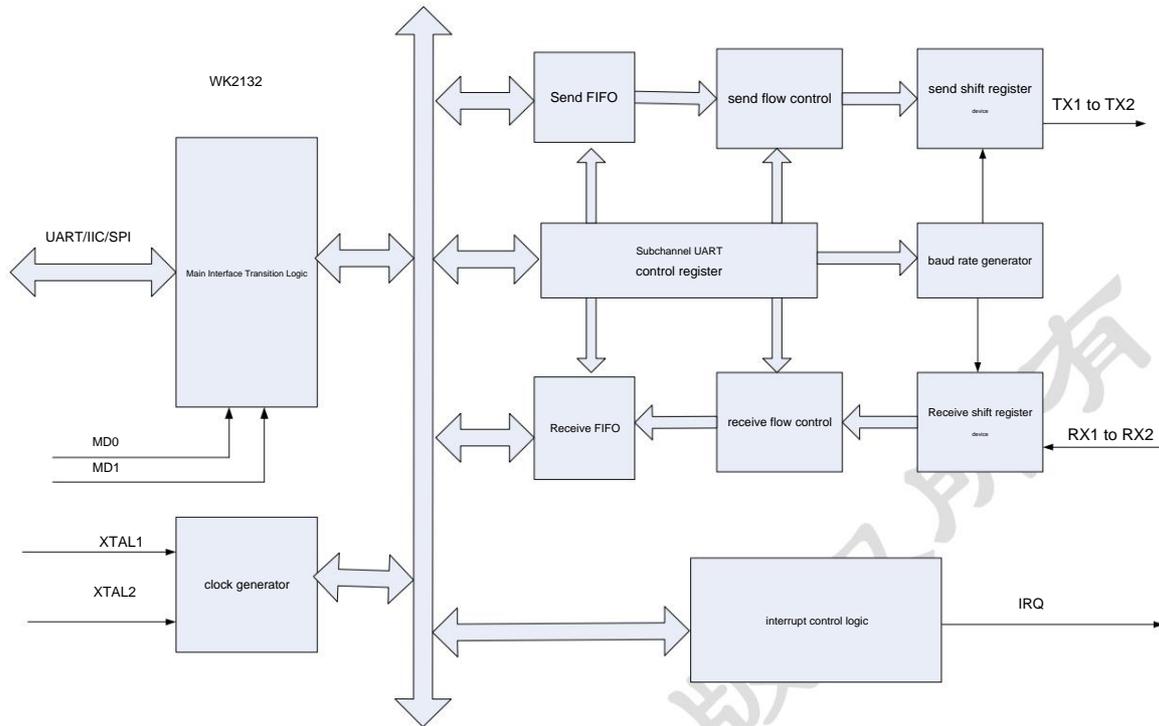
6. Package pins

6.1 Package diagram
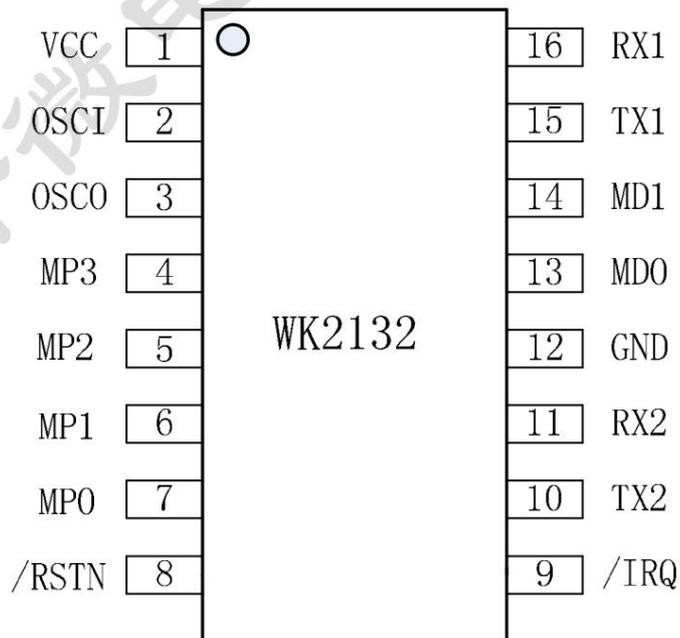
6.2 Pin Description

Table 6.2 WK2132 Pin Description

Name Pin Type Description				
VCC	1	- Power supply 2.5Vÿ5V working voltage		
GO	2	I Crystal oscillator input. Note: A 1M resistor needs to be connected in parallel with the crystal oscillator.		
OSCO	3	O Crystal oscillator output.		
MP3	4	I/O When the main interface is SPI, it is SSEL (SPI chip select) function pin: active low; When the main interface is IIC, it is the IA1 (IIC device address high) function pin; When the main interface is UART, it is the IR (main port infrared communication mode) function pin; IR=0 infrared communication mode; IR=1 Normal UART communication mode; IR is high level by default.		
MP2	5	I/O When the main interface is SPI, it is the SCLK (SPI clock input) function pin; When the main interface is IIC, it is the SCL (IIC clock input) function pin; When the main interface is UART, it is the MRX (master UART receiving) function pin.		
MP1	6	I/O When the main interface is SPI, it is the MOSI function pin; When the main interface is IIC, it is the IA0 (IIC device address low) function pin; When the main interface is UART, it is the MTX (master port UART transmit) function pin.		
MP0	7	I/O When the main interface is SPI, it is the MISO function pin; When the main interface is IIC, it is the SDA function pin; When the main interface is UART, it is NC (empty).		
RSTN	8	I Hardware reset pin, low level reset is active		
IRQ	9	O Interrupt output signal, active low. It is recommended to connect an external pull-up resistor, the typical value is 5.1K		
GND	12	- power ground		
MD0 MD1	13 14	I Master interface mode selection signal: MD1 MD0=00 SPI interface; MD1 MD0=10 IIC interface; MD1 MD0=11 UART interface; M1 M0 chip built-in pull-up circuit, M1 M0=11 when floating;		
RX1 RX2	16 11	I Sub-channel serial port serial data input. RX Input the serial data of the connected data UART to the corresponding pin of WK2132.		
TX1 TX2	15 10	O Sub-channel serial port serial data output. TX outputs serial data to the device pin it is connected to.		

7. Register description

7.1 Register list

The register address of WK2132 is numbered according to 6-bit address, address 000000ÿ111111, which is divided into global register and sub-serial port register.

There are 5 global registers, and the specific arrangement of the addresses of the global registers is shown in Table 7.1:

Table 7.1 Global register list

Register Address[5:0] Register Name Type Register Function Description		

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000000	GENA	R/W Global Control Register
000001	GRST	R/W Global sub-serial port reset register
000010	GMUT	R/W Global master serial port control register
010000	GAMES	R/W Global Interrupt Register
010001	GIFR	R Global Interrupt Flag Register

There are 16 sub-serial port registers, which are arranged as C1C0 REG[3:0], the upper two bits are the sub-serial port channel number, and the lower four bits are the register address, press

The specific arrangement of the lower 4-bit register address is shown in Table 7.2:

Table 7.2 Sub-serial port control register

Register Address[3:0]	Register Name	Type Register Function Description	
(C1,C0) 0011	SPAGE	R/W Sub-serial page control register	
(C1,C0) 0100	SCR	R/W Sub-serial port control register	SPAGE0
(C1,C0) 0101	LCR	R/W Sub-serial port configuration register	SPAGE0
(C1,C0) 0110	FCR	R/W Sub-serial port FIFO control register	SPAGE0
(C1,C0) 0111	SAYS	R/W Slave serial port interrupt enable register	SPAGE0
(C1,C0) 1000	ZERO	R/W Sub-serial interrupt flag register	SPAGE0
(C1,C0) 1001	TFCNT	R Sub-serial port send FIFO count register	SPAGE0
(C1,C0) 1010	RFCNT	R Sub-serial port receive FIFO count register Sub-	SPAGE0
(C1,C0) 1011	FSR	R serial port FIFO status register	SPAGE0
(C1,C0) 1100	LSR	R Sub-serial port receiving status register	SPAGE0
(C1,C0) 1101	FDA	R/W Sub-serial port FIFO data register	SPAGE0
(C1,C0) 0100	BAUD1	R/W Sub-serial port baud rate configuration register high byte SPAGE1	
(C1,C0) 0101	BAUD0	R/W Sub-serial port baud rate configuration register low byte SPAGE1	
(C1,C0) 0110	PRES	R/W Sub-serial port baud rate configuration register fractional part SPAGE1	
(C1,C0) 0111	RFTL	R/W Sub-serial port receive FIFO interrupt trigger point configuration register memory	SPAGE1
(C1,C0) 1000	TFTL	R/W Sub-serial port transmit FIFO interrupt trigger point configuration register memory	SPAGE1

C1, C0: sub-channel number, 00 corresponds to sub-serial port 1, 01 corresponds to sub-serial port 2

7.2 Register description

7.2.1 GENA Global Control Register: (000000)

bit	Reset value function description		type
Bit7	1	M1 M1 pin level status (M1 is high level by default)	R
Bit6	1	M0 M0 pin level status (M0 default is high level)	R
Bit5	1	RSV (reserved bit)	R
Bit4	1	RSV (reserved bit)	R
Bit3	0	RSV (reserved bit)	W/R

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Bit2	0	RSV (reserved bit)	W/R
Bit1	0	UT2EN Sub-serial port 2 clock enable bit (turn off the sub-serial port clock to achieve lower power consumption) 0: Disabled 1: enable	W/R
Bit0	0	UT1EN Sub-serial port 1 clock enable bit (turn off the sub-serial port clock to achieve lower power consumption) 0: Disabled 1: enable	W/R

7.2.2 GRST global sub-serial port reset register: (000001)

bit	Reset value function description		type
Bit7	0	RSV (reserved bit)	R
Bit6	0	RSV (reserved bit)	R
Bit5	0	UT2SLEEP Sub-serial port 2 sleep state bit (lower power consumption, can automatically wake up) 0: not sleeping 1: sleep	R
Bit4	0	UT1SLEEP Sub-serial port 1 sleep state bit (reduce power consumption, can wake up automatically) 0: not sleeping 1: sleep	R
Bit3	0	RSV (reserved bit)	W1/R0
Bit2	0	RSV (reserved bit)	W1/R0
Bit1	0	UT2RST Slave serial port 2 soft reset control bit 0: Not reset sub-serial port 2 1: Reset sub-serial port 2	W1/R0
Bit0	0	UT1RST Sub-serial port 1 soft reset control bit 0: Not reset sub-serial port 1 1: Reset sub-serial port 1	W1/R0

7.2.3 GMUT global master serial port control register: (000010)

bit	Reset value function description		type
Bit7	0	RSV (reserved bit)	W1/R0
Bit6 --- 4	0	RSV (reserved bit)	R0
Bit3	0	PAEN Master serial port verification enable control bit 0: no parity 1: Enable verification (the verification mode is determined according to the configuration of PAM1 and PAM0)	W/R
Bit2---1	0	PAM1—0 master serial port verification mode enable control bit When PAEN=1 master serial port verification is enabled: 00: Mandatory 0 parity; 01: Odd parity; 10: Even parity; 11: Mandatory 1 parity;	W/R
Bit0	0	GSTPL master serial port stop bit length setting bit 0ÿ1bit 1ÿ2bits	W/R

7.2.4 GIER global interrupt register: (010000)

bit	Reset value function description		type

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Bit7---5	000	RSV (reserved bit)	R
Bit4	0	RSV (reserved bit)	W/R
Bit3	0	RSV (reserved bit)	W/R
Bit2	0	RSV (reserved bit)	W/R
Bit1	0	UT2IE Slave serial port 2 interrupt enable control bit 0: Disabled 1: enable	W/R
Bit0	0	UT1IE Sub-serial port 1 interrupt enable control bit 0: Disabled 1: enable	W/R

7.2.5 GIFR Global Interrupt Flag Register: (010001)

Bit reset value function description		RSV (reserved	type
Bit7---4	000	bit) RSV (reserved	R
Bit3	0	bit) RSV (reserved	R
Bit2	0	bit) UT2INT Slave	R
Bit1	0	serial port 2 interrupt flag bit 0: no interrupt 1: interrupt	R
Bit0	0	UT1INT Sub-serial port 1 interrupt flag bit 0: no interrupt 1: interrupt	R

7.2.6 SPAGE sub serial port page control register: (0011)

Bit reset value function description 000000 RSV			type
Bit7 --- 1		(reserved bit) PAGE sub-serial port	R
Bit0	0	page control bit (sub-serial port registers are distributed in PAGE0 and PAGE1 On, switching between different pages is controlled by this register) 0ÿPAGE0 1ÿPAGE1	W/R

7.2.7 SCR sub-serial port control register: (PAGE0:0100)

bit	Reset value function description		type
Bit7---3	000	RSV (reserved bit)	W/R
Bit2	0	SLEEPEN Slave serial port sleep enable bit 0: Disable 1: Enable	W/R
Bit1	0	TXEN Sub-serial port transmit enable bit 0: disable 1: enable	W/R
Bit0	0	RXEN Sub-serial port receiving enable bit 0: disable 1: enable	W/R

7.2.8 LCR sub-serial port configuration register: (PAGE0:0101)

bit	Reset value function description		type
Bit7---6	00	RSV (reserved bit)	W/R
Bit5	0	BREAK Sub-serial Line-Break output control bit 0: normal output 1: Line-Break output (TX forced output 0)	W/R
Bit4	0	IREN Sub-serial infrared enable bit 0: normal mode 1: infrared mode	W/R
Bit3	0	PAEN sub-serial port check enable bit 0: No check digit (8-bit data) 1: With check digit (9-bit data)	W/R
Bit2---1	0	PAM1—0 sub-serial port check mode selection bit When PAEN=1 and the sub-serial port verification is enabled: 00: 0 parity; 01: odd parity; 10: even parity; 11: 1 parity	W/R
Bit0	0	STPL sub-serial stop bit length control bit 0ÿ1bit 1ÿ2bits	W/R

7.2.9 FCR sub-serial port FIFO control register: (PAGE0:0110)

Bit Reset Value Functional Description			type
Bit7---6	00	TFTRIG[1:0] Sub-serial port send FIFO contact setting bit When TFTL[7:0] is equal to 0: 00: 8Byte 01:16 Byte 10: 24 Byte 11:30 Byte	W/R
Bit5---4	00	RFTRIG[1:0] Sub-serial port receiving FIFO contact setting bit When RFTL[7:0] is equal to 0: 00: 8Byte 01:16 Byte 10: 24 Byte 11:28 Byte	W/R
Bit3	0	TFEN Sub-serial port transmit FIFO enable bit 0: Disable 1: Enable	W/R
Bit2	0	RFEN Sub-serial port receive FIFO enable bit 0: Disable 1: Enable	W/R
Bit1	0	TFRST Sub-serial port sends FIFO reset bit (this bit writes 1 to reset, and automatically resets after completion 0ÿ 0: reset not enabled 1: reset FIFO	W1/R0
Bit0	0	RFRST The sub-serial port receives FIFO reset bit (write 1 to reset this bit, and it will automatically set to 0)	W1/R0

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		0: reset not enabled	
		1: reset FIFO	

7.2.10 SIER slave serial port interrupt enable register: (PAGE0:0111)

Bit Reset Value		Functional Description	type
Bit7	0	FERR_IEN Receive FIFO data error interrupt enable bit 0: disable receive FIFO data error interrupt 1: Enable receive FIFO data error interrupt	W/R
Bit6	0	RSV (reserved bit)	W/R
Bit5	0	RSV (reserved bit)	W/R
Bit4	0	RSV (reserved bit)	W/R
Bit3	0	TFEMPTY_IEN transmit FIFO empty interrupt enable bit 0: Disable transmit FIFO empty interrupt 1: Enable transmit FIFO empty interrupt	W/R
Bit2	0	TFTRIG_IEN transmit FIFO contact interrupt enable bit 0: disable transmit FIFO contact interrupt 1: Enable transmit FIFO contact interrupt	W/R
Bit1	0	RXOVT_IEN Receive FIFO timeout interrupt enable bit 0: disable receive FIFO timeout interrupt 1: Enable receive FIFO timeout interrupt	W/R
Bit0	0	RFTRIG_IEN Receive FIFO contact interrupt enable bit 0: disable receive FIFO contact interrupt 1: Enable receive FIFO contact interrupt	W/R

7.2.11 SIFR slave serial port interrupt flag register: (PAGE0:1000)

Bit Reset Value		Functional Description	type
Bit7	0	FERR_INT Receive FIFO data error interrupt flag bit 0: No receive FIFO data error interrupt 1: Receive FIFO data error interrupt	W/R
Bit6	0	RSV (reserved bit)	W/R
Bit5	0	RSV (reserved bit)	W/R
Bit4	0	RSV (reserved bit)	W/R
Bit3	0	TFEMPTY_ INT Transmit FIFO empty interrupt flag 0: No transmit FIFO empty interrupt 1: Transmit FIFO empty interrupt	W/R
Bit2		TFTRIG_ INT Transmit FIFO contact interrupt flag 0: no transmit FIFO contact interrupt 1: There is a send FIFO contact interrupt	W/R
Bit1		RXOVT_ INT Receive FIFO timeout interrupt flag bit 0: No receive FIFO timeout interrupt 1: Receive FIFO timeout interrupt	W/R
Bit0	0	RFTRIG_ INT Receive FIFO contact interrupt flag bit 0: No receive FIFO contact interrupt	W/R

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		1: Receive FIFO contact interrupt	

7.2.12 TFCNT sub-serial port send FIFO count register: (PAGE0:1001)

bit	Reset value function description	type
Bit7 -- 0	00000000 The number of data in the sub-serial port sending FIFO	R

7.2.13 RFCNT sub-serial port receive FIFO count register: (PAGE0:1010)

bit	Reset value function description	type
Bit7 -- 0	00000000 The number of data in the sub-serial port receiving FIFO	R

7.2.14 FSR sub-serial port FIFO status register: (PAGE0:1011)

Bit Reset Value Functional Description			type
Bit7	0	RFOE sub-serial port receives data overflow error flag in FIFO 0: No OE error 1: OE error	R
Bit6	0	There is a Line-Break error in the data in the receiving FIFO of the RFBI sub-serial port 0: No Line-Break error 1: There is a Line-Break error (the Rx signal is always 0, including the parity bit and stop bits included)	W/R
Bit5	0	RFFE Sub-serial port receive data frame error flag in FIFO 0: No FE error 1: With FE error	W/R
Bit4	0	RFPE sub-serial port receive data verification error flag in FIFO 0: no PE error 1: There is a PE error	W/R
Bit3	0	RDAT sub-serial port receive FIFO empty flag 0: The sub-serial port receive FIFO is empty 1: The sub-serial port receiving FIFO is not empty	W/R
Bit2	0	TDAT sub-serial port send FIFO empty flag 0: Sub-serial port send FIFO is empty 1: The sub-serial port send FIFO is not empty	W/R
Bit1	0	TFULL Sub-serial transmit FIFO full flag 0: Sub-serial port send FIFO is not full 1: The sub-serial port send FIFO is full	W/R
Bit0	0	TBUSY Sub-serial port sends TX busy flag 0: Sub-serial port sends TX empty 1: The sub-serial port is busy sending TX	W/R

7.2.15 LSR sub-serial port receiving status register: (PAGE0:1100)

Bit Reset Value Functional Description			type
Bit7 - 4	0	RSV (reserved bit)	
Bit3	0	OE sub-serial port receiving FIFO currently read byte overflow error flag 0: No OE error	R

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		1: There is an OE error	
Bit2	0	Line-Break error flag of the currently read byte in the BI sub-serial port receiving FIFO	R
		0: No Line-Break error	
		1: There is a Line-Break error (the Rx signal is always 0, including the parity bit	
		and stop bits included)	
Bit1	0	FE sub-serial port receiving FIFO currently read byte frame error flag	R
		0: No FE error 1:	
		With FE error	
Bit0	0	PE sub-serial port receiving FIFO currently read byte verification error flag	R
		0: no PE error	
		1: There is a PE error	

7.2.16 FDAT sub-serial port FIFO data register: (PAGE0:1101)

bit	Reset value function description	type
Bit7 -- 0	00000000 During write operation: write the data sent by the sub-serial port to FIFO	W/R
	During read operation: read the data of the sub-serial port receiving FIFO	

7.2.17 BAUD1 sub-serial port baud rate configuration register high byte: (PAGE1:0100)

bit	Reset value function description	type
Bit7 --- 0	00000000 BAUD[15:8] High byte of sub-serial port baud rate configuration register	W/R

7.2.18 BAUD0 sub-serial port baud rate configuration register low byte: (PAGE1:0101)

bit	Reset value function description	type
Bit7 --- 0	00000000 BAUD[7:0] Low byte of sub-serial port baud rate configuration register	W/R

7.2.19 The decimal part of PRES sub-serial port baud rate configuration register: (PAGE1:0110)

bit	Reset value	function description	type
Bit7---4	0000	RSV	R
Bit3 --- 0	0000	PRES[3:0]	W/R

7.2.20 RFTL sub-serial port receive FIFO trigger interrupt register: (PAGE1:0111)

bit	Reset value function	type
Bit7 --- 0	description 00000000 Receive FIFO contact control	W/R

7.2.21 TFTL sub-serial port transmit FIFO trigger interrupt register: (PAGE1:1000)

bit	Reset value function	type
Bit7 --- 0	description 00000000 Send FIFO contact control	W/R

8. Global function description

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8.1 Reset

WK2132 is a low level reset.

The reset value of each register is listed in 7.2 Register Table.

During and after reset, each sub-serial port is in the state of prohibiting sending and receiving. When the sub-serial port is in networking mode, this feature makes

The child node where the child serial port is located will not interfere with other networked nodes during power-on and reset.

Each sub-serial port can realize software reset independently.

8.2 Clock Selection

WK2132 can choose to use the crystal oscillator clock as the clock source of the chip. Note: A 1M startup resistor needs to be connected in parallel with the crystal oscillator. See

Figure 8.2
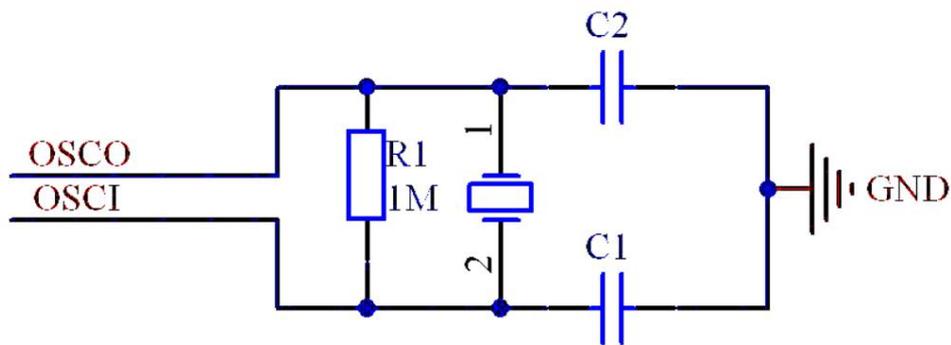
Figure 8.2 WK2132 clock circuit

8.3 Interrupt Control

WK2132 has two levels of interrupt: sub-serial port interrupt and global interrupt. When the IRQ pin indicates an interrupt, the global

Interrupt register GIFR to determine the type of the current interrupt, and then read the corresponding interrupt status register to determine the current interrupt

cut off the source.

The interrupt structure of WK2132 is shown in the figure below:
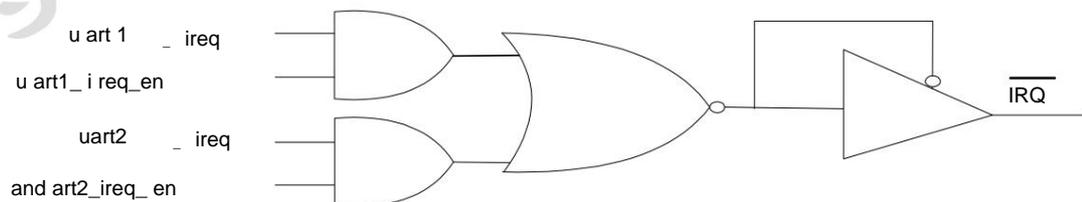
Figure 8.3 WK2132 interrupt structure diagram

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Each sub-serial port of WK2132 has an independent interrupt system, including: FIFO data error interrupt, send FIFO empty interrupt, send

Send FIFO trigger point interrupt, receive FIFO timeout interrupt, receive FIFO trigger point interrupt.

When any interrupt is enabled, the corresponding interrupt will be generated if the interrupt condition is met.

8.3.1 FIFO data error interrupt FIFO data error

interrupt indicates that there is one or more data errors in the current receiving FIFO, and the error conditions include OE

(data overflow error), FE (data frame error), and PE (parity error), BE (Line-Break error).

Once there is error data in the receiving FIFO, after reading the FSR register, the interrupt disappears; it can also be cleared by clearing the error data

Clear the interrupt.

8.3.2 Transmit FIFO Empty Interrupt This

interrupt is generated when there is no data in the transmit FIFO. When the number of data in the send FIFO is greater than the set send FIFO trigger point

, the interrupt is cleared.

8.3.3 Transmit FIFO trigger point interrupt

This interrupt is generated when the number of data in the send FIFO is less than the set send FIFO trigger point. When sending data in the FIFO

When the number is greater than the set send FIFO trigger point, the interrupt will be cleared.

8.3.4 Receive FIFO timeout interrupt When

the number of data in the receive FIFO is less than the set receive FIFO trigger point and there is no data within 4 bytes of the RX pin, a

The interruption. When the data in the receive FIFO is read or RX continues to receive data, the interrupt disappears.

8.3.5 Receive FIFO trigger point interrupt

This interrupt is generated when the number of data in the receive FIFO is greater than the set trigger point of the transmit FIFO. When the number in the receive FIFO

When the number of data is less than the set send FIFO trigger point, the interrupt is cleared.

8.4 Infrared Mode Operation

Both the main serial port and sub-serial port of WK2132 can be set to infrared communication mode. When the UART of WK2132 is set to IrDA mode

In this mode, it can communicate with devices conforming to the SIR infrared communication protocol standard, or be directly applied to optical isolation communication.

In IrDA mode, the period of one bit of data is shortened to 3/16 of that of ordinary UART, less than 1/16 of the baud period

Pulses will be ignored as noise.

8.4.1 Infrared receiving operation

The timing sequence of infrared data reception and the corresponding diagram of ordinary UART data reception are shown in Figure 8.4.1: IRX is the received red

External data signal, RX is the data decoded by infrared data. The decoded data has 1 BIT with the data on IRX

(16xCLOCK) delay. In receive mode, different from ordinary UART, RX performs a sampling in the middle of the pulse (area

Unlike the 3 samples of ordinary UART), the IrDA decoder decodes the pulse of 3/16 baud period on IRX as data 0, and the continuous low

The level is decoded as data 1.
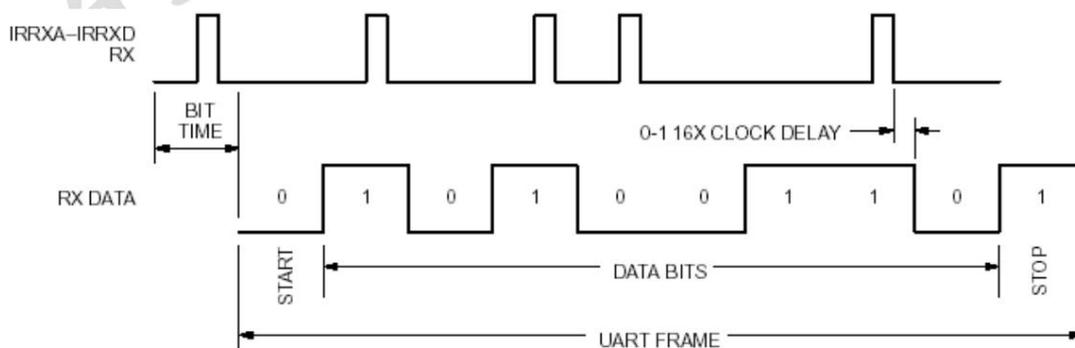
Figure 8.4.1 Infrared receiving sequence

8.4.2 Infrared sending operation

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The corresponding diagram of infrared data transmission and ordinary UART data transmission is shown in Figure 8.4.2, TX is the timing sequence of ordinary UART data transmission,

IRTX is the infrared transmission timing. When sending data 0, the infrared encoder will generate a 3/16-bit wide pulse to send through TX.

When sending data 0, keep the low level unchanged.
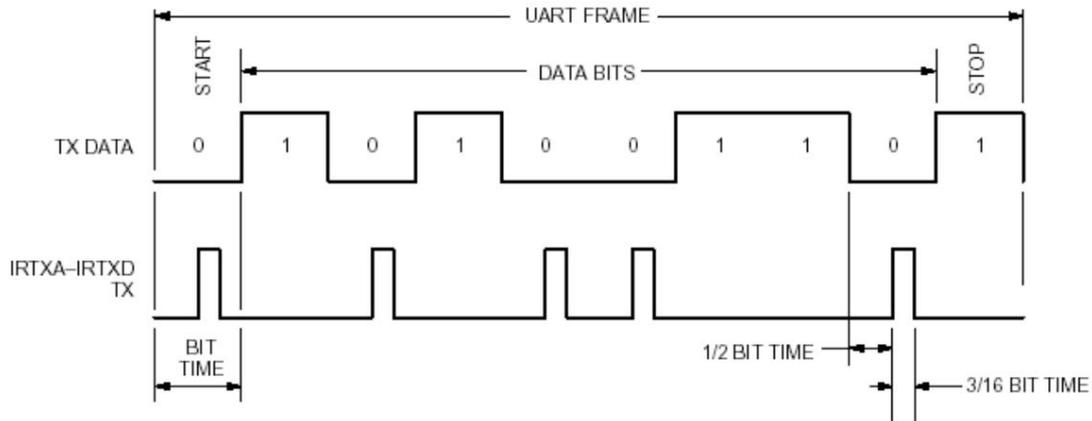
Figure 8.4.2 Infrared sending sequence

8.5 Programmable Baud Rate Generator

The main serial port and sub serial port of WK2132 use the same independent programmable baud rate generator. The Baud Rate Generator generates 16X series

The frequency division coefficient of the system clock can be set by software.

8.5.1 Common baud rate and crystal oscillator comparison table

The following table shows the serial port baud rate setting table at different system clock frequencies:

Table 8.5.1

BAUD BAUD[15-0]	PRES	baud rate Dark = 1.8432MHz	baud rate Dark = 3.6864MHz	baud rate Dark = 7.3728MHz	baud rate Dark = 11.0592MHz	baud rate Dark = 14.7456MHz
0X0002	0X00	38400	76800	153600	230400	307200
0X0005	0X00	19200	38400	76800	115200	153600
0X000b	0X00	9600	19200	38400	57600	76800
0X0017	0X00	4800	9600	19200	28800	38400
0X002f	0X00	2400	4800	9600	14400	19200
0X005f	0X00	1200	2400	4800	7200	9600
0X00bf	0X00	600	1200	2400	3600	4800
0X017f	0X00	300	600	1200	1800	2400
0X0000	0X00	115200	230400	460800	691200	921600
0X0001	0X00	57600	115200	230400	345600	460800
0X0003	0X00	28800	57600	115200	172800	230400
0X0007	0X00	14400	28800	57600	86400	115200
0X000f	0X00	7200	14400	28800	43200	57600
0X001f	0X00	3600	7200	14400	21600	28800
0X003f	0X00	1800	3600	7200	10800	14400
0X007f	0X00	900	1800	3600	5400	7200

8.5.2 Calculation of baud rate under arbitrary crystal oscillator

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Calculation formula:

$$\frac{f_s}{baud*16} = Reg$$

Note: f_s is the system clock, baud is the baud rate to be set, Reg is the calculation result (usually accurate to two decimal places)

bit)

Subtract one from the integer part of Reg and convert it into hexadecimal and write {BAUD1, BAUA0}; if there is a fractional part, take the decimal part

Write the first bit into PRES. If there is no fractional part, just write the integer part into { BAUD1, BAUA0}, and PRES into

0 is fine.

Example 1: f_s =11.0592MHz, baud =115200. Reg=6 can be obtained according to the formula. Then the data filled in the register is:

BAUD1=0X00;BAUD0=0X05;PRES=0X00.

Example 2: f_s =12MHz, baud =115200. According to the formula, Reg=6.51 (accurate to two decimal places). Then fill in the deposit

The data of the device is BAUD1=0X00; BAUD0=0X05; PRES=0X05. Example

3: High baud rate calculation

BAUD BAUD[15-0]	PRES	baud rate Dark = 8MHz	baud rate Dark = 16MHz	baud rate Dark = 24MHz
0X0000	0X00	500K	1M	1.5M
0X0001	0X00	250K	500K	750K
0X0003	0X00	125K	250K	375K

8.6 Data format setting

8.6.1 Check mode

The UART of WK2132 can provide mandatory checksum, calculate checksum and data format without checksum, through LCR (sub-serial port configuration

register) to set:

forced verification mode

WK2132 supports strong 1 checksum, strong 0 checksum and user-specified checksum mode. In this mode, the parity settings only affect the data

Sending, data receiving will ignore the parity.

In the RS-485 mode, it is recommended to use the forced check mode, in which the data and address can be easily distinguished.

Calculation check mode

WK2132 supports 1 parity, 0 parity, odd parity, even parity mode. In this mode, both received and transmitted data are

Parity calculation.

8.6.2 Data length

WK2132 supports 1 or 2-bit stop bit mode, the main serial port is set through GMUT.GSTPL, and the sub-serial port is set through LCR.STPL

place.

8.7 Sleep and automatic wake-up

WK2132 supports sleep and automatic wake-up modes, and each sub-serial port can be set separately for sleep.

Sleep conditions: 1, SCR.SLEEPEN=1

2. The receiving FIFO and sending FIFO should be empty

3. No data received on RX and no data sent on TX

4. The sub-serial port has no interruption

When the appeal conditions are met at the same time and the above state is maintained for 4 Bytes, the sub-serial port automatically enters the dormant state, and the sub-serial

The port clock is automatically turned off to reduce power consumption. At this time, judge whether the sub-serial port enters the sleep state by reading GRST.

When the sub-serial port enters the dormant state and one of the following conditions is met, the dormant sub-serial port can be automatically woken up. At this time, by reading

Take GRST to judge whether the sub-serial port is awakened.

Wake-up conditions: 1. Start receiving data on RX

2. Send FIFO write data to the sub-serial port

3. CTS pin level change

8.8 FIFO contact setting

WK2132 supports setting different trigger points for each sub-serial port, receiving FIFO and sending FIFO can set different triggers independently

point. There are two ways to set the contact: 1. Configure the fixed contact: through the TFTRIG[1:0] and RFTRIG[1:0] bits in the FCR register

Fixed programming to configure trigger point locations. 2. Configure any contact: set any trigger by setting the two registers TFTL and RFTL

point location. See Table 8.8.1 for specific configuration:

Table 8.8.1

TFTL [7:0]	TFTRIC [1:0]		TX Trigger Level	RFTL [7:0]	RFTRIG [1:0]		RX Trigger Level
= =0	0	0	8	= =0	0	0	8
= =0	0	1	16	= =0	0	1	16
= =0	1	0	24	= =0	1	0	24
= =0	1	1	30	= =0	1	1	28
! =0	X	X	TFTL	! =0	X	X	RFTL

9. SPI interface mode operation

9.1 SPI connection with host:

As shown in Figure 9.1, the SPI interface includes the following four signals:

MISO: SPI slave data output.

MOSI: SPI slave data input.

SCLK: SPI serial clock.

SSEL: SPI Chip Select (Slave Select).

The connection between WK2132 and host is shown in Figure 9.1.
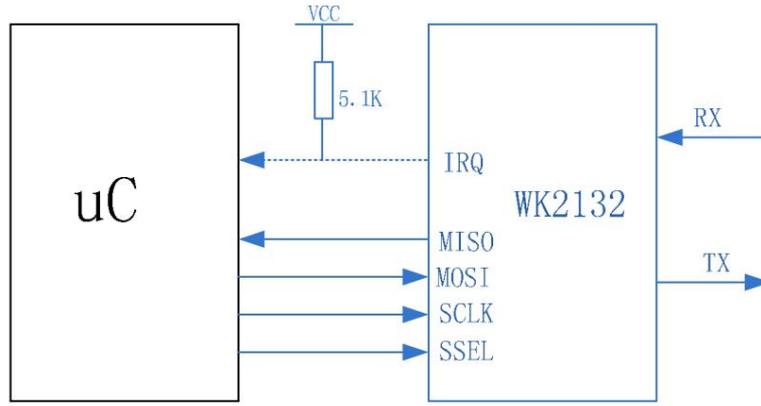
Figure 9.1 SPI and host connection diagram

9.2 Operation Timing of SPI Interface

WK2132 works in slave mode of SPI synchronous serial communication and supports SPI mode 0 standard. For implementing host and WK2132

For communication, it is necessary to set CPOL=0 (SPI clock polarity selection bit) and CPHA=0 (SPI clock phase selection bit) on the host side.

The operation sequence of WK2132 SPI interface is as follows:

The sequence of write register operations is shown in Figure 9.2: first write a command byte (Command Byte), then write the corresponding data

By byte, the register address of the data byte is automatically incremented.
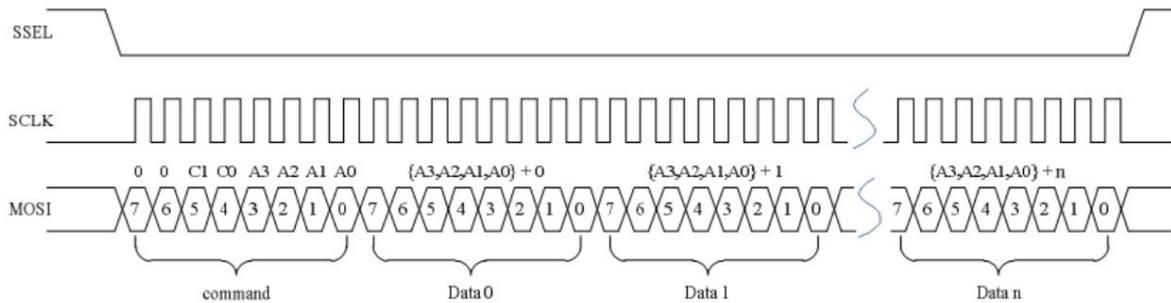
Figure 9.2 SPI write register timing diagram

The timing of the read register operation is shown in Figure 9.3: first write a command byte (Command Byte), and then the chip MISO line

The corresponding data bytes are returned. The register address of the returned data byte is automatically incremented.
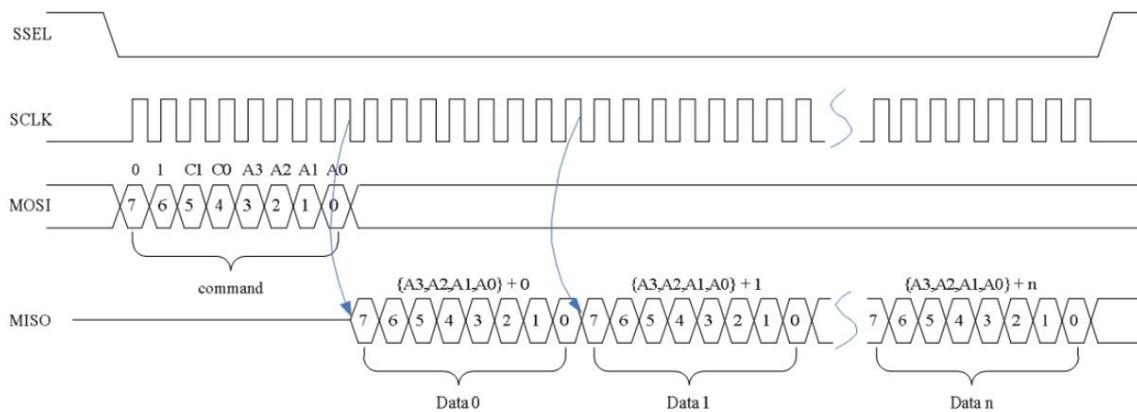

Figure 9.3 SPI read register timing diagram

The timing sequence of writing FIFO operation is shown in Figure 9.4: first write a command byte (Command Byte), and then write the corresponding data

Byte. The FIFO address is automatically incremented.
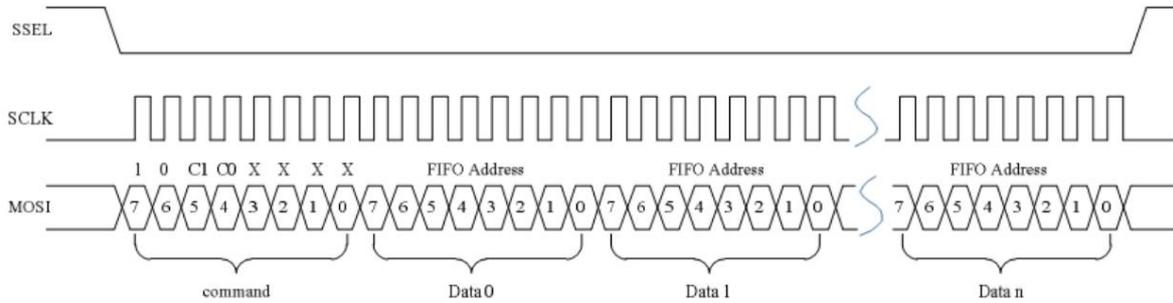
Figure 9.4 SPI write FIFO timing diagram

The timing sequence of reading FIFO operation is shown in Figure 9.5: first write a command byte (Command Byte), then the chip MISO line

The corresponding data bytes are returned. The FIFO address is automatically incremented.
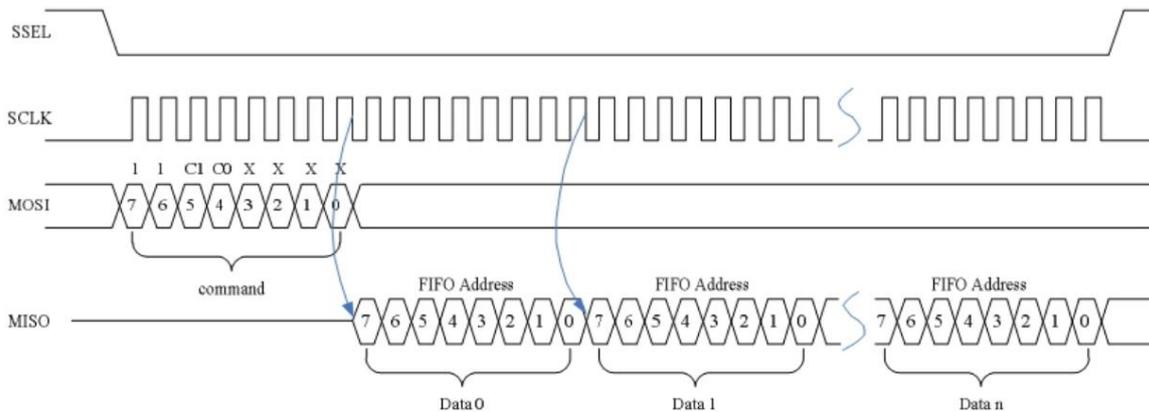
Figure 9.5 SPI read FIFO timing diagram

9.3 SPI bus communication protocol description:

9.3.1. SPI write register

SPI	Control byte CMD								Data byte DB (write N data bytes, register device address is automatically incremented)							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0 MOSI		0	C1	C0 A3	A2 A1	A0 D7t	D6t D5t	D4t D3t	D2t D1t D0t							
MISO	HZ HZ HZ			HZ HZ HZ HZ	HZ HZ HZ HZ HZ HZ	HZ HZ HZ										

9.3.2. SPI read register

SPI	Control byte CMD								Data byte DB (read N data bytes, register device address is automatically incremented)							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0 MOSI		1	C1	C0 A3	A2 A1	A0			X	X	X	X	X	X	X	X

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| MISO | HZ | HZ | HZ | | | HZ | HZ | HZ | HZ | HZ | D7t | D6t | D5t | D4t | D3t | D2t | D1t | D0t | | | | | | |

9.3.3. SPI write FIFO

SPI	control byte CMD								Data bytes DB (write N data bytes to {C1C0}'s FIFO, the FIFO address is automatically incremented)							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
MOSI 1		0	C1	C0	X	X	X	D7t	D6t	D5t	D4t	D3t	D2t	D1t	D0t		
MISO	HZ HZ HZ			HZ HZ HZ HZ HZ HZ HZ HZ HZ					HZ	HZ	HZ					

9.3.4. SPI read FIFO

SPI	control byte CMD								Data byte DB (read N bytes from the FIFO of {C1C0} data bytes, FIFO address is automatically incremented)							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
MOSI 1		1	C1	C0	X	X	X	X	X	X	X	X	X	X	X	X
MISO	HZ HZ HZ			HZ HZ HZ HZ D7t D6t D5t D4t					D3t	D2t	D1t	D0t				

illustrate:

C1 C0: sub-serial port channel number 00~11 respectively corresponding to sub-serial port 1 to sub-

serial port 4 A3-A0: sub-serial port register address

D7t…D0t: 8-bit data bytes

10. UART interface mode operation

10.1 Connection between UART interface and host computer

When the main interface of WK2132 is UART, only RX and TX need to be connected to the host. Use standard UART protocol for communication. Main interface UART

Can realize baud rate self-adaptation. After power-on reset, first write 0x55 to WK2132, and WK2132 can automatically measure according to the written data

At this time, the baud rate of the MCU and the baud rate of the main interface UART are locked, and communication will be performed at this baud rate in the future; if the main interface needs to

To change the baud rate, you need to reset the chip hardware, and then test and lock the baud rate again.

The interface between WK2132 and the host is shown in Figure 10.1:

Figure 10.1 UART interface and host connection diagram

10.2 Operation Timing of Master UART Interface

When writing, first write a command byte (Command Byte) to the MRX of WK2132, and then write the corresponding data byte.

The operation sequence (without verification mode) is shown in Figure 10.2.1:
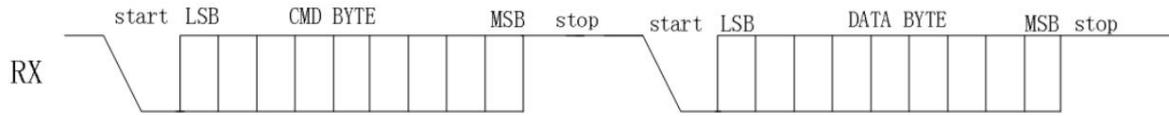

Figure 10.2.1 UART master interface write operation sequence

In the read operation, first write the command byte to the RX of WK2132, and the corresponding data byte is read from the MTX, and its operation timing (no check mode

formula) as shown in Figure 10.2.2
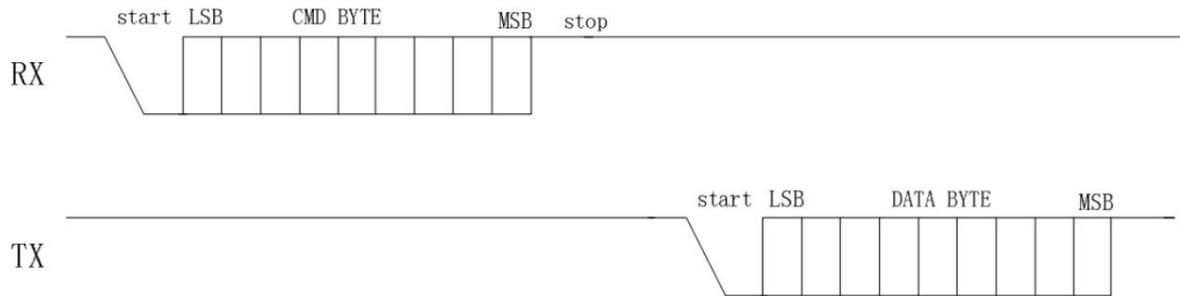
Figure 10.2.2 UART master interface read operation timing

10.3 Main UART communication transmission protocol description:

10.3.1. Write register:

Classification	Control byte CMD								1 data byte DB (downstream)							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
TX	0	0	C1	C0	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
RX																

10.3.2. Write FIFO: (multi-byte write)

classification	control byte CMD								[N3 N2 N1 N0] data bytes DB (downstream)							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
TX	1	0	C1	C0	N3	N2	N1	N0	D7	D6	D5	D4	D3	D2	D1	D0
RX																

10.3.3. Read register:

Classification	Control byte CMD								1 data byte DB (upstream)							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
TX	0	1	C1	C0	A3	A2	A1	N0								
RX									D7	D6	D5	D4	D3	D2	D1	D0

10.3.4. Read FIFO: (multi-byte read)

Classification	Control byte CMD								[N3 N2 N1 N0] data bytes DB (upstream)							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
TX	1	1	C1	C0	N3	N2	N1	N0								
RX									D7	D6	D5	D4	D3	D2	D1	D0

illustrate:

C1, C0: sub-serial port channel number, 00~11 correspond to sub-serial port 1 to sub-serial port 4 respectively.

A3, A2, A1, A0: sub-serial port register address;

N3, N2, N1, N0: the number of data bytes written/read from FIFO; when it is 0000, it indicates that there is one data byte after it; when When it is 1111, it indicates that 16 data bytes

follow; There are two ways to read/write data

to the sub-serial port: a. Read/write register mode, read/write to the sub-serial port FIFO register FDAT (1111), once Can only read/write one byte; b. Read/write FIFO mode, directly read/write to receive/send FIFO, and can read and write up to 16 consecutive data at a time

10.4 Main UART interface infrared operation mode

When the IR pin of the main serial port is connected to high level, the main UART of WK2132 works in the infrared mode, and the communication between the main UART and the host follows the infrared communication

Protocol, see 8.8 Infrared Mode Operation for its operation timing.

When the IR pin of the main serial port is connected to low level, WK2132 works in normal mode.

11. IIC interface bus mode operation

The two-wire IIC bus consists of a serial data line SDA and a serial clock line SCL. When the bus is idle, the two

Both lines are pulled to the positive supply voltage through pull-up resistors. Each device has an independent address. As shown in Figure 11,
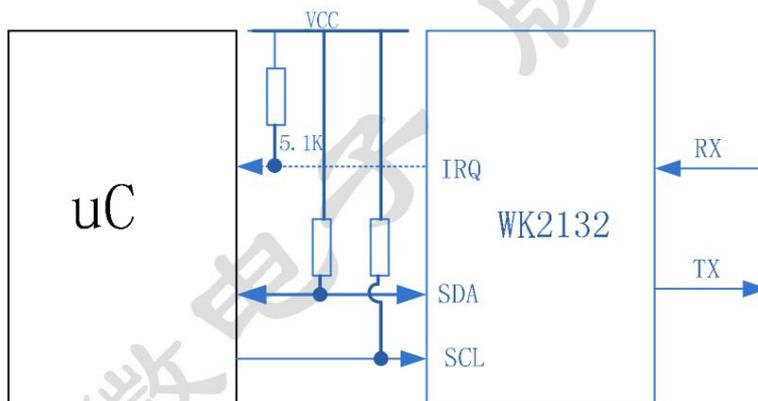

Figure 11 Schematic diagram of IIC main interface

11.1 Data transfer

Each bit of data is transmitted with an always pulse. The data on the SDA line must remain stable during the period that SCL is high. Changing data on the SDA line at this time is considered a control signal. When SCL is high, a high-to-low transition of the SDA line data represents a start bit, and a low-to-high transition represents a stop bit. The bus is considered busy after a start bit; it is considered free after a stop bit.

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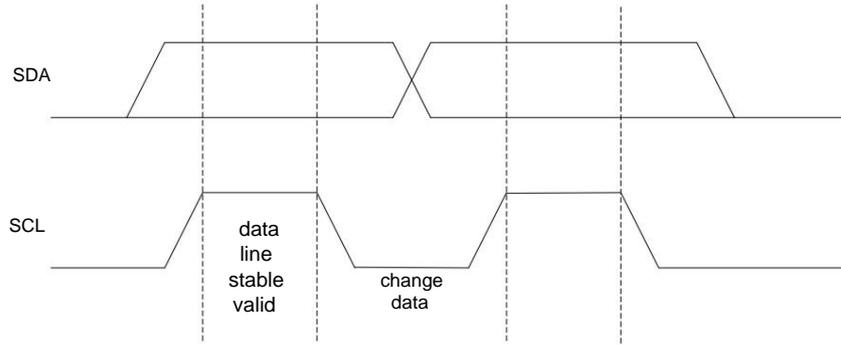

Figure 11.1.1 Data transmission
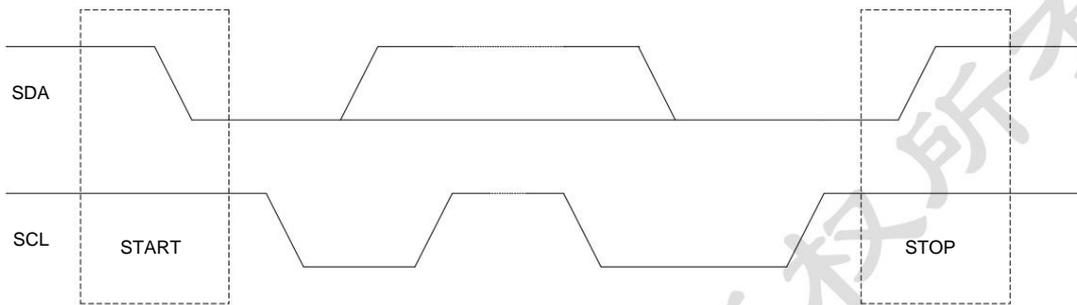
Figure 11.1.2 Start bit and stop bit

The data from the master to the slave between the start bit and the stop bit must be 8 bits long, the high bit first and there must be an acknowledge bit. The clock that matches the acknowledge bit is generated by the master. When the master releases the bus, the responding device must pull the SDA line low during the acknowledge cycle.

11.2 Operation Timing of Main IIC Interface

11.2.1.IIC write register:

The operation timing of writing registers is shown in Figure 11.2.1. First write a command byte (Command Byte), and then write to the register address byte, and finally write the corresponding data byte, the register address of the data byte will automatically increase.
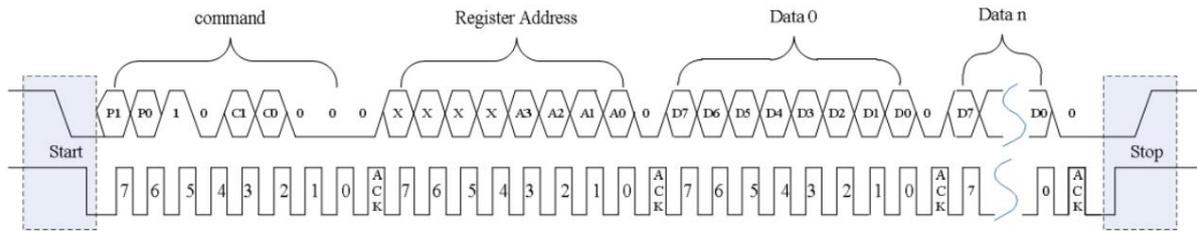

Figure 11.2.1 IIC write register operation timing

11.2.2.IIC read register:: The timing

sequence of read register operation is shown in Figure 11.2.2: IIC read register operation is completed in two steps. Write a command byte first (Command Byte), and then write the register address byte to complete this write operation. Then start the second operation, first write a command byte (Command Byte), then read in the corresponding data byte, the register address is automatically increased.

WK2132 Data Sheet Ver1.0
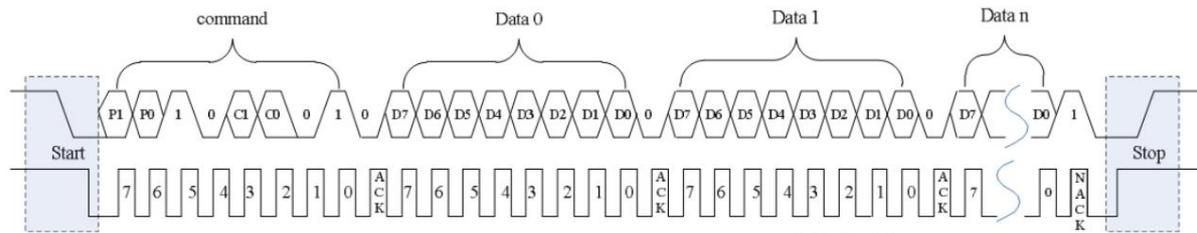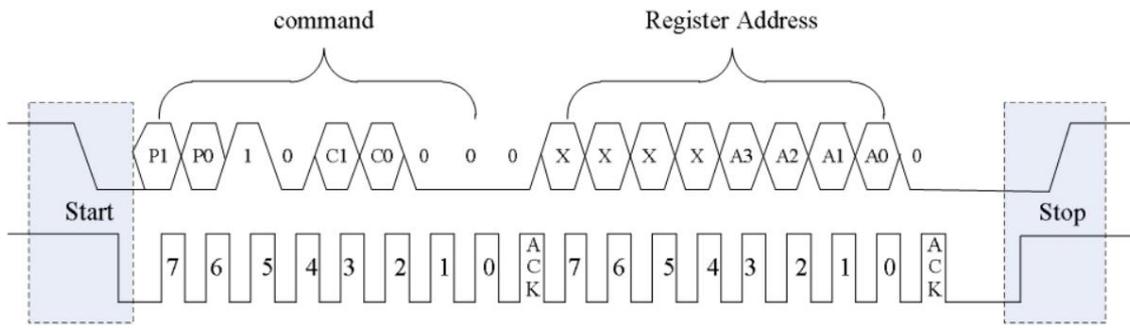
Figure 11.2.2 IIC read register operation timing

11.2.3.IIC write FIFO:

The timing of writing FIFO operations is shown in Figure 11.2.3, first write a command byte (Command Byte), and then write N bytes

data, the FIFO address is automatically incremented.
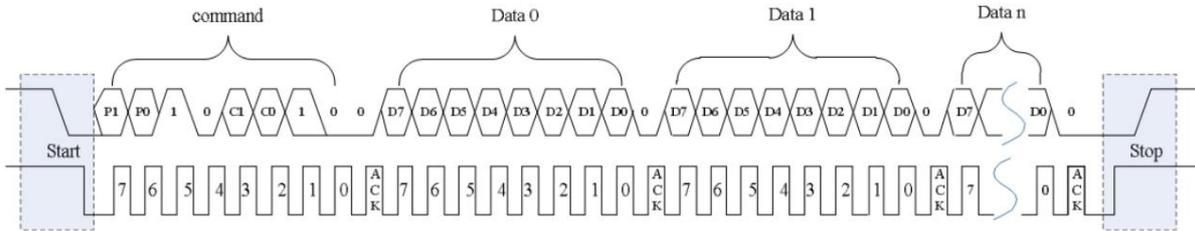
Figure 11.2.3 IIC write FIFO operation timing

11.2.4.IIC description FIFO:

The timing of reading FIFO operation is shown in Figure 11.2.4, first write a command byte (Command Byte), and then read N data

bytes, the FIFO address is automatically incremented.
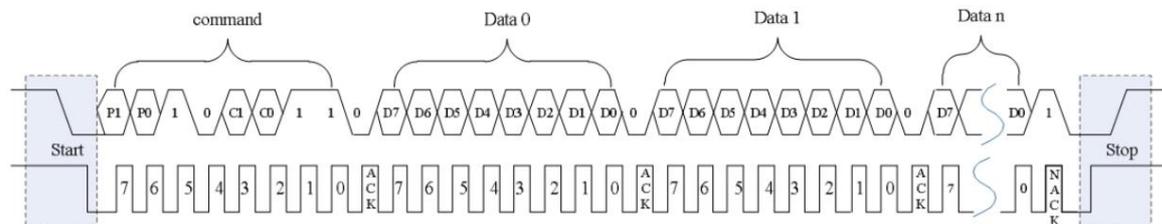
Figure 11.2.4 IIC read FIFO operation sequence

11.3 Address:

Every device on the bus must have its own unique address. Before data is transferred on the bus, the master sends

Send the address of the slave to start a transfer. All slaves will compare addresses, and if there is the same address in the network, of course they will reply to the master.

address request. The upper 2 bits of the first byte of the address transmitted after the start bit are transmitted. The address of each device is controlled by the A1A0 pin,

Then the programming only needs to correspond the value of P1P0 with the value of IA1 and IA0.

### 11.4 Transmission protocol:

11.4.1. Write register:

11.4.2. Read register:
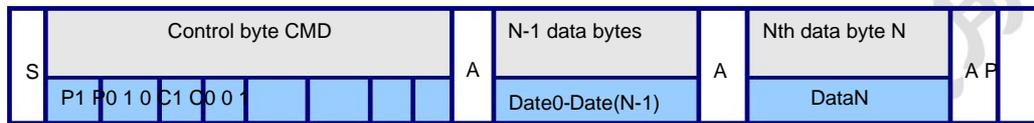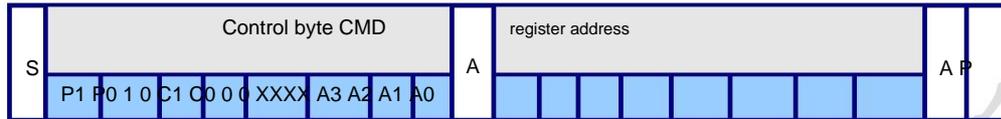
11.4.3. Write FIFO:

11.4.4.The FIFO:
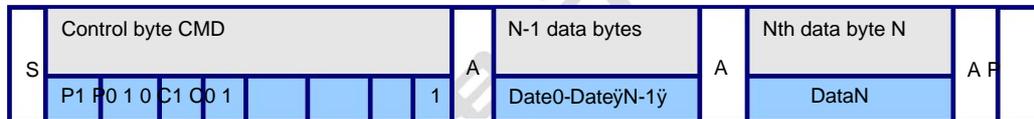
illustrate:

Note: When the MCU does not need to continue to receive data from WK2132, it does not need to send a response after receiving the current byte.

Just give the answer clock.

C1, CO: Sub-serial port channel number, 00~11 correspond to sub-serial port 1 to sub-serial port 4

A3, A2, A1, A0: sub-serial port register address

P1, P0: for the device address, this is controlled by the chip pin IA1, IA0

S: start bit P: stop bit A: response bit NA: no response signal

12. Sub-serial port operation description

12.1 Enable/disable sub-serial port

WK2132 allows to enable or disable each sub-serial channel independently.

Unused sub-serial channels can be prohibited during use.

The sub-serial port channel can receive and send data only when it is enabled.

12.2 Transceiver FIFO Control

WK2132 provides independent 256-level FIFO receiving and sending FIFO. (sub-serial port FIFO control register) to set.

12.2.1 Transmit FIFO trigger point operation

WK2132 provides independent programmable send FIFO trigger point settings for each channel to generate corresponding send FIFO trigger point interrupts.

When the transmit FIFO trigger point interrupt is enabled, a corresponding interrupt will be generated when the number of data in the transmit FIFO is less than the set trigger point.

12.2.2 Receive FIFO trigger point operation

WK2132 provides independent programmable receive FIFO trigger point settings for each channel to generate corresponding receive FIFO trigger point interrupts. When the receive FIFO trigger point interrupt is enabled, a corresponding interrupt will be generated when the number of data in the receive FIFO is greater than or equal to the set trigger point.

12.2.3 Enable/Disable Transmit FIFO After reset,

transmit FIFO is disabled. If you want to write data into the transmit FIFO, you need to enable the transmit FIFO first. Whether the data in the send FIFO is sent depends on whether the corresponding sub-channel UART is enabled. Once the corresponding sub-channel UART is enabled, the data in the send FIFO will be sent immediately, otherwise, the data in the send FIFO will not be sent until the corresponding sub-channel is enabled.

12.2.4 Enable/disable

receive FIFO After reset, the receive FIFO is disabled.

If you want to receive sub-serial port data, you need to enable the corresponding sub-serial port communication first.

channel and its receive FIFO. Only after the corresponding UART and receive FIFO are enabled, the received data can be written into receive FIFO storage.

If the sub-serial port channel is enabled and the receiving FIFO is disabled, the sub-serial port can receive data, but the data will not be written into the receiving FIFO and will be ignored. 12.2.5

Empty send FIFO When the send FIFO clear bit (TFRST) in FCR is set to 1, the data in the send FIFO of this sub-channel will be cleared, and the send FIFO Both counters and pointers will be cleared.

After the TFRST bit is set to 1, it will be automatically cleared to 0 by hardware after

one clock. 12.2.6 Clear the receive FIFO

When the receive FIFO clear bit (RFRST) in the FCR is set to 1, the data in the receive FIFO of the sub-channel will be cleared, and the receive FIFO Both counters and pointers will be cleared.

After the RFRST bit is set to 1, it will be automatically cleared to 0 by hardware after

one clock. 12.2.7 Send FIFO counter WK2132

uses an 8-bit register to reflect the number of data in the current send FIFO: when a byte of data is written into the send FIFO

After that, the send FIFO counter automatically increases by 1; when the data in a send FIFO is sent, the send FIFO counter automatically decreases by 1. Note: When the sending FIFO counter is 255 (11111111), if another data is written, the counter will become 0 (00000000). When the sending FIFO counter is 1 (00000001), the counter also becomes 0 (00000000) after sending a data. Therefore, when the transmit FIFO counter is 0, it indicates that the transmit FIFO is full or empty. In this case, it needs to be judged in conjunction with the relevant status bits in the sub-serial port status register (FSR).

12.2.8 Receive FIFO counter WK2132 uses

an 8-bit register to reflect the number of data in the current receive FIFO: when a byte of data is written into the receive FIFO

After that, the receiving FIFO counter automatically increases by 1; when the data in a receiving FIFO is read, the receiving FIFO counter automatically decreases by 1.

Note: When the receiving FIFO counter is 255 (11111111), if another data is received, the counter becomes 0 (00000000). When the receiving FIFO counter is 1 (00000001), the counter also becomes 0 (00000000) after reading one data. Therefore, when the receiving FIFO counter is 0, it indicates that the receiving FIFO is full or empty. In this case, it needs to be judged in conjunction with the relevant status bits in the sub-serial port status register (FSR).

13. Parameter index

13.1 Static parameters of WK2132

Unless otherwise specified, meet: VCC=(2.5V±0.2V) or (3.3±0.3V) or (5V); -40°C to +85°C;

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SPI/UART/IIC interface wide operating voltage 2-channel 256-level FIFO high-speed UART

symbol	illustrate	condition	VCC=2.5V	VCC=3.0V				VCC=5.0V Single	
			min max	min ma	x min max	bit			
power supply									
VCC supply voltage ICC			2.3	2.7	3.0	3.6	4.5	5.0	V
operating current 3.6864MHz crystal oscillator			0.8	2	1	2	2	3	mA
ICCSL sleep current		no load	150	-	200	-	460	-	uA
input logic signal									
VIH input high level			1.8	5.0	2.0	5.0	3.6	5.0	V
VIL input low level			-	0.6	-	0.9	-	1.1	V
IIL input leakage current VI=5.0 or 0V CI input			- ±10		-	±10	-	±10	uA
capacitor output logic			-	5	-	5	-	5	pF
signal									
VOH output high level IOH=3mA VOL output			1.9	·	2.4	·	4.5	-	IN
low level IOL=-3mA IOL output leakage current			-	0.4	-	0.4	0	0.4	V
			- ±10		-	±10	-	±10	uA
Co output capacitance			-	5	-	5	-	5	pF

13.2 Dynamic parameters of WK2132

symbol	illustrate	condition	VCC=2.5V	VCC=3.0V				VCC=5.0V Single	
			min max	min ma	x min max	bit			
FOSI crystal frequency			-	16	-	24	-	32	MHz

13.3 Limit parameters of WK2132

Symbol Description	condition	the smallest	maximum	unit
VCC supply voltage		-0.5	6	IN
VI input voltage		-0.5	+5.5	IN
VO output voltage		-0.5	+5.5	IN
PTOL total power consumption		-	300	mW
TO operating temperature		-40	+85	ÿ
TSTG storage temperature		-65	+150	ÿ

14. Package information

WK2132 adopts SSOP16 lead-free green package

Figure 14.1 SSOP16 Package Information
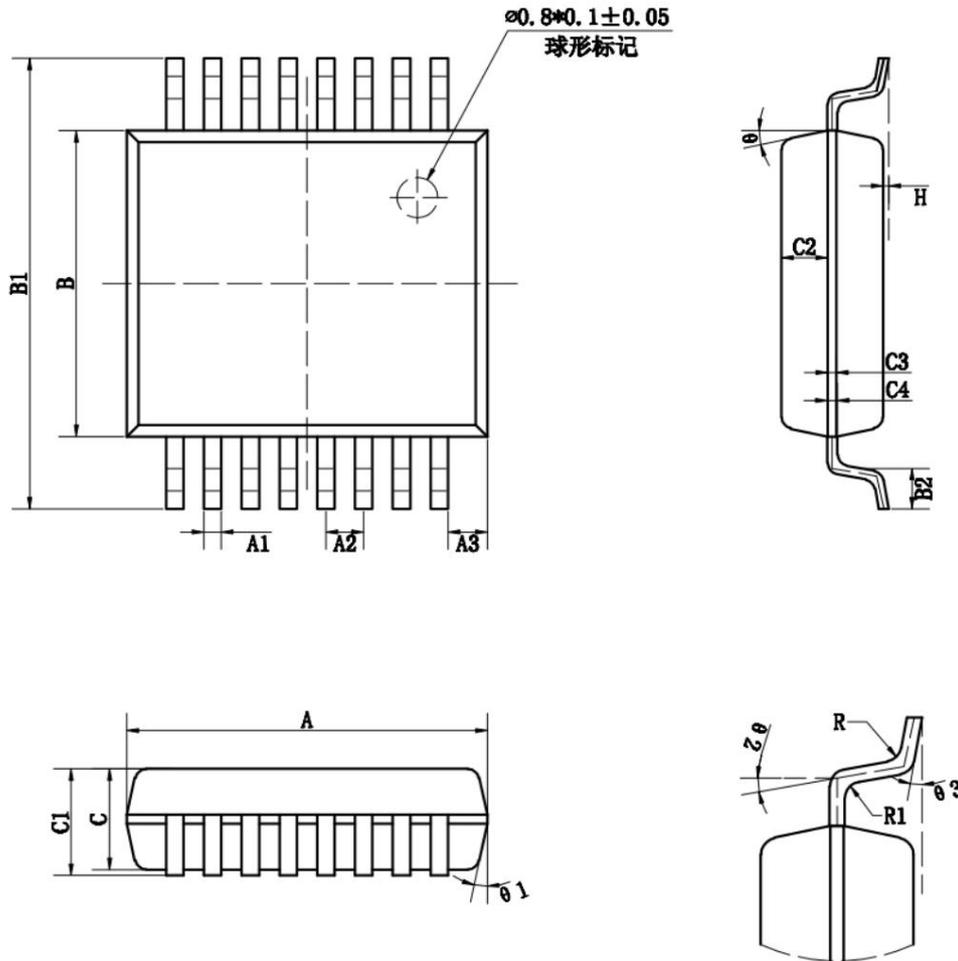
size label	Minimum (mm) Maximum (mm)		size label	Minimum (mm) Maximum (mm)	
A	6.15	6.25	C3	0.152	
A1	0.30TYP		C4	0.172	
A2	0.65TYP		H	0.05	0.15
A3	0.675TYP		i	12°TYP4	
B	5.25	5.35	i2	12°TYP4	
B1	7.65	7.95	i2	10° TYPE	
B2	0.60	0.80	i3	0°ÿ 8°	
C	1.70	1.80	R	0.20TYPE	
C1	1.75	1.95	R1	0.15TYP	
C2	0.799				

15. welding process

WK2132 uses green environmental protection materials, and the pins are electroplated with pure tin. The recommended peak temperature is less than 260°C, which meets the lead-free standard

Standard reflow soldering process for soldering.

All SMD device soldering processes are sensitive to humidity (see the outer packing box for humidity levels and conditions), and it is recommended to dry them before soldering.

When manual soldering is used, two diagonal pins should be soldered first for fixing, and then other pins should be soldered. The soldering temperature is 300°C,

The contact time between the soldering iron and the pin is controlled within 10 seconds.

16. special statement

This product is not designed for life support systems, aerospace systems, all consequences caused by the application of this product in this field, for

Kai Microelectronics will not assume any responsibility. Weikai Microelectronics reserves the right to modify the performance, function and parameters of the product. For positive

For mass-produced products, users will be notified of changes made for Kaiwei Electronics through announcements.

17. version history

Versions prior to V1.0 are internal versions that have not been officially released.

Release Date		Modify content
V1.0	2017.09	Create a file

18. contact information

. Please visit WKMIC website for our latest contact information: www.wkmic.com

QQ3002931911   13148878879