TECHNICAL SPECIFICATION

Model Number : IL0398

Description : Compatible with UC8176

DALIAN QIYUN DISPLAY CO., LTD.

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INTRODUCTION

This driver is an all-in-one driver with timing controller for ESL. Its output is of 1-bit white/black and 1-bit red resolution per pixel. The timing controller provides control signals for the source driver and gate drivers.

The DC-DC controller allows it to generate the source output voltage VDH/VDL (+/-2.4V~+/-11V). The chip also includes an output buffer for the supply of the COM electrode (VCOMAC or VCOMDC). The system is configurable through a 3-wire/4-wire (SPI) serial interface.

MAIN APPLICATIONS

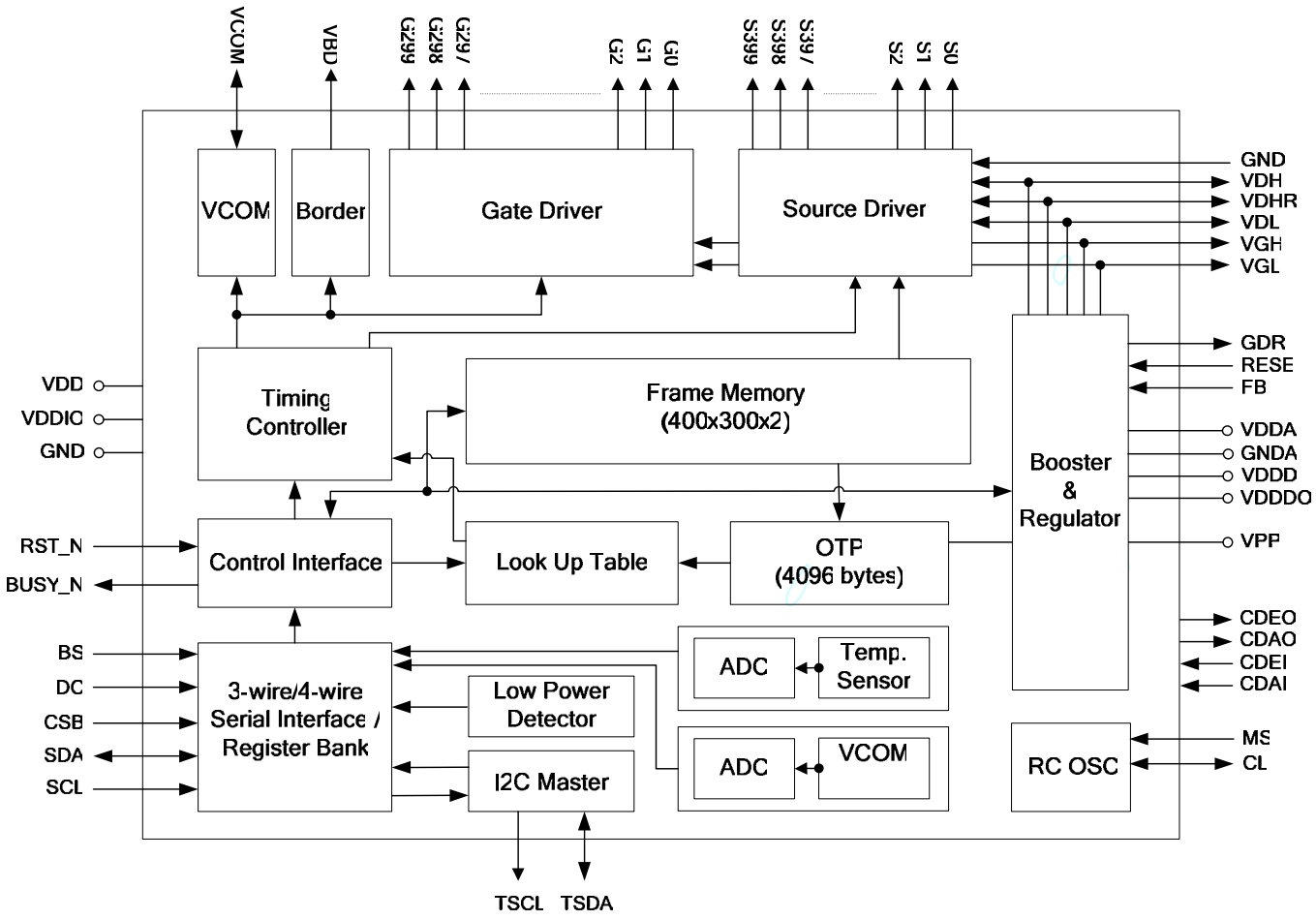
- E-tag application

FEATURE HIGHLIGHTS

- System-on-chip (SOC) for ESL
- Timing controller supports several all-resolutions
- Resolution:
  - Up to 400 source x 300 gate resolution + 1 border + 1 Vcom
  - 1 bit for white/black and 1 bit for red per pixel
- Cascade: Up to 2 chip cascade mode
- Memory (Max.): 400 x 300 x 2 bits SRAM
- 3-wire/4-wire (SPI) serial interface
  - Clock rate up to 20MHz
- Temperature sensor:
  - On-Chip: -25~50 ^{o}C +/- 2.0^{o}C / 8-bit status
  - Off-Chip: -55~125^{o}C +/- 2.0^{o}C /11-bit status (I^2C/LM75)
- Support LPD, Low Power Detection (V_{DD}<2.5V)
- OSC / PLL: On-chip RC oscillator (1.625MHz +/- 5%)
- Vcom:
  - AC-Vcom / DC-Vcom (by LUT)
  - Support Vcom sensing (6-bit digital status)
- Charge Pump: On-chip booster and regulator:
  - VGH: +16V
  - VGL: -16V
  - VDH: +2.4 ~ +11.0V (programmable, black/white)
  - VDL: -2.4 ~ -11.0V (programmable, black/white)
  - VDHR: +2.4 ~ +11.0V (programmable, red)
- Digital supply voltage (VDD/AVDD) : 2.3~ 3.6V
- OTP: 4K-byte OTP for LUT
- Package: (TBD)
- COM/SEG bump information
  Bump pitch: (TBD) µM
  Bump gap: (TBD) µM +/- 3µM
  Bump surface: (TBD) µM^2

Remark: Contact UltraChip for a visual inspection document (03-DOC-093).

BLOCK DIAGRAM



PIN DESCRIPTION

Type: I: Input, O: Output, I/O: Input/Output, PWR: Power, C: Capacitor pin

Pin (Pad) Name	Pin Count	Type	Description
POWER SUPPLY PINS			
VDD	7	PWR	Digital power
VDDA	10	PWR	Analog power
VDDIO	10	PWR	IO power
VDDDO	5	PWR	Digital power output (1.8V)
VDDD (VDDDI)	5	PWR	Digital power input (1.8V)
VPP	7	PWR	OTP program power (7.75V)
VDM	4	PWR	Analog Ground.
GND	32	PWR	Digital Ground.
GNDA	10	PWR	Analog Ground
LDO PINS			
VDH (VSH)	10	I/O	Positive source driver Voltage (+2.4V ~ +11V)
VDHR	8	I/O	Positive source driver voltage for Red (+2.4V ~ +11V)
VDL (VSL)	10	I/O	Negative source driver voltage (-2.4V ~ -11V)
CONTROL INTERFACE PINS			
BS	1	I	Bus Selection. Select 3-wire / 4-wire SPI interface L: 4-wire interface. **H: 3-wire interface. (Default)**
RST_N	1	I (Pull-up)	Global reset pin. Low: reset. When RST_N become low, driver will reset. All registers will be reset to their default value, and all driver functions will be disabled. SD output and VCOM will be based on its previous condition; and may have two conditions: 0V or floating.
MS	1	I	Cascade setting pin. L: Slave chip. H: Master chip.
CL	1	I/O	Clock input/output pin. Master: Clock output. Slave: Clock input.
CDEI	1	I	Cascade signal input pin.
CDEO	1	I	Cascade signal output pin.
CDAI	1	I	Cascade data input pin.
CDAO	1	I	Cascade data output pin.
BUSY_N	1	O	Driver busy flag. L: Driver is Busy. H: Host side can send command/data to driver.
MCU INTERFACE (SPI) PINS			
CSB	1	I	Serial communication chip select.
SDA	1	I/O	Serial communication data input/output
SCL	1	I	Serial communication clock input.
DC	1	I	Command/Data input. L: command H: data

Pin (Pad) Name	Pin Count	Type	Description
I²C INTERFACE			
TSCL	2	O (open-drain)	I²C clock (External pull-up resistor is necessary.)
TSDA	2	I/O (open-drain)	I²C data (External pull-up resistor is necessary.)
OUTPUT PINS			
S0~S399 (S<0>~S<399>)	400	O	Source driver output signals.
G0~G299 (G<0>~G<299>)	300	O	Gate driver output signals.
VCOM	16	O	VCOM output.
VBD (VBD<1>~VBD<2>)	1x2	O	Border output pins.
BOOSTER PINS			
GDR	8	O	N-MOS gate control
RESE	2	P	Current sense input for control loop.
FB	2	P	(Keep Open.)
VGH	14	I/O	Positive Gate voltage.
VGL	16	I/O	Negative Gate voltage.
RESERVED PINS			
VSYNC	1	O	UltraChip reserved. Leave it floating.
TEST1~TEST3	1x3	I	UltraChip reserved. Leave it floating or connected to VSS.
TEST4~TEST7	1x4	O	UltraChip reserved. Leave it floating.
TEST8~13	1x6		
TESTVDD	1	I	UltraChip reserved. Connected to VSS.
DUMMY	71	-	UltraChip reserved. Leave it floating.
NC	28	--	Not Connected.
GD<0>~GD<3>	1x4		

COMMAND TABLE

W/R: 0: Write Cycle 1: Read Cycle C/D: 0: Command / 1: Data D7~D0: –: Don't Care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	Panel Setting (PSR)	0	0	0	0	0	0	0	0	0	0		00h
		0	1	#	#	#	#	#	#	#	#	RES[1:0],REG,KW/R,UD,SHL, SHD_N,RST_N	0Fh
2	Power Setting (PWR)	0	0	0	0	0	0	0	0	0	1		01h
		0	1	--	--	--	--	--	--	#	#	VDS_EN, VDG_EN	03h
		0	1	--	--	--	--	--	#	#	#	VCOM_HV,VGHL_LV[1:0]	00h
		0	1	--	--	#	#	#	#	#	#	VDH[5:0]	26h
		0	1	--	--	#	#	#	#	#	#	VDL[5:0]	26h
		0	1	--	--	#	#	#	#	#	#	VDHR[5:0]	03h
3	Power OFF (POF)	0	0	0	0	0	0	0	0	1	0		02h
4	Power OFF Sequence Setting (PFS)	0	0	0	0	0	0	0	0	1	1		03h
		0	1	--	--	#	#	--	--	--	--	T_VDS_OF	00h
5	Power ON (PON)	0	0	0	0	0	0	0	1	0	0		04h
6	Power ON Measure (PMES)	0	0	0	0	0	0	0	1	0	1		05h
7	Booster Soft Start (BTST)	0	0	0	0	0	0	0	1	1	0		06h
		0	1	#	#	#	#	#	#	#	#	BT_PHA[7:0]	17h
		0	1	#	#	#	#	#	#	#	#	BT_PHB[7:0]	17h
		0	1	--	--	#	#	#	#	#	#	BT_PHC[5:0]	17h
8	Deep sleep (DSLP)	0	0	0	0	0	0	0	1	1	1		07h
		0	1	1	0	1	0	0	1	0	1	Check code	A5h
9	Display Start Transmission 1 (DTM1, White/Black Data) (x-byte command)	0	0	0	0	0	1	0	0	0	0	B/W Pixel Data (400x300):	10h
		0	1	#	#	#	#	#	#	#	#	KPXL[1:8]	00h
		0	1	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	KPXL[n-1:n]	00h
10	Data Stop (DSP)	0	0	0	0	0	1	0	0	0	1		11h
		1	1	#	--	--	--	--	--	--	--		00h
11	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12h
12	Display Start transmission 2 (DTM2, Red Data) (x-byte command)	0	0	0	0	0	1	0	0	1	1	Red Pixel Data (400x300):	13h
		0	1	#	#	#	#	#	#	#	#	RPXL[1:8]	00h
		0	1	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	RPXL[n-1:n]	00h
13	PLL control (PLL)	0	0	0	0	1	1	0	0	0	0		30h
		0	1	--	--	#	#	#	#	#	#	M[2:0], N[2:0]	3Ch
14	Temperature Sensor Calibration (TSC)	0	0	0	1	0	0	0	0	0	0		40h
		1	1	#	#	#	#	#	#	#	#	LM[10:3] / TSR[7:0]	00h
		1	1	#	#	#	--	--	--	--	--	LM[2:0] / -	00h
15	Temperature Sensor Selection (TSE)	0	0	0	1	0	0	0	0	0	1		41h
		0	1	#	--	--	--	#	#	#	#	TSE,TO[3:0]	00h
16	Temperature Sensor Write (TSW)	0	0	0	1	0	0	0	0	1	0		42h
		0	1	#	#	#	#	#	#	#	#	WATTR[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WMSB[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WLSB[7:0]	00h
17	Temperature Sensor Read (TSR)	0	0	0	1	0	0	0	0	1	1		43h
		1	1	#	#	#	#	#	#	#	#	RMSB[7:0]	00h
		1	1	#	#	#	#	#	#	#	#	RLSB[7:0]	00h
18	Vcom and data interval setting	0	0	0	1	0	1	0	0	0	0		50h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
	(CDI)	0	1	#	#	#	#	#	#	#	#	VBD[1:0], DDX[1:0], CDI[3:0]	D7h
19	Lower Power Detection (LPD)	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**1**		**51h**
		1	1	--	--	--	--	--	--	--	#	LPD	01h
20	TCON setting (TCON)	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**		**60h**
		0	1	#	#	#	#	#	#	#	#	S2G[3:0], G2S[3:0]	22h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
21	Resolution setting (TRES)	0	0	0	1	1	0	0	0	0	1	HRES[8:3]	61h
		0	1	--	--	--	--	--	--	--	#		00h
		0	1	#	#	#	#	#	0	0	0		00h
		0	1	--	--	--	--	--	--	--	#	VRES[8:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
22	GSST Setting (GSST)	0	0	0	1	1	0	0	1	0	1	HST[8:3]	65h
		0	1	--	--	--	--	--	--	--	#		00h
		0	1	#	#	#	#	#	0	0	0		00h
		0	1	--	--	--	--	--	--	--	#	VST[8:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
23	Revision (REV)	0	0	0	1	1	1	0	0	0	0		70h
		0	1	#	#	#	#	#	#	#	#	LUT_REV[7:0]	00h
24	Get Status (FLG)	0	0	0	1	1	1	0	0	0	1		71h
		1	1	--	#	#	#	#	#	#	#	PTL_FLAG ,I²C_ERR, I²C_BUSYN, DATA_FLAG, PON, POF, BUSY_N	02h
25	Auto Measurement Vcom	0	0	1	0	0	0	0	0	0	0		80h
		0	1	--	--	#	#	#	#	#	#	AMVT[1:0], XON,AMVS, AMV, AMVE	10h
26	Read Vcom Value(VV)	0	0	1	0	0	0	0	0	0	1		81h
		1	1	--	--	#	#	#	#	#	#	VV[5:0]	00h
27	VCM_DC Setting (VDCS)	0	0	1	0	0	0	0	0	1	0		82h
		0	1	--	--	#	#	#	#	#	#	VDCS[5:0]	00h
28	Partial Window (PTL)	0	0	1	0	0	1	0	0	0	0		90h
		0	1	--	--	--	--	--	--	--	#	HRST[8:3]	00h
		0	1	#	#	#	#	#	0	0	0		00h
		0	1	--	--	--	--	--	--	--	#	HRED[8:3]	00h
		0	1	#	#	#	#	#	1	1	1		07h
		0	1	--	--	--	--	--	--	--	#	VRST[8:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	--	--	--	--	--	--	--	#	VRED[8:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	--	--	--	--	--	--	--	#	PT_SCAN	01h
29	Partial In (PTIN)	0	0	1	0	0	1	0	0	0	1		91h
30	Partial Out (PTOUT)	0	0	1	0	0	1	0	0	1	0		92h
31	Program Mode (PGM)	0	0	1	0	1	0	0	0	0	0		A0h
		0	1	1	0	1	0	0	1	0	1	Check code = A5h	A5h
32	Active Progrmming (APG)	0	0	1	0	1	0	0	0	0	1		A1h
33	Read OTP (ROTP)	0	0	1	0	1	0	0	0	1	0		A2h
		1	1	--	--	--	--	--	--	--	--	Read Dummy	N/A
		1	1	#	#	#	#	#	#	#	#	Data of Address = 000h	N/A
		1	1	:	:	:	:	:	:	:	:	:	N/A
		1	1	#	#	#	#	#	#	#	#	Data of Address = n	N/A
34	Cascade Setting (CCSET)	0	0	1	1	1	0	0	0	0	0		E0h
		0	1	--	--	--	--	--	--	#	#	TSFIX, CCEN	00h
35	Power Saving (PWS)	0	0	1	1	1	0	0	0	1	1		E3h
		0	1	#	#	#	#	#	#	#	#	VCOM_W[3:0], SD_W[3:0]	00h
36	Force Temperauture (TSSET)	0	0	1	1	1	0	0	1	0	1		E5h
		0	1	#	#	#	#	#	#	#	#	TS_SET[7:0]	00h

Note: (1) All other register addresses are invalid or reserved by UltraChip, and should NOT be used.

(2) Any bits shown here as 0 must be written with a 0. All unused bits should also be set to zero. Device malfunction may occur if this is not done.

(3) Commands are processed on the 'stop' condition of the interface.

(4) Registers marked ‘W/R’ can be read, but the contents are written when the SPI command completes – so the contents can be read and altered. The user can subsequently write the register to restore the contents following an SPI read.

COMMAND DESCRIPTION

W/R: 0: Write Cycle / 1: Read Cycle C/D: 0: Command / 1: Data D7-D0: –: Don't Care

(1) PANEL SETTING (PSR) (REGISTER: R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting the panel	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	00h
	0	1	RES1	RES0	REG_EN	BWR	UD	SHL	SHD_N	RST_N	0Fh

RES[1:0]: Display Resolution setting (source x gate)
00b: 400x300 (Default) Active source channels: S0 ~ S399. Active gate channels: G0 ~ G299.
01b: 320x300 Active source channels: S0 ~ S319. Active gate channels: G0 ~ G299.
10b: 320x240 Active source channels: S0 ~ S319. Active gate channels: G0 ~ G239.
11b: 200x300 Active source channels: S0 ~ S199. Active gate channels: G0 ~ G299.

REG_EN: LUT selection
0: LUT from OTP. (Default)
1: LUT from register.

BWR: Black / White / Red
0: Pixel with B/W/Red. (Default)
1: Pixel with B/W.

UD: Gate Scan Direction
0: Scan down. First line to Last line: Gn-1 → Gn-2 → Gn-3 → … → G0
1: Scan up. (Default) First line to Last line: G0 → G1 → G2 → … … . → Gn-1

SHL: Source Shift Direction
0: Shift left. First data to Last data: Sn-1 → Sn-2 → Sn-3 → … → S0
1: Shift right. (Default) First data to Last data: S0 → S1 → S2 → … … . → Sn-1

SHD_N: Booster Switch
0: Booster OFF, register data are kept, and SEG/BG/VCOM are kept 0V or floating.
1: Booster ON (Default)
When SHD_N become LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF, and SD output and VCOM will remain previous condition. SHD_N may have two conditions: 0v or floating.

RST_N: Soft Reset
1: No effect (Default). Booster OFF, Register data are set to their default values, and SEG/BG/VCOM: 0V
When RST_N become LOW, the driver will be reset, all registers will be reset to their default value. All driver functions will be disabled. SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

(2) POWER SETTING (PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Selecting Internal/External Power	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	01h
	0	1	-	-	-	-	-	-	VDS_EN	VDG_EN	03h
	0	1	-	-	-	-	-	VCOM_HV	VGHL_LV[1:0]		00h
	0	1	-	-	VDH[5:0]						26h
	0	1	-	-	VDL[5:0]						26h
	0	1	-	-	VDHR[5:0]						03h

VDS_EN: Source power selection
0 : External source power from VDH/VDL pins
1 : Inetrnal DC/DC function for generating VDH/VDL

VDG_EN: Gate power selection
0 : External gate power from VGH/VGL pins
1 : Internal DC/DC function for generating VGH/VGL

VCOM_HV: VCOM Voltage Level
0 : VCOMH=VDH+VCOMDC, VCOML=VDL+VCOMDC
1 : VCOMH=VGH, VCOML=VGL

VGHL_LV[1:0]: VGH / VGL Voltage Level selection.

VGHL_LV	VGHL Voltage Level
00 (DEFAULT)	VGH=16V, VGL= -16V
01	VGH=15V, VGL= -15V
10	VGH=14V, VGL= -14V
11	VGH=13V, VGL= -13V

VDH[5:0]: Internal VDH power selection for B/W pixel.(**Default value: 100110b**)

VDH	Voltage	VDH	Voltage	VDH	Voltage	VDH	Voltage
000000	2.4 V	001100	4.8 V	011000	7.2 V	100100	9.6 V
000001	2.6 V	001101	5.0 V	011001	7.4 V	100101	9.8 V
000010	2.8 V	001110	5.2 V	011010	7.6 V	**100110**	**10.0V**
000011	3.0 V	001111	5.4 V	011011	7.8 V	100111	10.2 V
000100	3.2 V	010000	5.6 V	011100	8.0 V	101000	10.4 V
000101	3.4 V	010001	5.8 V	011101	8.2V	101001	10.6 V
000110	3.6 V	010010	6.0 V	011110	8.4 V	101010	10.8 V
000111	3.8 V	010011	6.2 V	011111	8.6 V	101011	11.0 V
001000	4.0 V	010100	6.4 V	100000	8.8 V	(others)	11.0 V
001001	4.2 V	010101	6.6 V	100001	9.0 V		
001010	4.4 V	010110	6.8 V	100010	9.2 V		
001011	4.6 V	010111	7.0 V	100011	9.4 V		

VDL[5:0]: Internal VDL power selection for B/W pixel. (**Default value: 100110b**)

VDL	Voltage	VDL	Voltage	VDL	Voltage	VDL	Voltage
000000	-2.4 V	001100	-4.8 V	011000	-7.2 V	100100	-9.6 V
000001	-2.6 V	001101	-5.0 V	011001	-7.4 V	100101	-9.8 V
000010	-2.8 V	001110	-5.2 V	011010	-7.6 V	**100110**	**-10.0V**
000011	-3.0 V	001111	-5.4 V	011011	-7.8 V	100111	-10.2 V
000100	-3.2 V	010000	-5.6 V	011100	-8.0 V	101000	-10.4 V
000101	-3.4 V	010001	-5.8 V	011101	-8.2V	101001	-10.6 V
000110	-3.6 V	010010	-6.0 V	011110	-8.4 V	101010	-10.8 V
000111	-3.8 V	010011	-6.2 V	011111	-8.6 V	101011	-11.0 V
001000	-4.0 V	010100	-6.4 V	100000	-8.8 V	(others)	-11.0 V
001001	-4.2 V	010101	-6.6 V	100001	-9.0 V		
001010	-4.4 V	010110	-6.8 V	100010	-9.2 V		
001011	-4.6 V	010111	-7.0 V	100011	-9.4 V		

VDHR[5:0]: Internal VDHR power selection for Red pixel. (**Default value: 000011b**)

VDHR	Voltage	VDHR	Voltage	VDHR	Voltage	VDHR	Voltage
000000	2.4 V	001100	4.8 V	011000	7.2 V	100100	9.6 V
000001	2.6 V	001101	5.0 V	011001	7.4 V	100101	9.8 V
000010	2.8 V	001110	5.2 V	011010	7.6 V	100110	10.0V
000011	**3.0 V**	001111	5.4 V	011011	7.8 V	100111	10.2 V
000100	3.2 V	010000	5.6 V	011100	8.0 V	101000	10.4 V
000101	3.4 V	010001	5.8 V	011101	8.2V	101001	10.6 V
000110	3.6 V	010010	6.0 V	011110	8.4 V	101010	10.8 V
000111	3.8 V	010011	6.2 V	011111	8.6 V	101011	11.0 V
001000	4.0 V	010100	6.4 V	100000	8.8 V	(others)	11.0 V
001001	4.2 V	010101	6.6 V	100001	9.0 V		
001010	4.4 V	010110	6.8 V	100010	9.2 V		
001011	4.6 V	010111	7.0 V	100011	9.4 V		

(3) POWER OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning OFF the power	0	0	0	0	0	0	0	0	1	0	02h

After the Power Off command, the driver will power off following the Power Off Sequence. This command will turn off charge pump, T-con, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD becomes OFF.

Source Driver output and Vcom will remain as previous condition, which may have 2 conditions: floating.

(4) POWER OFF SEQUENCE SETTING (PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1	1	03h
	0	1	-	-	T_VDS_OFF[1:0]		-	-	-	-	00h

T_VDS_OFF[1:0]: Power OFF Sequence of VDH and VDL.

00b: 1 frame (Default) 01b: 2 frames 10b: 3 frames 11b: 4 frame

(5) POWER ON (PON) (REGISTER: R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning ON the power	0	0	0	0	0	0	0	1	0	0	04h

After the Power ON command, the driver will be powered ON following the Power ON Sequence. Refer to the Power ON Sequence section. In the sequence, temperature sensor will be activated for one time sensing before enabling booster.

(6) POWER ON MEASURE (PMES) (R05H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
	0	0	0	0	0	0	0	1	0	1	05h

This command enables the internal bandgap, which will be cleared by the next POF.

(7) BOOSTER SOFT START (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	06h
	0	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0	17h
	0	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0	17h
	0	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0	17h

BTPHA[7:6]: Soft start period of phase A.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHA[5:3]: Driving strength of phase A

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHA[2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHB[7:6]: Soft start period of phase B.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHB[5:3]: Driving strength of phase B

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHB[2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHC[5:3]: Driving strength of phase C

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHC[2:0]: Minimum OFF time setting of GDR in phase C

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

(8) DEEP SLEEP (DSLP) (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Deep Sleep	0	0	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	07h
	0	1	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	A5h

After this command is transmitted, the chip would enter the deep-sleep mode to save power.

The deep sleep mode would return to standby by hardware reset.

The only one parameter is a check code, the command would be excuted if check code = 0xA5.

(9) DATA START TRANSMISSION 1 (DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	1	0	0	0	0	10h
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8	00h
	0	1	:	:	:	:	:	:	:	:	00h
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	00h

This command starts transmitting data and write them into SRAM. To complete data transmission, command DSP (Data transmission Stop) must be issued. Then the chip will start to send data/VCOM for panel.

In B/W mode, this command writes “OLD” data to SRAM.

In B/W/Red mode, this command writes “B/W” data to SRAM.

In Program mode, this command writes “OTP” data to SRAM for programming.

(10) DATA STOP (DSP) (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Stopping data transmission	0	0	0	0	0	1	0	0	0	1	11h
	1	1	data_flag	-	-	-	-	-	-	-	00h

To stop data transmission, this command must be issued to check the data_flag.

Data_flag: Data flag of receiving user data.

0: Driver didn’t receive all the data.
1: Driver has already received all the one-frame data (DTM1 and DTM2).

After “Data Start” (R10h) or “Data Stop” (R11h) commands and when data_flag=1, the refreshing of panel starts and BUSY_N signal will become “0”.

(11) DISPLAY REFRESH (DRF) (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Refreshing the display	0	0	0	0	0	1	0	0	1	0	12h

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT.

After Display Refresh command, BUSY_N signal will become “0” and the refreshing of panel starts.

(12) DATA START TRANSMISSION 2 (DTM2) (R13H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	1	0	0	0	0	13h
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8	00h
	0	1	:	:	:	:	:	:	:	:	00h
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	00h

This command starts transmitting data and write them into SRAM. To complete data transmission, command DSP (Data transmission Stop) must be issued. Then the chip will start to send data/VCOM for panel.

In B/W mode, this command writes “NEW” data to SRAM.

In B/W/Red mode, this command writes “RED” data to SRAM.

(13) PLL CONTROL (PLL) (R30H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Controlling PLL	0	0	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	30h
	0	1	-	-	M[2:0]			N[2:0]			3Ch

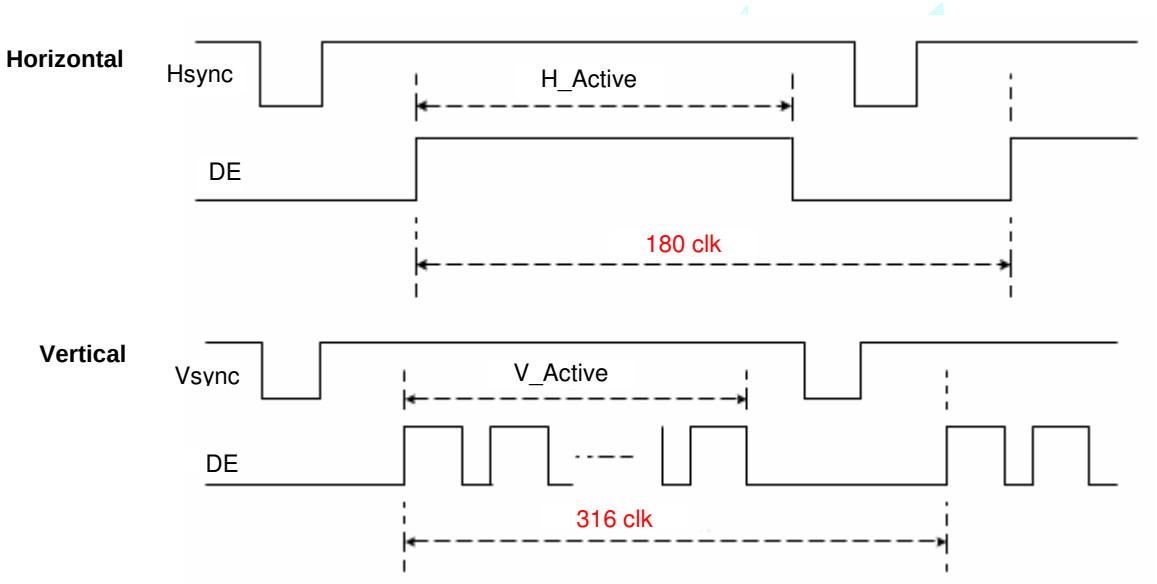
The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

M	N	Frame rate
1	1	29 Hz
	2	14 Hz
	3	10 Hz
	4	7 Hz
	5	6 Hz
	6	5 Hz
	7	4 Hz
2	1	57 Hz
	2	29 Hz
	3	19 Hz
	4	14 Hz
	5	11 Hz
	6	10 Hz
	7	8 Hz

M	N	Frame rate
3	1	86 Hz
	2	43 Hz
	3	29 Hz
	4	21 Hz
	5	17 Hz
	6	14 Hz
	7	12 Hz
4	1	114 Hz
	2	57 Hz
	3	38 Hz
	4	29 Hz
	5	23 Hz
	6	19 Hz
	7	16 Hz

M	N	Frame rate
5	1	150 Hz
	2	72 Hz
	3	48Hz
	4	36 Hz
	5	29 Hz
	6	24 Hz
	7	20 Hz
6	1	171 Hz
	2	86 Hz
	3	57 Hz
	4	43 Hz
	5	34 Hz
	6	29 Hz
	7	24 Hz

M	N	Frame rate
7	1	200 Hz
	2	100 Hz
	3	67 Hz
	4	**50 Hz (default)**
	5	40 Hz
	6	33 Hz
	7	29 Hz



(14) TEMPERATURE SENSOR CALIBRATION (TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Sensing Temperature	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	40h
	1	1	D10/TS7	D9/TS6	D8/TS5	D7/TS4	D6 / TS3	D5 / TS2	D4 / TS1	D3 / TS0	00h
	1	1	D2	D1	D0	-	-	-	-	-	00h

This command reads the temperature sensed by the temperature sensor.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

TS[7:0]/D[10:3]	Temperature (°C)
1110_0111	-25
1110_1000	-24
1110_1001	-23
1110_1010	-22
1110_1011	-21
1110_1100	-20
1110_1101	-19
1110_1110	-18
1110_1111	-17
1111_0000	-16
1111_0001	-15
1111_0010	-14
1111_0011	-13
1111_0100	-12
1111_0101	-11
1111_0110	-10
1111_0111	-9
1111_1000	-8
1111_1001	-7
1111_1010	-6
1111_1011	-5
1111_1100	-4
1111_1101	-3
1111_1110	-2
1111_1111	-1

TS[7:0]/D[10:3]	Temperature(°C)
0000_0000	0
0000_0001	1
0000_0010	2
0000_0011	3
0000_0100	4
0000_0101	5
0000_0110	6
0000_0111	7
0000_1000	8
0000_1001	9
0000_1010	10
0000_1011	11
0000_1100	12
0000_1101	13
0000_1110	14
0000_1111	15
0001_0000	16
0001_0001	17
0001_0010	18
0001_0011	19
0001_0100	20
0001_0101	21
0001_0110	22
0001_0111	23
0001_1000	24

TS[7:0]/D[10:3]	Temperature(°C)
0001_1001	25
0001_1010	26
0001_1011	27
0001_1100	28
0001_1101	29
0001_1110	30
0001_1111	31
0010_0000	32
0010_0001	33
0010_0010	34
0010_0011	35
0010_0100	36
0010_0101	37
0010_0110	38
0010_0111	39
0010_1000	40
0010_1001	41
0010_1010	42
0010_1011	43
0010_1100	44
0010_1101	45
0010_1110	46
0010_1111	47
0011_0000	48
0011_0001	49

(15) TEMPERATURE SENSOR ENABLE (TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enable Temperature Sensor /Offset	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	41h
	0	1	TSE	-	-	-	TO[3:0]				00h

This command selects Internal or External temperature sensor.

TSE: Internal temperature sensor switch

0: Enable (default) 1: Disable; using external sensor.

TO[3:0]: Temperature offset.

TO[3:0]	Calculation
0000 b	+0 (Default)
0001	+1
0010	+2
0011	+3
0100	+4
0101	+5
0110	+6
0111	+7

TO[3:0]	Calculation
1000	-8
1001	-7
1010	-6
1011	-5
1100	-4
1101	-3
1110	-2
1111	-1

(16) TEMPERATURE SENSOR WRITE (TSW) (R42H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Write External Temperature Sensor	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	42h
	0	1	WATTR[7:0]								00h
	0	1	WMSB[7:0]								00h
	0	1	WLSB[7:0]								00h

This command reads the temperature sensed by the temperature sensor.

WATTR: **D[7:6]:** I^2C Write Byte Number
00b : 1 byte (head byte only)
01b : 2 bytes (head byte + pointer)
10b : 3 bytes (head byte + pointer + 1st parameter)
11b : 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

D[5:3]: User-defined address bits (A2, A1, A0)

D[2:0]: Pointer setting

WMSB[7:0]: MSByte of write-data to external temperature sensor

WLSB[7:0]: LSByte of write-data to external temperature sensor

(17) TEMPERATURE SENSOR READ (TSR) (R43H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read External Temperature Sensor	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**	43h
	1	1	RMSB[7:0]								00h
	1	1	RLSB[7:0]								00h

This command reads the temperature sensed by the temperature sensor.

RMSB[7:0]: MSByte read data from external temperature sensor

RLSB[7:0]: LSByte read data from external temperature sensor

(18) VCOM AND DATA INTERVAL SETTING (CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Interval between Vcom and Data	0	0	0	1	0	1	0	0	0	0	50h
	0	1	VBD[1:0]		DDX[1:0]		CDI[3:0]				D7h

This command indicates the interval of Vcom and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

VBD[1:0]: Border data selection

B/W/Red mode (BWR=0)

DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTR
	10	LUTW
	11	LUTB
1 (Default)	00	LUTB
	01	LUTW
	10	LUTR
	11	Floating

B/W mode (BWR=1)

DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTBW (1 → 0)
	10	LUTWB (0 → 1)
	11	Floating
1 (Default)	00	Floating
	01	LUTWB (1 → 0)
	10	LUTBW (0 → 1)
	11	Floating

DDX[1:0]: Data polality.

DDX[1] for RED data, DDX[0] for BW data in the B/W/Red mode.

DDX[0] for B/W mode.

B/W/Red mode (BWR=0)

DDX[1:0]	Data {Red, B/W}	LUT
00	00	LUTW
	01	LUTB
	10	LUTR
	11	LUTR
01 (Default)	00	LUTB
	01	LUTW
	10	LUTR
	11	LUTR

DDX[1:0]	Data {Red, B/W}	LUT
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTB
11	00	LUTR
	01	LUTR
	10	LUTB
	11	LUTW

B/W mode (BWR=1)

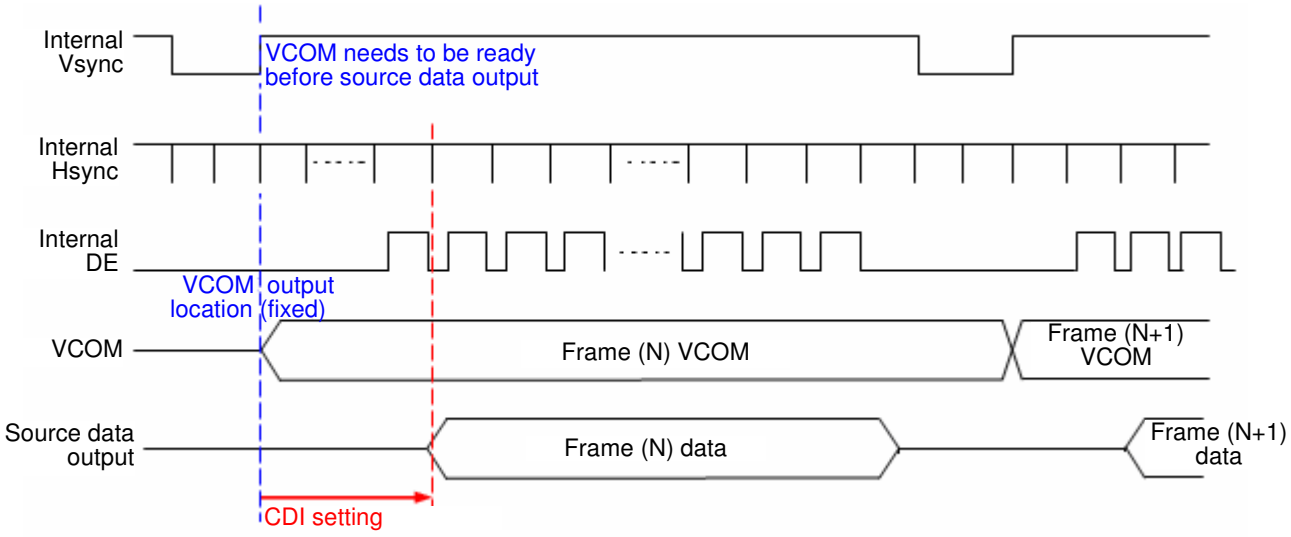
DDX[1:0]	Data {New, Old}	LUT
00	00	LUTWW (0 → 0)
	01	LUTBW (1 → 0)
	10	LUTWB (0 → 1)
	11	LUTBB (1 → 1)
01 (Default)	00	LUTBB (0 → 0)
	01	LUTWB (1 → 0)
	10	LUTBW (0 → 1)
	11	LUTWW (1 → 1)

DDX[1:0]	Data {New}	LUT
10	0	LUTBW (1 → 0)
	1	LUTWB (0 → 1)
11	0	LUTWB (1 → 0)
	1	LUTBW (0 → 1)

CDI[3:0]: Vcom and data interval

CDI[3:0]	Vcom and Data Interval
0000 b	17 hsync
0001	16
0010	15
0011	14
0100	13
0101	12
0110	11
0111	10 (Default)

CDI[3:0]	Vcom and Data Interval
1000	9
1001	8
1010	7
1011	6
1100	5
1101	4
1110	3
1111	2



(19) LOW POWER DETECTION (LPD) (R51H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Detect Low Power	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**1**	51h
	1	1	-	-	-	-	-	-	-	LPD	01h

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Internal Low Power Detection Flag

0: Low power input (V_{DD}<2.5V) **1: Normal status (default)**

(20) TCON SETTING (TCON) (R60H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Non-overlap Period	0	0	0	1	1	0	0	0	0	0	60h
	0	1	S2G[3:0]				G2S[3:0]				22h

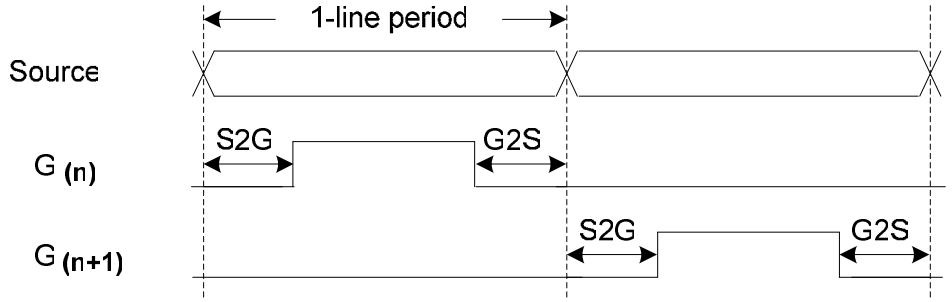
This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period
0000 b	4
0001	8
0010	12 (Default)
0011	16
0100	20
0101	24
0110	28
0111	32

S2G[3:0] or G2S[3:0]	Period
1000 b	36
1001	40
1010	44
1011	48
1100	52
1101	56
1110	60
1111	64

Period = 660 nS.



(21) RESOLUTION SETTING (TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Display Resolution	0	0	0	1	1	0	0	0	0	1	61h
	0	1	-	-	-	-	-	-	-	HRES[8]	00h
	0	1	HRES[7:3]					0	0	0	00h
	0	1	-	-	-	-	-	-	-	VRES[8]	00h
	0	1	VRES[7:0]								00h

This command defines alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).

HRES[8:3]: Horizontal Display Resolution

VRES[8:0]: Vertical Display Resolution

Active channel calculation:

SD: First active source, defined by HST[8:3] (Refer to the following command GSST). (Default: S0).

LAST active source = HRES[8:3]*8 - 1

GD: First active gate, defined by VST[8:0] (Refer to the following command GSST). (Default: G0).

LAST active gate = VRES[8:0] - 1

Example: 128x272

SD: First active source = S0 (default start source), LAST active source = 16*8 – 1 = 127; (HRES[8:3]=16, S127)

GD: First active gate = G0 (default start gate), LAST active gate = 272 - 1= 271; (VRES[8:0] = 272, G271)

(22) GSST SETTING (GSST) (R65H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Gate/Source Start setting	0	0	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**1**	65h
	0	1	--	--	--	--	--	--	--	HST8	00h
	0	1	HST[7:3]					**0**	**0**	**0**	00h
	0	1	--	--	--	--	--	--	--	VST8	00h
	0	1	VST[7:0]								00h

This command defines the Fist Active Gate and First Active Source of active channels.

HST[8:3]: First active source. (Default: S0)

VST[8:0]: First active gate. (Default: G0)

(23) REVISION (REV) (R70H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Chip Revision	0	0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	70h
	1	1	LUT_REV								00h

The LUT_REV is read from OTP address = 0x001.

(24) GET STATUS (FLG) (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read Flags	0	0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**1**	71h
	1	1	**-**	PTL_ flag	I^2C_ERR	I^2C_ BUSYN	data_ flag	PON	POF	BUSY_N	02h

This command reads the IC status.

PTL_FLAG Partial display status (high: partial mode)

I^2C_ERR: I^2C master error status

I^2C_BUSYN: I^2C master busy status (low active)

data_flag: Driver has already received all the one frame data

PON: Power ON status

POF: Power OFF status

BUSY_N: Driver busy status (low active)

(25) AUTO MEASURE VCOM (AMV) (R80H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure Vcom	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	80h
	0	1	**-**	**-**	AMVT[1:0]		XON	AMVS	AMV	AMVE	10h

This command reads the IC status.

AMVT[1:0]: Auto Measure Vcom Time

00b: 3s **01b: 5s (default)**

10b: 8s 11b: 10s

XON: All Gate ON of AMV

0: Gate normally scan during Auto Measure VCOM period. (default)

1: All Gate ON during Auto Measure VCOM period.

AMVS: Source output of AMV

0: Source output 0V during Auto Measure VCOM period. (default)

1: Source output VDHR during Auto Measure VCOM period.

AMV: Analog signal

0: Get Vcom value with the VV command (R81h) (default)

1: Get Vcom value in analog signal. (External analog to digital converter)

AMVE: Auto Measure Vcom Enable (/Disable)

0: No effect

1: Trigger auto Vcom sensing.

(26) VCOM VALUE (VV) (R81H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure Vcom	0	0	1	0	0	0	0	0	0	1	81h
	1	1	-	-	VV[5:0]						00h

This command gets the Vcom value.

VV[5:0]: Vcom Value Output

VV[5:0]	Vcom value
00 0000b	-0.10 V
00 0001b	-0.15 V
00 0010b	-0.20 V
:	:
11 1010b	-3.00 V

(27) VCM_DC SETTING (VDCS) (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set VCM_DC	0	0	1	0	0	0	0	0	1	0	82h
	0	1	-	-	VDCS[5:0]						00h

This command sets VCOM_DC value

VDCS[5:0]: VCOM_DC Setting

VDCS[5:0]	Vcom value
00 0000b	**-0.10 V (default)**
00 0001b	-0.15 V
00 0010b	-0.20 V
:	:
11 1010b	-3.00 V

(28) PARTIAL WINDOW (PTL) (R90H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Partial Window	0	0	1	0	0	0	0	0	1	0	90h
	0	1	-	-	-	-	-	-	-	HRST[8]	00h
	0	1	HRST[7:3]					0	0	0	00h
	0	1	-	-	-	-	-	-	-	HRED[8]	00h
	0	1	HRED[7:3]					1	1	1	07h
	0	1	-	-	-	-	-	-	-	VRST[8]	00h
	0	1	VRST[7:0]								00h
	0	1	-	-	-	-	-	-	-	VRED[8]	00h
	0	1	VRED[7:0]								00h
	0	1	-	-	-	-	-	-	-	PT_SCAN	00h

This command sets partial window.

HRST[8:3]: Horizontal start channel bank. (value 00h~31h)

HRED[8:3]: Horizontal end channel bank. (value 00h~31h). HRED must be greater than HRST.

VRST[8:0]: Vertical start line. (value 000h~12Bh)

VRED[8:0]: Vertical end line. (value 000h~12Bh). VRED must be greater than VRST.

PT_SCAN: 0: Gates scan only inside of the partial window.

1: Gates scan both inside and outside of the partial window. (default)

(29) PARTIAL IN (PTIN) (R91H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial In	0	0	1	0	0	1	0	0	0	1	91h

This command makes the display enter partial mode.

(30) PARTIAL OUT (PTOUT) (R92H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial Out	0	0	1	0	0	1	0	0	1	0	92h

This command makes the display exit partial mode and enter normal mode.

(31) PROGRAM MODE (PGM) (RA0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enter Program Mode	0	0	1	0	1	0	0	0	0	0	A0h
	0	1	1	0	1	0	0	1	0	1	A5h

After this command is issued, the chip would enter the program mode.

After the programming procedure completed, a hardware reset is necessary for leaving program mode.

The only one parameter is a check code, the command would be excuted if check code = 0xA5.

(32) ACTIVE PROGRAM (APG) (RA1H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Active Program OTP	0	0	1	0	1	0	0	0	0	1	A1h

After this command is transmitted, the programming state machine would be activated.

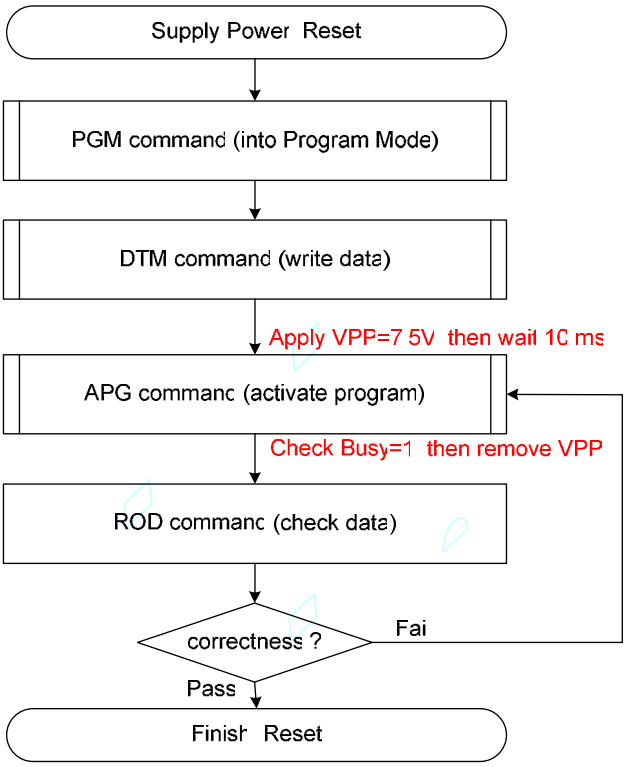
The BUSY flag would fall to 0 until the programming is completed.

(33) READ OTP DATA (ROTP) (RA2H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read OTP data for check	0	0	1	0	1	0	0	0	1	0	A2h
	1	1	Dummy								--
	1	1	The data of address 0x000 in the OTP								--
	1	1	The data of address 0x001 in the OTP								--
	1	1	:								--
	1	1	The data of address (n-1) in the OTP								--
	1	1	The data of address (n) in the OTP								--

The command is used for reading the content of OTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, tha max address = 0xFFF.



The sequence of programming OTP.

(34) CASCADE SETTING (CCSET) (RE0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Cascade Option	0	0	1	1	1	0	0	0	0	0	E0h
	0	1	-	-	-	-	-	-	TSFIX	CCEN	00h

This command is used for cascade.

CCEN: Output clock enable/disable.

0: Output 0V at CL pin. (default)

1: Output clock at CL pin for slave chip.

TSFIX: Let the value of slave's temperuature is same as the master's.

0: Temperature value is defined by internal temperature sensor / external LM75. (default)

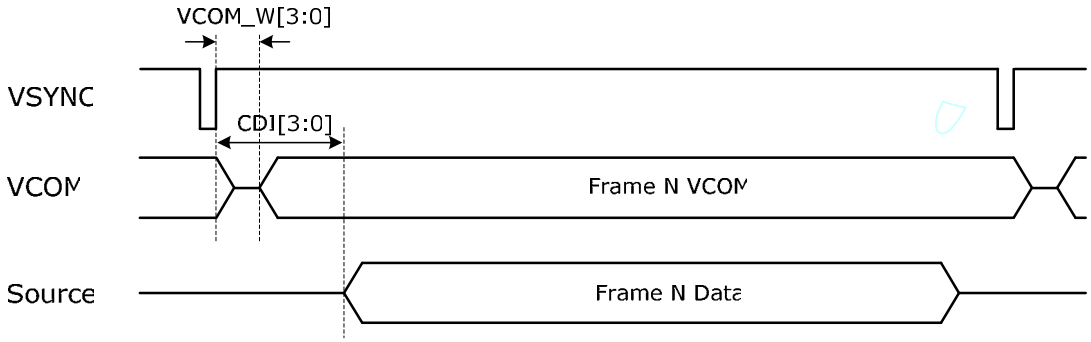
1: Temperature value is defined by TS_SET[7:0] registers.

(35) POWER SAVING (PWS) (RE3H)

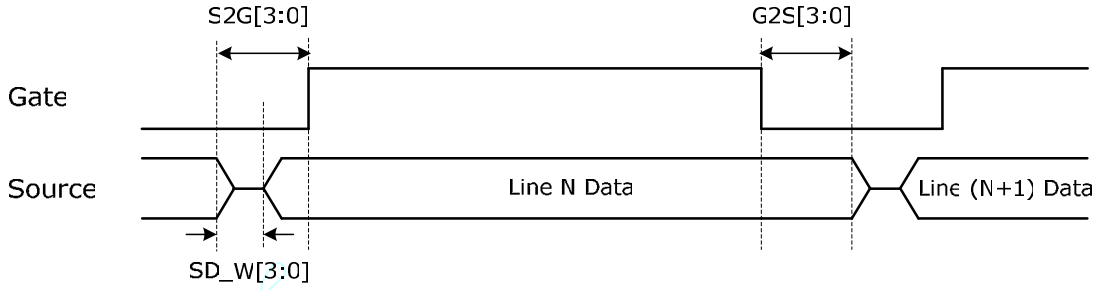
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Power Saving for VCOM & Source	0	0	1	1	1	0	0	0	1	1
	0	1	VCOM_W[3:0]				SD_W[3:0]			

This command is set for saving power during fresh period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W[3:0]: VCOM power saving width (unit = line period)



SD_W[3:0]: Source power saving width (unit = 660nS)



(36) FORCE TEMPERATURE (TSSET) (RE5H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Force Temeperature Value for Cascade	0	0	1	1	1	0	0	1	0	1	E5h
	0	1	TS_SET[7:0]								00h

This command is used for cascade to fix the temperature value of master and slave chip.

COMMAND DEFAULT SETTING

This function can modify the default value of command registers by the OTP content between address 0x020~0x033. The data of address 0x020 is the Enable Key of the function. Changing default value function is used to reduce the initial code length executed by the microcontroller.

ADDRESS (HEX)	D7	D6	D5	D4	D3	D2	D1	D0	Command	Registers	Original
0x020	#	#	#	#	#	#	#	#	Check Code	0xA5 (Enable Key)	0xFF
0x021	#	#	#	#	#	#	--	--	PSR	RES[1:0], REG, KW/R, UD, SHL	0x0F
0x022	--	--	#	#	--	--	--	--	PFS	T_VDS_OF[1:0]	0x00
0x023	#	#	#	#	#	#	#	#	BTST	BT_PHA[7:0]	0x17
0x024	#	#	#	#	#	#	#	#		BT_PHB[7:0]	0x17
0x025	--	--	#	#	#	#	#	#		BT_PHC[5:0]	0x17
0x026	#	--	--	--	#	#	#	#	TSE	TSE, TO[3:0]	0x00
0x027	#	#	#	#	#	#	#	#	CDI	VBD[1:0], DDX[1:0], CDI[3:0]	0xD7
0x028	#	#	#	#	#	#	#	#	TCON	S2G[3:0], G2S[3:0]	0x00
0x029	--	--	--	--	--	--	--	#	TRES	HRES[8:3]	0x00
0x02A	#	#	#	#	#	--	--	--			0x00
0x02B	--	--	--	--	--	--	--	#		VRES[8:0]	0x00
0x02C	#	#	#	#	#	#	#	#			0x00
0x02D	--	--	--	--	--	--	--	#	GSST	HST[8:3]	0x00
0x02E	#	#	#	#	#	--	--	--			0x00
0x02F	--	--	--	--	--	--	--	#		VST[8:0]	0x00
0x030	#	#	#	#	#	#	#	#			0x00
0x031	--	--	--	--	--	--	#	#	CCSET	TSFIX, CCEN	0x00
0x032	#	#	#	#	#	#	#	#	PWS	VCOM_W[3:0], SD_W[3:0]	0x00
0x033	#	#	#	#	#	#	#	#	TSSET	TS_SET[7:0]	0x00

HOST INTERFACES

3-WIRE SPI

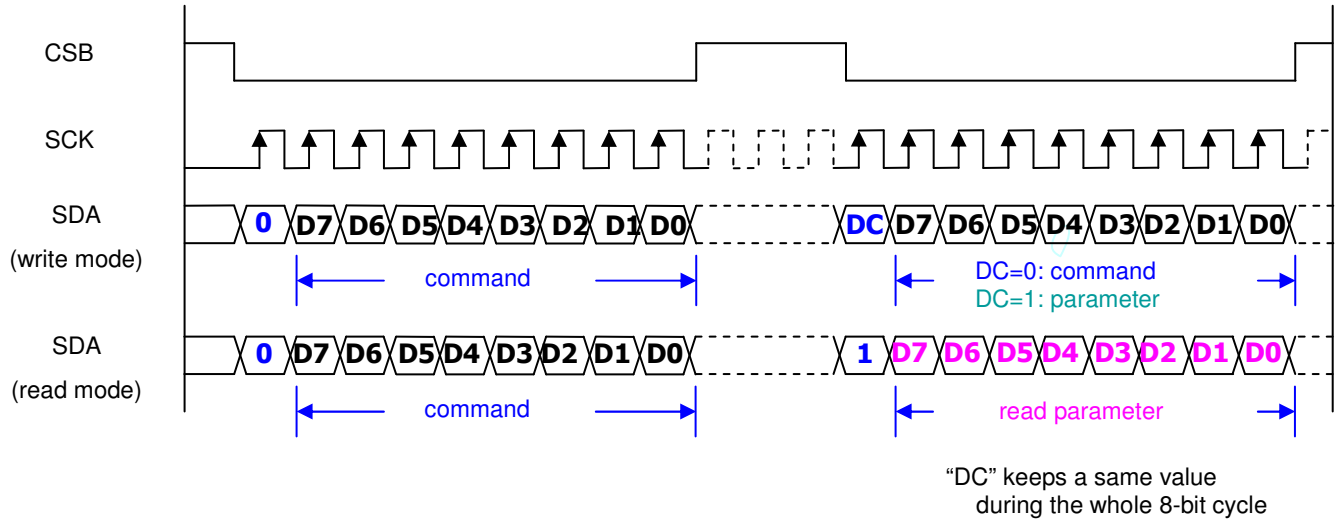


Figure : 3-wire SPI Typical Waveform – BS=1

4-WIRE SPI

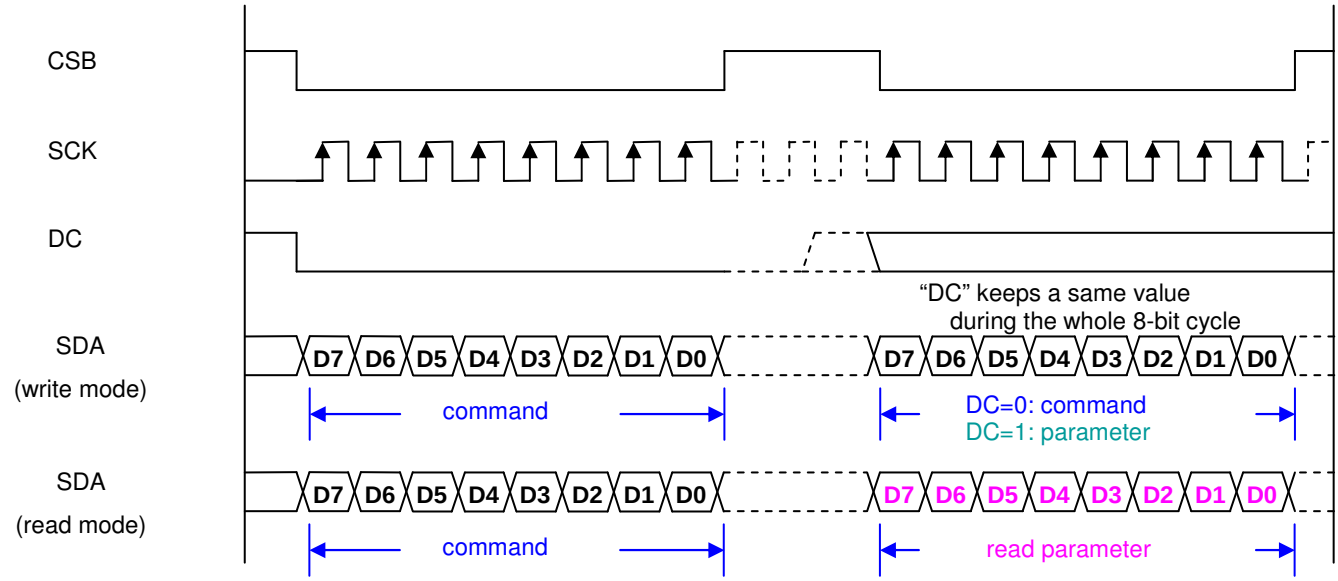
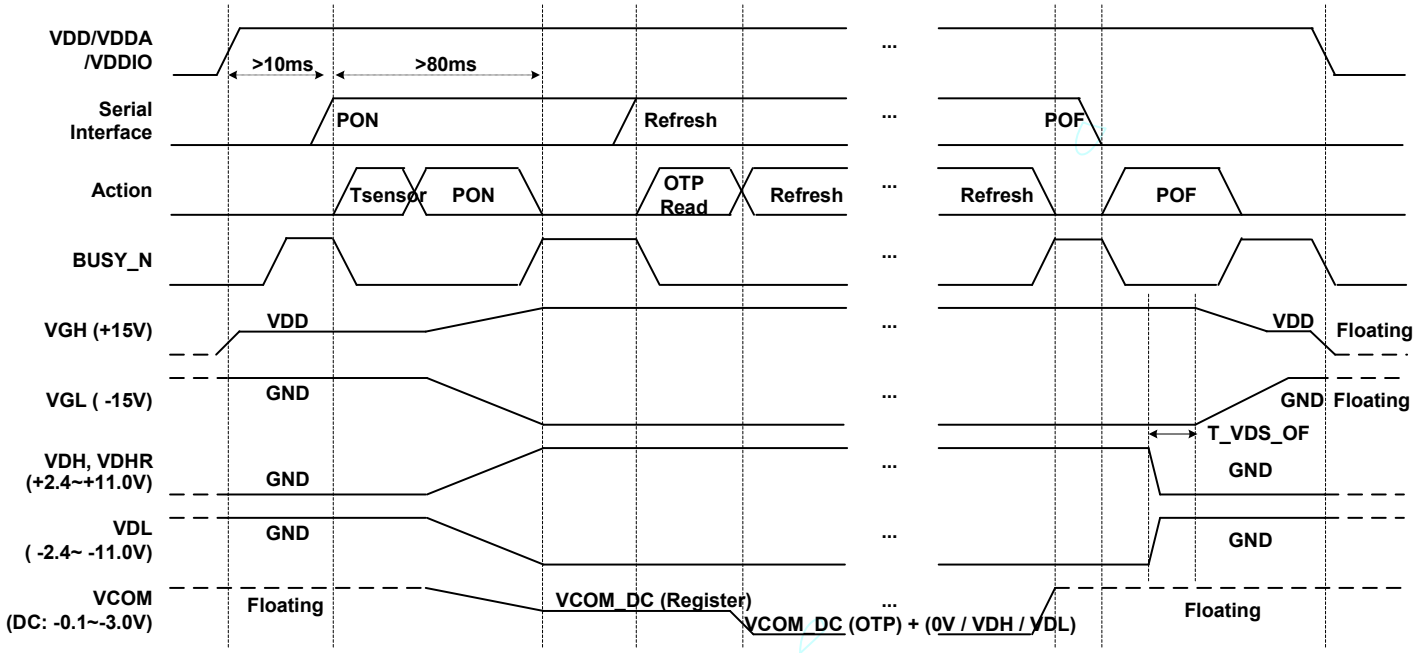


Figure : 4-wire Serial Interface – BS=0

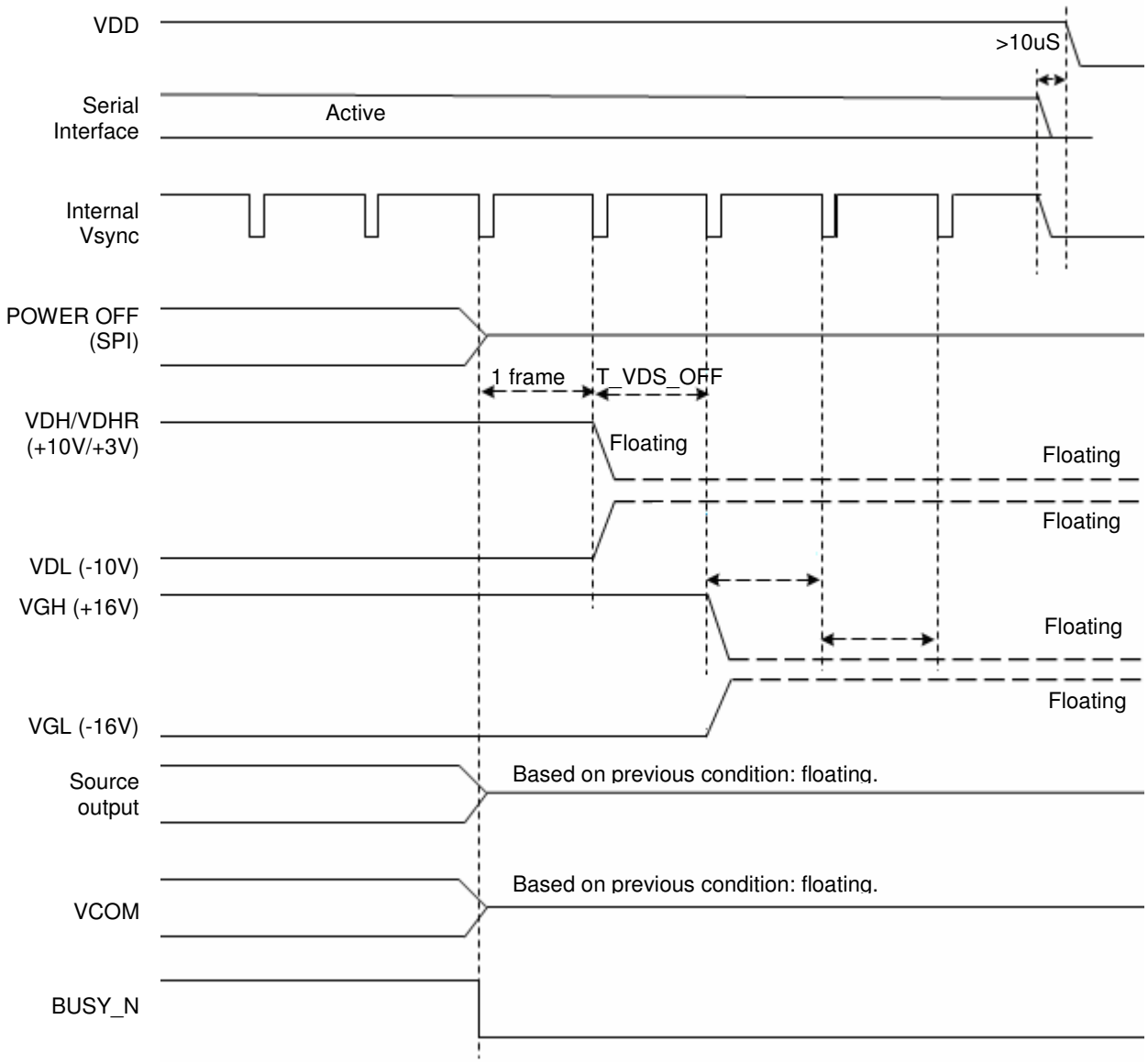
POWER MANAGEMENT

Power ON Sequence

1. Temperature sensor will be activated automatically for one-time sensing before enabling booster.
2. After refreshing display, VCOM will be set to floating automatically.
3. In LUT mode (REG_EN=0), the LUT in OTP will be copied to register automatically after the DSP/DRF command.



Power OFF Sequence



BUSY_N Signal

Commands, except reading command, are restricted by refreshing display (DRF / DSP) as listed in the following table.

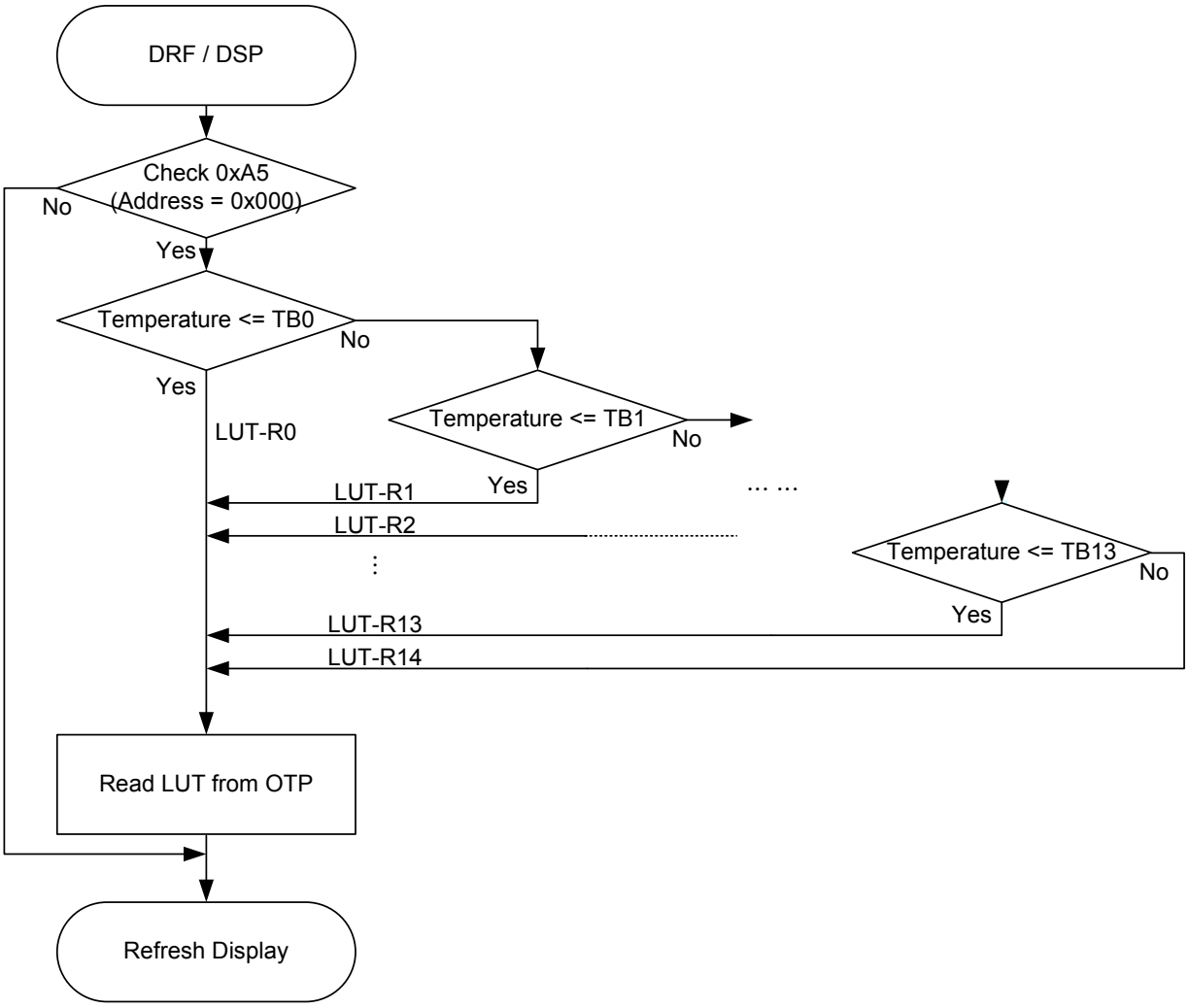
BUSY_N is used to represent the status of internal action.Commands activating internal operation or calculation will cause BUSY_N falling to LOW. After actions compeleted, BUSY_N will return to HIGH.

Command	Refresh Restriction	BUSY_N flag
PSR	X	No action
PWR	X	No action
POF	X	Flag
PFS	X	No action
PON	X	Flag
PMES	X	Flag
BTST	X	No action
DSLP	X	Flag
DTM1	X	No action
DSP	Valid (only read)	Flag
DRF	X	Flag
DTM2	X	No action
LUTC	X	No action
LUTWW/ -	X	No action
LUTWB/LUTW	X	No action
LUTBW/LUTR	X	No action
LUTBB/LUTB	X	No action
PLL	X	No action
TSC	Valid (only read)	Flag
TSE	X	No action
TSW	X	No action
TSR	Valid (only read)	No action
CDI	X	No action
LPD	Valid (only read)	Flag
TCON	X	No action
TRES	X	No action
GSST	X	No action
REV	V	No action
FLG	V	No action
AMV	X	Flag
VV	Valid	No action
VDCS	X	No action
PTL	X	No action
PTIN	X	No action
PTOUT	X	No action
PGM	X	No action
APG	X	Flag
ROTP	X	No action
CCSET	X	No action
TSSET	X	No action
PWS	X	No action

Remark: X: Invalid

TEMPERATURE RANGE

The temperature selection mechanism consists of a less-than-or-equal-to operator and 14 temperature boundary settings (TBx) to determine 15 temperature ranges. The sequence of mechanism is from TB0 to TB13, as shown below. If less than 15 tempeature ranges are used, the last TBx must be set to 0x7F to end the mechanism.



Temperature Selection Mechanism

Example:

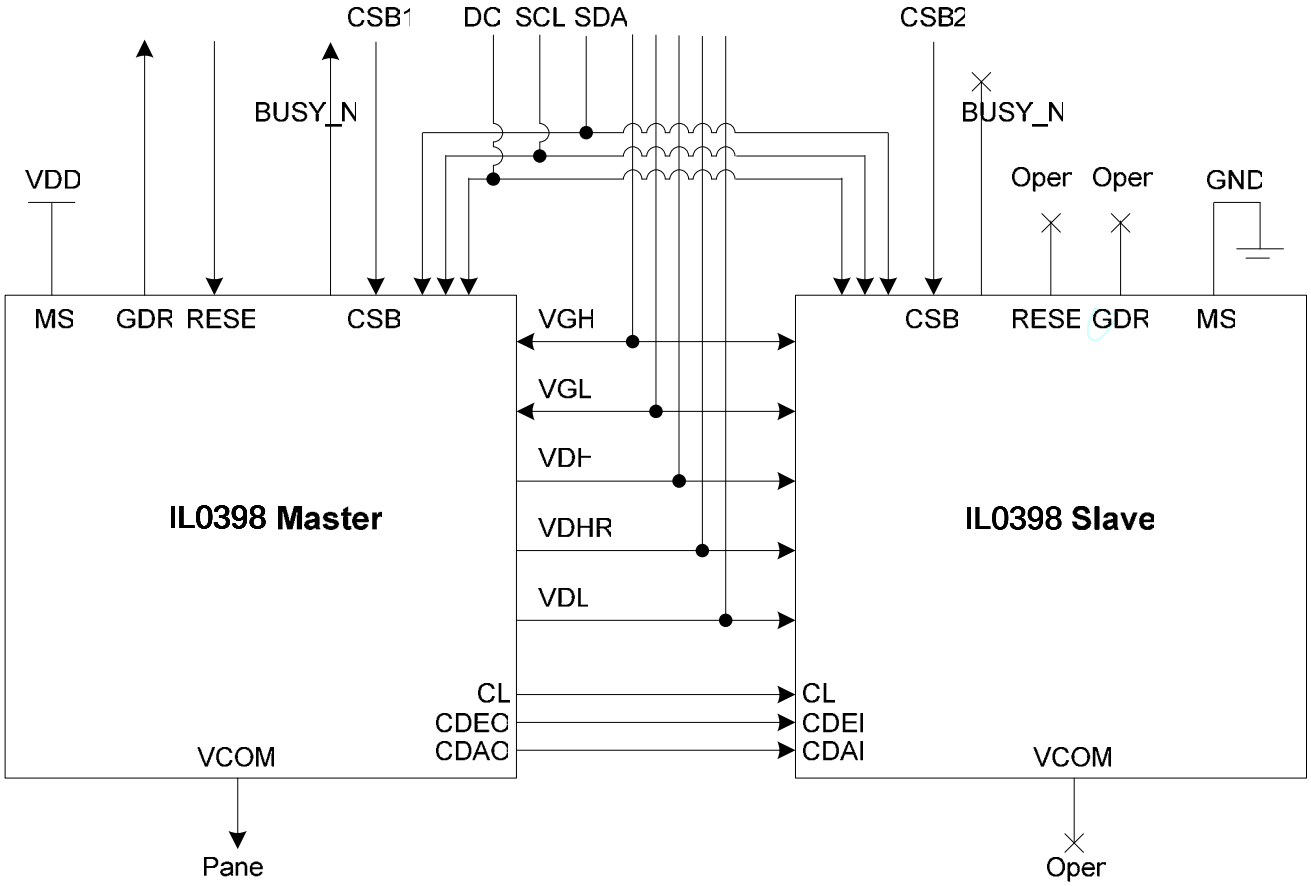
If temperature = -20 °C, LUT-R0 is selected.
If temperature = -10 °C, LUT-R1 is selected.
If temperature = 0 °C, LUT-R2 is selected.
If temperature = 20 °C, LUT-R4 is selected.
If temperature = 40 °C, LUT-R5 is selected.
If temperature > 40 °C, LUT-R6 is selected.

OTP Address	Content	
002h	0xF1	(-15 °C)
003h	0xFB	(-5 °C)
004h	0x00	(0 °C)
005h	0x0A	(10 °C)
006h	0x1E	(30 °C)
007h	**0x7F**	**-**

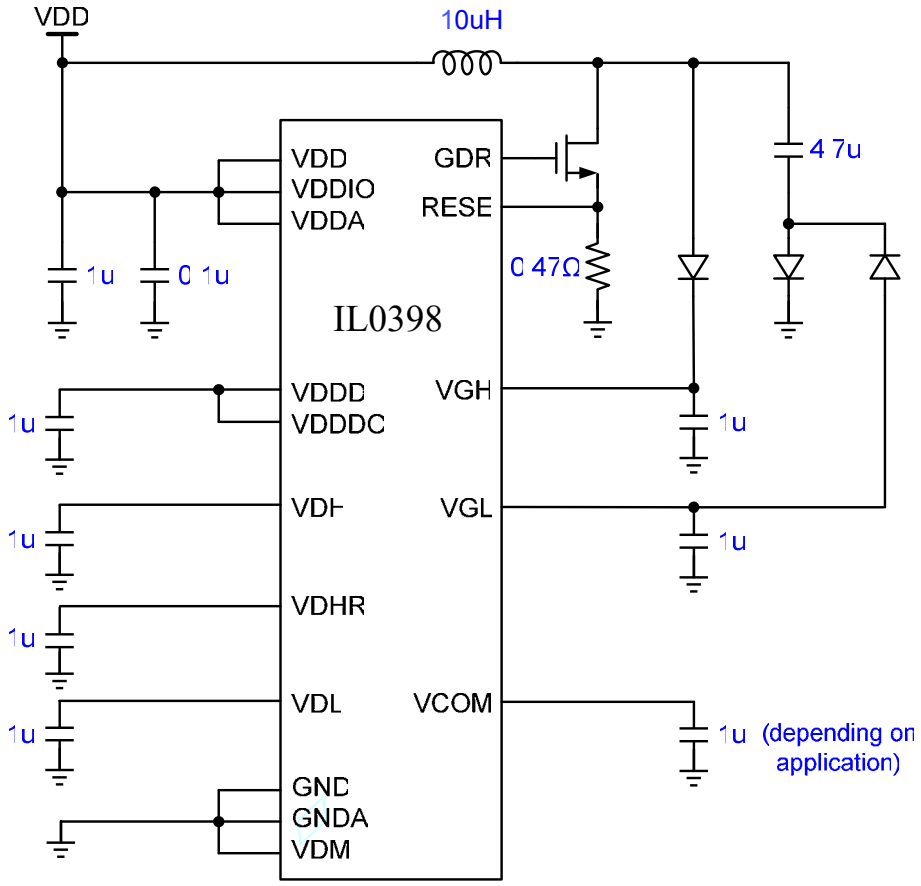
Table 2: Temperature Boundary (TBx) Setting in OTP

OTP Address (Hex)	Content	Description	
002h	TB0	If temperature [TB0, LUT-R0 is selected.	(start address=0x100)
003h	TB1	If temperature [TB1, LUT-R1 is selected.	(start address=0x200)
004h	TB2	If temperature [TB2, LUT-R2 is selected.	(start address=0x300)
005h	TB3	If temperature [TB3, LUT-R3 is selected.	(start address=0x400)
006h	TB4	If temperature [TB4, LUT-R4 is selected.	(start address=0x500)
007h	TB5	If temperature [TB5, LUT-R5 is selected.	(start address=0x600)
008h	TB6	If temperature [TB6, LUT-R6 is selected.	(start address=0x700)
009h	TB7	If temperature [TB7, LUT-R7 is selected.	(start address=0x800)
00Ah	TB8	If temperature [TB8, LUT-R8 is selected.	(start address=0x900)
00Bh	TB9	If temperature [TB9, LUT-R9 is selected.	(start address=0xA00)
00Ch	TB10	If temperature [TB10, LUT-R10 is selected.	(start address=0xB00)
00Dh	TB11	If temperature [TB11, LUT-R11 is selected.	(start address=0xC00)
00Eh	TB12	If temperature [TB12, LUT-R12 is selected.	(start address=0xD00)
00Fh	TB13	If temperature [TB13, LUT-R13 is selected.	(start address=0xE00)
-	-	If temperature > TB13, LUT-R14 is selected.	(start address=0xF00)

CASCADE APPLICATION CIRCUIT



BOOSTER APPLICATION CIRCUIT



Recommended Device

1. Switch MOS NMOS: Vishay Si1304BDL (V_{DS} > 20V, I_D > 500mA, V_{th} < 1.5V, C_{iss} < 200pF)
2. Schottky Diode: OnSemi MBR0530 (V_R > 20V, I_F > 500mA, I_R < 1mA @ V_R=15V, T_a=100°C)

Recommended Resister

Item	Pins	Resistance
Powers	VDD, VDDA, VDDIO, GND, GNDA, VDM	< 10 Ω
Boosters	VGL, VGH, GDR, RESE, FB	< 10 Ω
Regulators	VDH, VDL, VDHR, VCOM, VDDD, VDDDO	< 10 Ω
Logics	MS, BS, CSB, SCL, SDA, GDR, FB, etc.	< 50 Ω
OTP	VPP	< 20 Ω

ABSOLUTE MAXIMUM RATINGS

Signal	Item	Min	Max.	Unit
V_{DD}, V_{DDIO}, V_{DDA}	Logic Supply voltage	-0.3	+6.0	V
V_{PP}	OTP programming voltage	-0.3	+8.0	V
V_I	Digital input range	-0.3	V_{DDIO}+2.4	V
VGH-VGL	Supply range	VGL-0.3	VGH+0.3	V
Source				
VDH	Analog supply voltage – positive	+20		V
VDL	Analog supply voltage -- negative	-20		V
VDHR	Analog supply voltage – positive	+20		V
Gate				
VGH	Analog supply voltage – positive	-0.3	VGL+40	V
VGL	Analog supply voltage -- negative	VGH-40	0.3	V
IVGH	Input rush current for VGH	(TBD)	(TBD)	mA
IVGL	Input rush current for VGL	(TBD)	(TBD)	mA
T_{STG}	Storage temperature range	-55	+125	^oC

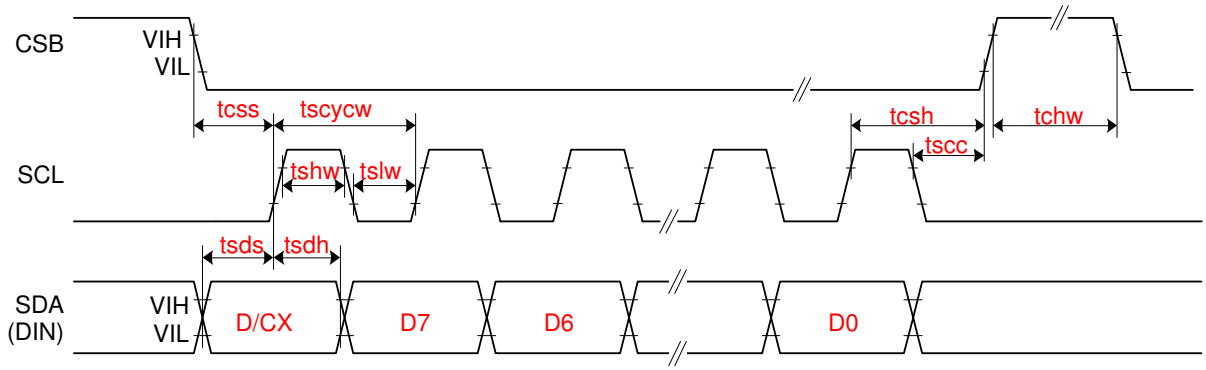
Warning:

If ICs are stressed beyond those listed above “absolute maximum ratings”, they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

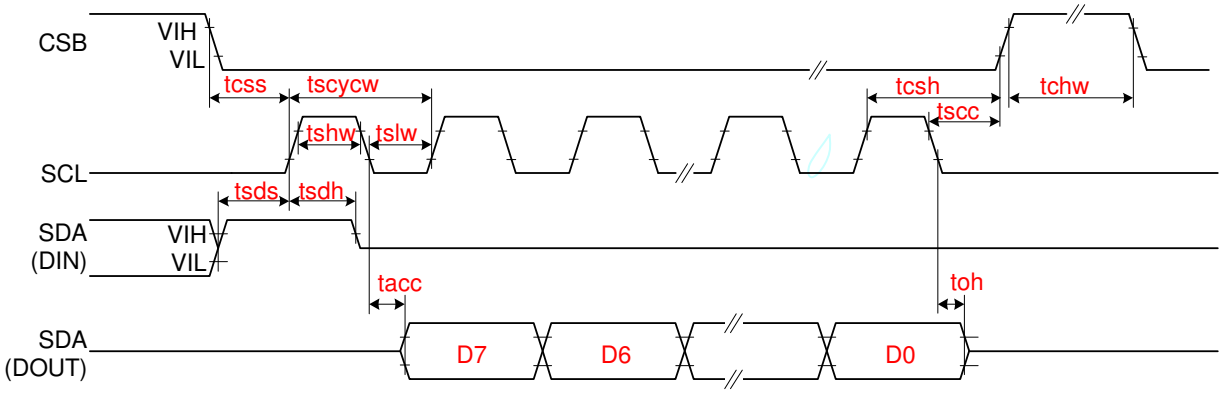
DC CHARACTERISTICS

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
VDDIO	IO supply voltage		2.3	3.3	3.6	V
VDD	Supply voltage		2.3	3.3	3.6	V
VDDA	DCDC driver supply voltage		2.3	3.3	3.6	V
VIL	LOW Level input voltage	Digital input pins	0	--	0.3xVDD	V
VIH	HIGH Level input voltage	Digital input pins	0.7xVDDIO	--	VDDIO	V
VOH	HIGH Level output voltage	Digital output pins, IOH=400uA	VDDIO-0.4	--	--	V
VOL	LOW Level output voltage	Digital output pins, IOL=-400uA	0	--	0.4	V
IIN	Input leakage current	Digital input pins except pull-up, pull-down pin	-1	--	1	uA
RIN	Pull-up/down impedance			200		KΩ
Top	Operating temperature		-30		85	°C
VGH	VGH voltage Range	For gate driver	13		VGL+35	V
dVGH	VGH Supply voltage dev		-400	0	+400	mV
VGL	VGL voltage Range	For gate driver	-16		-13	V
dVGL	VGL Supply voltage dev		-400	0	+400	mV
VGH-VGL	Voltage Range of VGH - VGL		--		35	V
VDH	Supply Voltage	For source driver/VCOM		10		V
dVDH	Supply voltage dev		-300	0	+300	mV
VDL	Supply Voltage	For source driver/VCOM		-10		V
dVDL	Supply voltage dev		-300	0	+300	mV
VDHR	Supply Voltage	For source driver		3.0		V
dVDHR	Supply voltage dev		-300	0	+300	mV
VCOM	Supply Voltage			-1.0		V
dVCOM	Supply voltage dev		-200	0	+200	mV
IVDD	Digital sleep current	VDDD OFF	--	0.1	0.2	uA
	Digital stand-by current	All stopped	--	8.2	10.0	uA
	Digital operating current		--	--	0.1	mA
IVDDIO	IO sleep current	VDDD OFF	--	0.1	0.3	uA
	IO stand-by current	Booster OFF	--	2.5	4.0	uA
	IO operating current	No load	--	--	0.1	mA
IVDDA	DCDC sleep current	VDDD OFF	--	0.3	0.5	uA
	DCDC stand-by current	Booster OFF	--	15.5	20.0	uA
	DCDC operating current	Source output VDH/VDL, Duty=0.5, Period =126us VCOM DC No load	--	--	2.5	mA
		Source output VDH/VDL, Duty=0.5, Period =126us, VCOM DC External cap: 415pF, NMOS=340pF	--	--	15.0	

AC CHARACTERISTICS



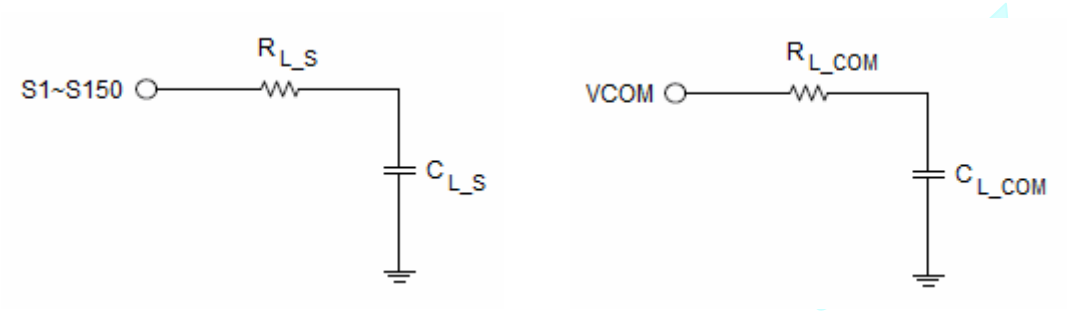
3-wire Serial Interface – Write



3-wire Serial Interface – Read

SYMBOL	SIGNAL			MIN.	TYP.	MAX.	UNIT
SERIAL COMMUNICATION							
tCSS	CSB	Chip select setup time		60			ns
tCSH		Chip select hold time		65			ns
tSCC		Chip select setup time		20			ns
tCHW		Chip select setup time		40			ns
tSCYCW	SCL	Serial clock cycle (Write)		100			ns
tSHW		SCL “H” pulse width (Write)		35			ns
tSLW		SCL “L” pulse width (Write)		35			ns
tSCYCR		Serial clock cycle (Read)		150			ns
tSHR		SCL “H” pulse width (Read)		60			ns
tSLR		SCL “L” pulse width (Read)		60			ns
tSDS	SDA (DIN) (DOUT)	Data setup time		30			ns
tSDH		Data hold time		30			ns
tACC		Access time				10	ns
tOH		Output disable time		15			ns

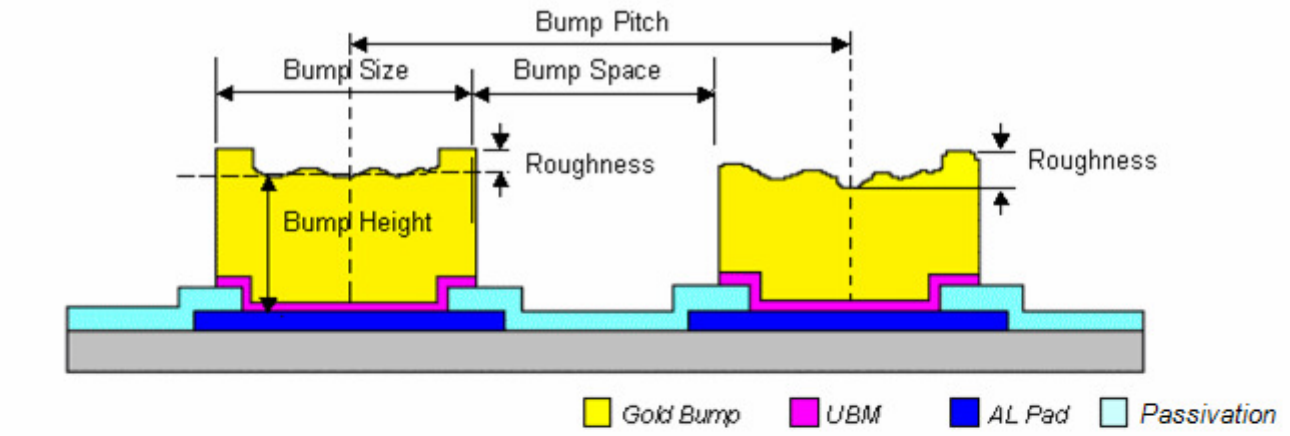
SYMBOL	SIGNAL			MIN.	TYP.	MAX.	UNIT
DRIVER							
trS		Source driver rise time	99% final value		5		us
tFS		Source driver fall time			5		us
trG		Gate driver rise time	99% final value		5		us
tFG		Gate driver fall time			5		us
trCOM		VCOM rise time	99% final value		1		ms
tFCOM		VCOM fall time			1		ms
RC LOADING							
RL_S		Source driver output loading			TBD		K Ω
CL_S					TBD		pf
RL_G		Gate driver output loading			TBD		KΩ
CL_G					TBD		pf
RL_com		VCOM output loading			TBD		Ω
CL_com					TBD		pf



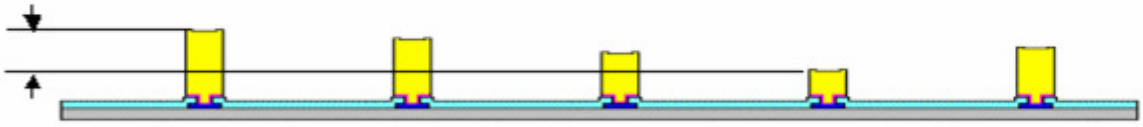
RC Loading

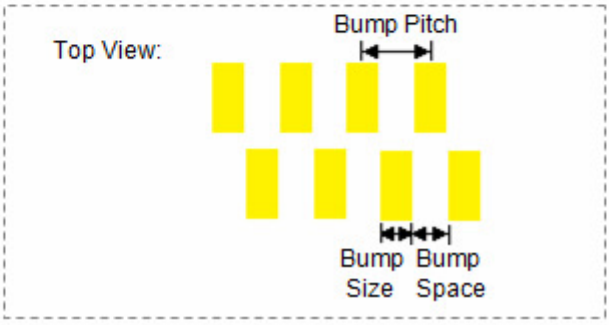
PHYSICAL DIMENSIONS

Die Size:	(13130 µM +/- 40µM) x (1030 µM +/- 40µM)
Die Thickness:	300 µM +/- 20µM
Die TTV:	(D_{MAX} – D_{MIN}) within die ≤ 2µM
Bump Height:	12 µM +/- 3µM
	(H_{MAX} – H_{MIN}) within die ≤ 2µM
Bump Size:	16 µM x 75 µM +/- 3µM
Bump Area:	1200 μM^2
Bump Pitch:	28 µM
Bump Gap:	12 µM +/- 3µM
Hardness:	65 Hv +/- 15Hv
Shear:	/ 5g/Mil^2
Coordinate origin:	Chip center
Pad reference:	Pad center



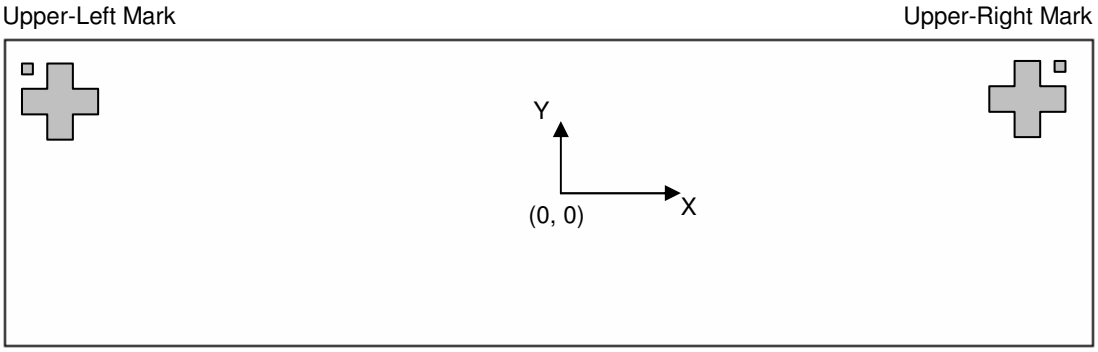
Bump Height Coplanarity within Die



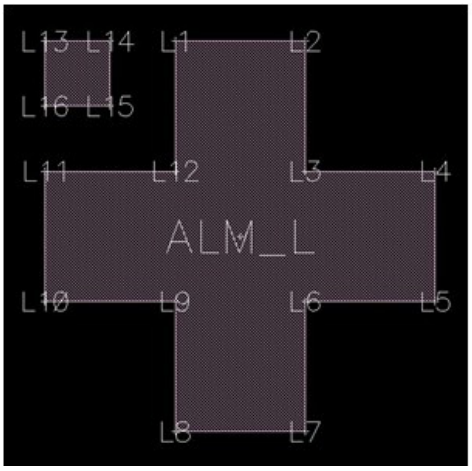


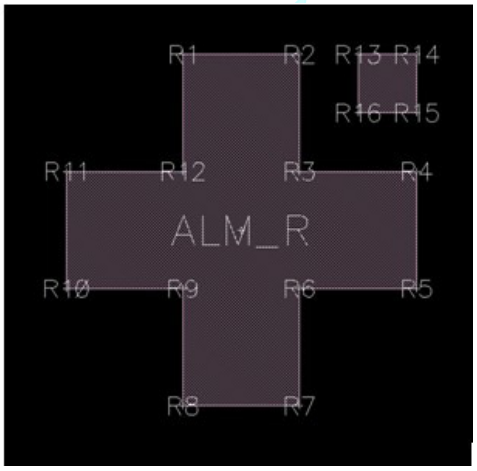
ALIGNMENT MARK INFORMATION

Location:



Shapes and Points:





Point Coordinates:

Point	Upper-Left Mark		Upper-Right Mark	
	X	Y	X	Y
Center	-6465	415	6465	415
1	-6475	445	6455	445
2	-6455	445	6475	445
3	-6455	425	6475	425
4	-6435	425	6495	425
5	-6435	405	6495	405
6	-6455	405	6475	405
7	-6455	385	6475	385
8	-6475	385	6455	385
9	-6475	405	6455	405
10	-6495	405	6435	405
11	-6495	425	6435	425
12	-6475	425	6455	425
13	-6495	445	6485	445
14	-6485	445	6495	445
15	-6485	435	6495	435
16	-6495	435	6485	435

PAD COORDINATES

#	Pad	X	Y	W	H
1	NC	-6440	-423	28	70
2	VCOM	-6394	-423	28	70
3	VCOM	-6348	-423	28	70
4	VCOM	-6302	-423	28	70
5	VCOM	-6256	-423	28	70
6	VCOM	-6210	-423	28	70
7	VCOM	-6164	-423	28	70
8	VCOM	-6118	-423	28	70
9	VCOM	-6072	-423	28	70
10	VDM	-6026	-423	28	70
11	VGL	-5980	-423	28	70
12	VGL	-5934	-423	28	70
13	VGL	-5888	-423	28	70
14	VGL	-5842	-423	28	70
15	VGL	-5796	-423	28	70
16	VGL	-5750	-423	28	70
17	VGL	-5704	-423	28	70
18	VGL	-5658	-423	28	70
19	VGL	-5612	-423	28	70
20	VGL	-5566	-423	28	70
21	VGL	-5520	-423	28	70
22	VGL	-5474	-423	28	70
23	VGL	-5428	-423	28	70
24	VGL	-5382	-423	28	70
25	VGL	-5336	-423	28	70
26	VGL	-5290	-423	28	70
27	GND	-5244	-423	28	70
28	VSL	-5198	-423	28	70
29	VSL	-5152	-423	28	70
30	VSL	-5106	-423	28	70
31	VSL	-5060	-423	28	70
32	VSL	-5014	-423	28	70
33	VSL	-4968	-423	28	70
34	VSL	-4922	-423	28	70
35	VSL	-4876	-423	28	70
36	VSL	-4830	-423	28	70
37	VSL	-4784	-423	28	70
38	GND	-4738	-423	28	70
39	VGH	-4692	-423	28	70
40	VGH	-4646	-423	28	70
41	VGH	-4600	-423	28	70
42	VGH	-4554	-423	28	70
43	VGH	-4508	-423	28	70
44	VGH	-4462	-423	28	70
45	VGH	-4416	-423	28	70
46	VGH	-4370	-423	28	70
47	VGH	-4324	-423	28	70
48	VGH	-4278	-423	28	70
49	VGH	-4232	-423	28	70
50	VGH	-4186	-423	28	70
51	VGH	-4140	-423	28	70
52	VGH	-4094	-423	28	70
53	GND	-4048	-423	28	70
54	VSH	-4002	-423	28	70
55	VSH	-3956	-423	28	70
56	VSH	-3910	-423	28	70
57	VSH	-3864	-423	28	70

#	Pad	X	Y	W	H
58	VSH	-3818	-423	28	70
59	VSH	-3772	-423	28	70
60	VSH	-3726	-423	28	70
61	VSH	-3680	-423	28	70
62	VSH	-3634	-423	28	70
63	VSH	-3588	-423	28	70
64	GND	-3542	-423	28	70
65	VPP	-3496	-423	28	70
66	VPP	-3450	-423	28	70
67	VPP	-3404	-423	28	70
68	VPP	-3358	-423	28	70
69	VPP	-3312	-423	28	70
70	VPP	-3266	-423	28	70
71	VPP	-3220	-423	28	70
72	VDDDI	-3174	-423	28	70
73	VDDDI	-3128	-423	28	70
74	VDDDI	-3082	-423	28	70
75	VDDDI	-3036	-423	28	70
76	VDDDI	-2990	-423	28	70
77	VDDDO	-2944	-423	28	70
78	VDDDO	-2898	-423	28	70
79	VDDDO	-2852	-423	28	70
80	VDDDO	-2806	-423	28	70
81	VDDDO	-2760	-423	28	70
82	VDM	-2714	-423	28	70
83	VDM	-2668	-423	28	70
84	GNDA	-2622	-423	28	70
85	GNDA	-2576	-423	28	70
86	GNDA	-2530	-423	28	70
87	GNDA	-2484	-423	28	70
88	GNDA	-2438	-423	28	70
89	GNDA	-2392	-423	28	70
90	GNDA	-2346	-423	28	70
91	GNDA	-2300	-423	28	70
92	GNDA	-2254	-423	28	70
93	GNDA	-2208	-423	28	70
94	GND	-2162	-423	28	70
95	GND	-2116	-423	28	70
96	GND	-2070	-423	28	70
97	GND	-2024	-423	28	70
98	GND	-1978	-423	28	70
99	GND	-1932	-423	28	70
100	GND	-1886	-423	28	70
101	GND	-1840	-423	28	70
102	GND	-1794	-423	28	70
103	GND	-1748	-423	28	70
104	GND	-1702	-423	28	70
105	GND	-1656	-423	28	70
106	VDDA	-1610	-423	28	70
107	VDDA	-1564	-423	28	70
108	VDDA	-1518	-423	28	70
109	VDDA	-1472	-423	28	70
110	VDDA	-1426	-423	28	70
111	VDDA	-1380	-423	28	70
112	VDDA	-1334	-423	28	70
113	VDDA	-1288	-423	28	70
114	VDDA	-1242	-423	28	70

#	Pad	X	Y	W	H
115	VDDA	-1196	-423	28	70
116	VDD	-1150	-423	28	70
117	VDD	-1104	-423	28	70
118	VDD	-1058	-423	28	70
119	VDD	-1012	-423	28	70
120	VDD	-966	-423	28	70
121	VDD	-920	-423	28	70
122	VDD	-874	-423	28	70
123	DUMMY	-828	-423	28	70
124	DUMMY	-782	-423	28	70
125	DUMMY	-736	-423	28	70
126	DUMMY	-690	-423	28	70
127	DUMMY	-644	-423	28	70
128	DUMMY	-598	-423	28	70
129	DUMMY	-552	-423	28	70
130	DUMMY	-506	-423	28	70
131	DUMMY	-460	-423	28	70
132	DUMMY	-414	-423	28	70
133	DUMMY	-368	-423	28	70
134	DUMMY	-322	-423	28	70
135	DUMMY	-276	-423	28	70
136	DUMMY	-230	-423	28	70
137	DUMMY	-184	-423	28	70
138	DUMMY	-138	-423	28	70
139	DUMMY	-92	-423	28	70
140	DUMMY	-46	-423	28	70
141	DUMMY	0	-423	28	70
142	DUMMY	46	-423	28	70
143	DUMMY	92	-423	28	70
144	DUMMY	138	-423	28	70
145	DUMMY	184	-423	28	70
146	DUMMY	230	-423	28	70
147	DUMMY	276	-423	28	70
148	DUMMY	322	-423	28	70
149	DUMMY	368	-423	28	70
150	DUMMY	414	-423	28	70
151	DUMMY	460	-423	28	70
152	DUMMY	506	-423	28	70
153	DUMMY	552	-423	28	70
154	DUMMY	598	-423	28	70
155	DUMMY	644	-423	28	70
156	DUMMY	690	-423	28	70
157	DUMMY	736	-423	28	70
158	DUMMY	782	-423	28	70
159	DUMMY	828	-423	28	70
160	TEST1	874	-423	28	70
161	GND	920	-423	28	70
162	TEST2	966	-423	28	70
163	DUMMY	1012	-423	28	70
164	DUMMY	1058	-423	28	70
165	VDDIO	1104	-423	28	70
166	VDDIO	1150	-423	28	70
167	VDDIO	1196	-423	28	70
168	VDDIO	1242	-423	28	70
169	DUMMY	1288	-423	28	70
170	TEST3	1334	-423	28	70
171	DUMMY	1380	-423	28	70
172	DUMMY	1426	-423	28	70
173	DUMMY	1472	-423	28	70

#	Pad	X	Y	W	H
174	DUMMY	1518	-423	28	70
175	DUMMY	1564	-423	28	70
176	SDA	1610	-423	28	70
177	SCL	1656	-423	28	70
178	GND	1702	-423	28	70
179	CSB	1748	-423	28	70
180	VDDIO	1794	-423	28	70
181	DUMMY	1840	-423	28	70
182	DUMMY	1886	-423	28	70
183	GND	1932	-423	28	70
184	DC	1978	-423	28	70
185	VDDIO	2024	-423	28	70
186	DUMMY	2070	-423	28	70
187	DUMMY	2116	-423	28	70
188	DUMMY	2162	-423	28	70
189	DUMMY	2208	-423	28	70
190	RST_N	2254	-423	28	70
191	BUSY_N	2300	-423	28	70
192	GND	2346	-423	28	70
193	DUMMY	2392	-423	28	70
194	DUMMY	2438	-423	28	70
195	DUMMY	2484	-423	28	70
196	CDAO	2530	-423	28	70
197	CDEO	2576	-423	28	70
198	CL	2622	-423	28	70
199	CDEI	2668	-423	28	70
200	CDAI	2714	-423	28	70
201	DUMMY	2760	-423	28	70
202	VDDIO	2806	-423	28	70
203	VSYNC	2852	-423	28	70
204	GND	2898	-423	28	70
205	DUMMY	2944	-423	28	70
206	VDDIO	2990	-423	28	70
207	BS	3036	-423	28	70
208	GND	3082	-423	28	70
209	DUMMY	3128	-423	28	70
210	VDDIO	3174	-423	28	70
211	TESTVDD	3220	-423	28	70
212	GND	3266	-423	28	70
213	MS	3312	-423	28	70
214	VDDIO	3358	-423	28	70
215	GND	3404	-423	28	70
216	TSDA	3450	-423	28	70
217	TSDA	3496	-423	28	70
218	TSCL	3542	-423	28	70
219	TSCL	3588	-423	28	70
220	GND	3634	-423	28	70
221	TEST4	3680	-423	28	70
222	TEST5	3726	-423	28	70
223	GND	3772	-423	28	70
224	TEST6	3818	-423	28	70
225	TEST7	3864	-423	28	70
226	GND	3910	-423	28	70
227	TEST8	3956	-423	28	70
228	TEST9	4002	-423	28	70
229	GND	4048	-423	28	70
230	TEST10	4094	-423	28	70
231	TEST11	4140	-423	28	70
232	GND	4186	-423	28	70

#	Pad	X	Y	W	H
233	TEST12	4232	-423	28	70
234	TEST13	4278	-423	28	70
235	DUMMY	4324	-423	28	70
236	DUMMY	4370	-423	28	70
237	DUMMY	4416	-423	28	70
238	DUMMY	4462	-423	28	70
239	DUMMY	4508	-423	28	70
240	DUMMY	4554	-423	28	70
241	DUMMY	4600	-423	28	70
242	DUMMY	4646	-423	28	70
243	VDHR	4692	-423	28	70
244	VDHR	4738	-423	28	70
245	VDHR	4784	-423	28	70
246	VDHR	4830	-423	28	70
247	VDHR	4876	-423	28	70
248	VDHR	4922	-423	28	70
249	VDHR	4968	-423	28	70
250	VDHR	5014	-423	28	70
251	DUMMY	5060	-423	28	70
252	DUMMY	5106	-423	28	70
253	DUMMY	5152	-423	28	70
254	DUMMY	5198	-423	28	70
255	DUMMY	5244	-423	28	70
256	DUMMY	5290	-423	28	70
257	GND	5336	-423	28	70
258	FB	5382	-423	28	70
259	FB	5428	-423	28	70
260	GND	5474	-423	28	70
261	RESE	5520	-423	28	70
262	RESE	5566	-423	28	70
263	GND	5612	-423	28	70
264	GDR	5658	-423	28	70
265	GDR	5704	-423	28	70
266	GDR	5750	-423	28	70
267	GDR	5796	-423	28	70
268	GDR	5842	-423	28	70
269	GDR	5888	-423	28	70
270	GDR	5934	-423	28	70
271	GDR	5980	-423	28	70
272	VDM	6026	-423	28	70
273	VCOM	6072	-423	28	70
274	VCOM	6118	-423	28	70
275	VCOM	6164	-423	28	70
276	VCOM	6210	-423	28	70
277	VCOM	6256	-423	28	70
278	VCOM	6302	-423	28	70
279	VCOM	6348	-423	28	70
280	VCOM	6394	-423	28	70
281	NC	6440	-423	28	70
282	NC	6345	338.5	17	75
283	NC	6324	438.5	17	75
284	NC	6303	338.5	17	75
285	NC	6282	438.5	17	75
286	NC	6261	338.5	17	75
287	GD<0>	6240	438.5	17	75
288	G<0>	6219	338.5	17	75
289	G<2>	6198	438.5	17	75
290	G<4>	6177	338.5	17	75
291	G<6>	6156	438.5	17	75

#	Pad	X	Y	W	H
292	G<8>	6135	338.5	17	75
293	G<10>	6114	438.5	17	75
294	G<12>	6093	338.5	17	75
295	G<14>	6072	438.5	17	75
296	G<16>	6051	338.5	17	75
297	G<18>	6030	438.5	17	75
298	G<20>	6009	338.5	17	75
299	G<22>	5988	438.5	17	75
300	G<24>	5967	338.5	17	75
301	G<26>	5946	438.5	17	75
302	G<28>	5925	338.5	17	75
303	G<30>	5904	438.5	17	75
304	G<32>	5883	338.5	17	75
305	G<34>	5862	438.5	17	75
306	G<36>	5841	338.5	17	75
307	G<38>	5820	438.5	17	75
308	G<40>	5799	338.5	17	75
309	G<42>	5778	438.5	17	75
310	G<44>	5757	338.5	17	75
311	G<46>	5736	438.5	17	75
312	G<48>	5715	338.5	17	75
313	G<50>	5694	438.5	17	75
314	G<52>	5673	338.5	17	75
315	G<54>	5652	438.5	17	75
316	G<56>	5631	338.5	17	75
317	G<58>	5610	438.5	17	75
318	G<60>	5589	338.5	17	75
319	G<62>	5568	438.5	17	75
320	G<64>	5547	338.5	17	75
321	G<66>	5526	438.5	17	75
322	G<68>	5505	338.5	17	75
323	G<70>	5484	438.5	17	75
324	G<72>	5463	338.5	17	75
325	G<74>	5442	438.5	17	75
326	G<76>	5421	338.5	17	75
327	G<78>	5400	438.5	17	75
328	G<80>	5379	338.5	17	75
329	G<82>	5358	438.5	17	75
330	G<84>	5337	338.5	17	75
331	G<86>	5316	438.5	17	75
332	G<88>	5295	338.5	17	75
333	G<90>	5274	438.5	17	75
334	G<92>	5253	338.5	17	75
335	G<94>	5232	438.5	17	75
336	G<96>	5211	338.5	17	75
337	G<98>	5190	438.5	17	75
338	G<100>	5169	338.5	17	75
339	G<102>	5148	438.5	17	75
340	G<104>	5127	338.5	17	75
341	G<106>	5106	438.5	17	75
342	G<108>	5085	338.5	17	75
343	G<110>	5064	438.5	17	75
344	G<112>	5043	338.5	17	75
345	G<114>	5022	438.5	17	75
346	G<116>	5001	338.5	17	75
347	G<118>	4980	438.5	17	75
348	G<120>	4959	338.5	17	75
349	G<122>	4938	438.5	17	75
350	G<124>	4917	338.5	17	75

#	Pad	X	Y	W	H
351	G<126>	4896	438.5	17	75
352	G<128>	4875	338.5	17	75
353	G<130>	4854	438.5	17	75
354	G<132>	4833	338.5	17	75
355	G<134>	4812	438.5	17	75
356	G<136>	4791	338.5	17	75
357	G<138>	4770	438.5	17	75
358	G<140>	4749	338.5	17	75
359	G<142>	4728	438.5	17	75
360	G<144>	4707	338.5	17	75
361	G<146>	4686	438.5	17	75
362	G<148>	4665	338.5	17	75
363	G<150>	4644	438.5	17	75
364	G<152>	4623	338.5	17	75
365	G<154>	4602	438.5	17	75
366	G<156>	4581	338.5	17	75
367	G<158>	4560	438.5	17	75
368	G<160>	4539	338.5	17	75
369	G<162>	4518	438.5	17	75
370	G<164>	4497	338.5	17	75
371	G<166>	4476	438.5	17	75
372	G<168>	4455	338.5	17	75
373	G<170>	4434	438.5	17	75
374	G<172>	4413	338.5	17	75
375	G<174>	4392	438.5	17	75
376	G<176>	4371	338.5	17	75
377	G<178>	4350	438.5	17	75
378	G<180>	4329	338.5	17	75
379	G<182>	4308	438.5	17	75
380	G<184>	4287	338.5	17	75
381	G<186>	4266	438.5	17	75
382	G<188>	4245	338.5	17	75
383	G<190>	4224	438.5	17	75
384	G<192>	4203	338.5	17	75
385	G<194>	4182	438.5	17	75
386	G<196>	4161	338.5	17	75
387	G<198>	4140	438.5	17	75
388	G<200>	4119	338.5	17	75
389	G<202>	4098	438.5	17	75
390	G<204>	4077	338.5	17	75
391	G<206>	4056	438.5	17	75
392	G<208>	4035	338.5	17	75
393	G<210>	4014	438.5	17	75
394	G<212>	3993	338.5	17	75
395	G<214>	3972	438.5	17	75
396	G<216>	3951	338.5	17	75
397	G<218>	3930	438.5	17	75
398	G<220>	3909	338.5	17	75
399	G<222>	3888	438.5	17	75
400	G<224>	3867	338.5	17	75
401	G<226>	3846	438.5	17	75
402	G<228>	3825	338.5	17	75
403	G<230>	3804	438.5	17	75
404	G<232>	3783	338.5	17	75
405	G<234>	3762	438.5	17	75
406	G<236>	3741	338.5	17	75
407	G<238>	3720	438.5	17	75
408	G<240>	3699	338.5	17	75
409	G<242>	3678	438.5	17	75

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413	G<250>	3594	438.5	17	75
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415	G<254>	3552	438.5	17	75
416	G<256>	3531	338.5	17	75
417	G<258>	3510	438.5	17	75
418	G<260>	3489	338.5	17	75
419	G<262>	3468	438.5	17	75
420	G<264>	3447	338.5	17	75
421	G<266>	3426	438.5	17	75
422	G<268>	3405	338.5	17	75
423	G<270>	3384	438.5	17	75
424	G<272>	3363	338.5	17	75
425	G<274>	3342	438.5	17	75
426	G<276>	3321	338.5	17	75
427	G<278>	3300	438.5	17	75
428	G<280>	3279	338.5	17	75
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430	G<284>	3237	338.5	17	75
431	G<286>	3216	438.5	17	75
432	G<288>	3195	338.5	17	75
433	G<290>	3174	438.5	17	75
434	G<292>	3153	338.5	17	75
435	G<294>	3132	438.5	17	75
436	G<296>	3111	338.5	17	75
437	G<298>	3090	438.5	17	75
438	GD<2>	3069	338.5	17	75
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441	NC	3006	438.5	17	75
442	NC	2985	338.5	17	75
443	NC	2964	438.5	17	75
444	NC	2943	338.5	17	75
445	NC	2835	438.5	16	75
446	NC	2821	338.5	16	75
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450	S<2>	2765	338.5	16	75
451	S<3>	2751	438.5	16	75
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458	S<10>	2653	338.5	16	75
459	S<11>	2639	438.5	16	75
460	S<12>	2625	338.5	16	75
461	S<13>	2611	438.5	16	75
462	S<14>	2597	338.5	16	75
463	S<15>	2583	438.5	16	75
464	S<16>	2569	338.5	16	75
465	S<17>	2555	438.5	16	75
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467	S<19>	2527	438.5	16	75
468	S<20>	2513	338.5	16	75

#	Pad	X	Y	W	H
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471	S<23>	2471	438.5	16	75
472	S<24>	2457	338.5	16	75
473	S<25>	2443	438.5	16	75
474	S<26>	2429	338.5	16	75
475	S<27>	2415	438.5	16	75
476	S<28>	2401	338.5	16	75
477	S<29>	2387	438.5	16	75
478	S<30>	2373	338.5	16	75
479	S<31>	2359	438.5	16	75
480	S<32>	2345	338.5	16	75
481	S<33>	2331	438.5	16	75
482	S<34>	2317	338.5	16	75
483	S<35>	2303	438.5	16	75
484	S<36>	2289	338.5	16	75
485	S<37>	2275	438.5	16	75
486	S<38>	2261	338.5	16	75
487	S<39>	2247	438.5	16	75
488	S<40>	2233	338.5	16	75
489	S<41>	2219	438.5	16	75
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491	S<43>	2191	438.5	16	75
492	S<44>	2177	338.5	16	75
493	S<45>	2163	438.5	16	75
494	S<46>	2149	338.5	16	75
495	S<47>	2135	438.5	16	75
496	S<48>	2121	338.5	16	75
497	S<49>	2107	438.5	16	75
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501	S<53>	2051	438.5	16	75
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503	S<55>	2023	438.5	16	75
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506	S<58>	1981	338.5	16	75
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519	S<71>	1799	438.5	16	75
520	S<72>	1785	338.5	16	75
521	S<73>	1771	438.5	16	75
522	S<74>	1757	338.5	16	75
523	S<75>	1743	438.5	16	75
524	S<76>	1729	338.5	16	75
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526	S<78>	1701	338.5	16	75
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532	S<84>	1617	338.5	16	75
533	S<85>	1603	438.5	16	75
534	S<86>	1589	338.5	16	75
535	S<87>	1575	438.5	16	75
536	S<88>	1561	338.5	16	75
537	S<89>	1547	438.5	16	75
538	S<90>	1533	338.5	16	75
539	S<91>	1519	438.5	16	75
540	S<92>	1505	338.5	16	75
541	S<93>	1491	438.5	16	75
542	S<94>	1477	338.5	16	75
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546	S<98>	1421	338.5	16	75
547	S<99>	1407	438.5	16	75
548	S<100>	1393	338.5	16	75
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551	S<103>	1351	438.5	16	75
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558	S<110>	1253	338.5	16	75
559	S<111>	1239	438.5	16	75
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562	S<114>	1197	338.5	16	75
563	S<115>	1183	438.5	16	75
564	S<116>	1169	338.5	16	75
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571	S<123>	1071	438.5	16	75
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573	S<125>	1043	438.5	16	75
574	S<126>	1029	338.5	16	75
575	S<127>	1015	438.5	16	75
576	S<128>	1001	338.5	16	75
577	S<129>	987	438.5	16	75
578	S<130>	973	338.5	16	75
579	S<131>	959	438.5	16	75
580	S<132>	945	338.5	16	75
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582	S<134>	917	338.5	16	75
583	S<135>	903	438.5	16	75
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585	S<137>	875	438.5	16	75
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591	S<143>	791	438.5	16	75
592	S<144>	777	338.5	16	75
593	S<145>	763	438.5	16	75
594	S<146>	749	338.5	16	75
595	S<147>	735	438.5	16	75
596	S<148>	721	338.5	16	75
597	S<149>	707	438.5	16	75
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599	S<151>	679	438.5	16	75
600	S<152>	665	338.5	16	75
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602	S<154>	637	338.5	16	75
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606	S<158>	581	338.5	16	75
607	S<159>	567	438.5	16	75
608	S<160>	553	338.5	16	75
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610	S<162>	525	338.5	16	75
611	S<163>	511	438.5	16	75
612	S<164>	497	338.5	16	75
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615	S<167>	455	438.5	16	75
616	S<168>	441	338.5	16	75
617	S<169>	427	438.5	16	75
618	S<170>	413	338.5	16	75
619	S<171>	399	438.5	16	75
620	S<172>	385	338.5	16	75
621	S<173>	371	438.5	16	75
622	S<174>	357	338.5	16	75
623	S<175>	343	438.5	16	75
624	S<176>	329	338.5	16	75
625	S<177>	315	438.5	16	75
626	S<178>	301	338.5	16	75
627	S<179>	287	438.5	16	75
628	S<180>	273	338.5	16	75
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630	S<182>	245	338.5	16	75
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632	S<184>	217	338.5	16	75
633	S<185>	203	438.5	16	75
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635	S<187>	175	438.5	16	75
636	S<188>	161	338.5	16	75
637	S<189>	147	438.5	16	75
638	S<190>	133	338.5	16	75
639	S<191>	119	438.5	16	75
640	S<192>	105	338.5	16	75
641	S<193>	91	438.5	16	75
642	S<194>	77	338.5	16	75
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644	S<196>	49	338.5	16	75
645	S<197>	35	438.5	16	75

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649	S<201>	-21	438.5	16	75
650	S<202>	-35	338.5	16	75
651	S<203>	-49	438.5	16	75
652	S<204>	-63	338.5	16	75
653	S<205>	-77	438.5	16	75
654	S<206>	-91	338.5	16	75
655	S<207>	-105	438.5	16	75
656	S<208>	-119	338.5	16	75
657	S<209>	-133	438.5	16	75
658	S<210>	-147	338.5	16	75
659	S<211>	-161	438.5	16	75
660	S<212>	-175	338.5	16	75
661	S<213>	-189	438.5	16	75
662	S<214>	-203	338.5	16	75
663	S<215>	-217	438.5	16	75
664	S<216>	-231	338.5	16	75
665	S<217>	-245	438.5	16	75
666	S<218>	-259	338.5	16	75
667	S<219>	-273	438.5	16	75
668	S<220>	-287	338.5	16	75
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670	S<222>	-315	338.5	16	75
671	S<223>	-329	438.5	16	75
672	S<224>	-343	338.5	16	75
673	S<225>	-357	438.5	16	75
674	S<226>	-371	338.5	16	75
675	S<227>	-385	438.5	16	75
676	S<228>	-399	338.5	16	75
677	S<229>	-413	438.5	16	75
678	S<230>	-427	338.5	16	75
679	S<231>	-441	438.5	16	75
680	S<232>	-455	338.5	16	75
681	S<233>	-469	438.5	16	75
682	S<234>	-483	338.5	16	75
683	S<235>	-497	438.5	16	75
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685	S<237>	-525	438.5	16	75
686	S<238>	-539	338.5	16	75
687	S<239>	-553	438.5	16	75
688	S<240>	-567	338.5	16	75
689	S<241>	-581	438.5	16	75
690	S<242>	-595	338.5	16	75
691	S<243>	-609	438.5	16	75
692	S<244>	-623	338.5	16	75
693	S<245>	-637	438.5	16	75
694	S<246>	-651	338.5	16	75
695	S<247>	-665	438.5	16	75
696	S<248>	-679	338.5	16	75
697	S<249>	-693	438.5	16	75
698	S<250>	-707	338.5	16	75
699	S<251>	-721	438.5	16	75
700	S<252>	-735	338.5	16	75
701	S<253>	-749	438.5	16	75
702	S<254>	-763	338.5	16	75
703	S<255>	-777	438.5	16	75
704	S<256>	-791	338.5	16	75

#	Pad	X	Y	W	H
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707	S<259>	-833	438.5	16	75
708	S<260>	-847	338.5	16	75
709	S<261>	-861	438.5	16	75
710	S<262>	-875	338.5	16	75
711	S<263>	-889	438.5	16	75
712	S<264>	-903	338.5	16	75
713	S<265>	-917	438.5	16	75
714	S<266>	-931	338.5	16	75
715	S<267>	-945	438.5	16	75
716	S<268>	-959	338.5	16	75
717	S<269>	-973	438.5	16	75
718	S<270>	-987	338.5	16	75
719	S<271>	-1001	438.5	16	75
720	S<272>	-1015	338.5	16	75
721	S<273>	-1029	438.5	16	75
722	S<274>	-1043	338.5	16	75
723	S<275>	-1057	438.5	16	75
724	S<276>	-1071	338.5	16	75
725	S<277>	-1085	438.5	16	75
726	S<278>	-1099	338.5	16	75
727	S<279>	-1113	438.5	16	75
728	S<280>	-1127	338.5	16	75
729	S<281>	-1141	438.5	16	75
730	S<282>	-1155	338.5	16	75
731	S<283>	-1169	438.5	16	75
732	S<284>	-1183	338.5	16	75
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734	S<286>	-1211	338.5	16	75
735	S<287>	-1225	438.5	16	75
736	S<288>	-1239	338.5	16	75
737	S<289>	-1253	438.5	16	75
738	S<290>	-1267	338.5	16	75
739	S<291>	-1281	438.5	16	75
740	S<292>	-1295	338.5	16	75
741	S<293>	-1309	438.5	16	75
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749	S<301>	-1421	438.5	16	75
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752	S<304>	-1463	338.5	16	75
753	S<305>	-1477	438.5	16	75
754	S<306>	-1491	338.5	16	75
755	S<307>	-1505	438.5	16	75
756	S<308>	-1519	338.5	16	75
757	S<309>	-1533	438.5	16	75
758	S<310>	-1547	338.5	16	75
759	S<311>	-1561	438.5	16	75
760	S<312>	-1575	338.5	16	75
761	S<313>	-1589	438.5	16	75
762	S<314>	-1603	338.5	16	75
763	S<315>	-1617	438.5	16	75

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767	S<319>	-1673	438.5	16	75
768	S<320>	-1687	338.5	16	75
769	S<321>	-1701	438.5	16	75
770	S<322>	-1715	338.5	16	75
771	S<323>	-1729	438.5	16	75
772	S<324>	-1743	338.5	16	75
773	S<325>	-1757	438.5	16	75
774	S<326>	-1771	338.5	16	75
775	S<327>	-1785	438.5	16	75
776	S<328>	-1799	338.5	16	75
777	S<329>	-1813	438.5	16	75
778	S<330>	-1827	338.5	16	75
779	S<331>	-1841	438.5	16	75
780	S<332>	-1855	338.5	16	75
781	S<333>	-1869	438.5	16	75
782	S<334>	-1883	338.5	16	75
783	S<335>	-1897	438.5	16	75
784	S<336>	-1911	338.5	16	75
785	S<337>	-1925	438.5	16	75
786	S<338>	-1939	338.5	16	75
787	S<339>	-1953	438.5	16	75
788	S<340>	-1967	338.5	16	75
789	S<341>	-1981	438.5	16	75
790	S<342>	-1995	338.5	16	75
791	S<343>	-2009	438.5	16	75
792	S<344>	-2023	338.5	16	75
793	S<345>	-2037	438.5	16	75
794	S<346>	-2051	338.5	16	75
795	S<347>	-2065	438.5	16	75
796	S<348>	-2079	338.5	16	75
797	S<349>	-2093	438.5	16	75
798	S<350>	-2107	338.5	16	75
799	S<351>	-2121	438.5	16	75
800	S<352>	-2135	338.5	16	75
801	S<353>	-2149	438.5	16	75
802	S<354>	-2163	338.5	16	75
803	S<355>	-2177	438.5	16	75
804	S<356>	-2191	338.5	16	75
805	S<357>	-2205	438.5	16	75
806	S<358>	-2219	338.5	16	75
807	S<359>	-2233	438.5	16	75
808	S<360>	-2247	338.5	16	75
809	S<361>	-2261	438.5	16	75
810	S<362>	-2275	338.5	16	75
811	S<363>	-2289	438.5	16	75
812	S<364>	-2303	338.5	16	75
813	S<365>	-2317	438.5	16	75
814	S<366>	-2331	338.5	16	75
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816	S<368>	-2359	338.5	16	75
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820	S<372>	-2415	338.5	16	75
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#	Pad	X	Y	W	H
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824	S<376>	-2471	338.5	16	75
825	S<377>	-2485	438.5	16	75
826	S<378>	-2499	338.5	16	75
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829	S<381>	-2541	438.5	16	75
830	S<382>	-2555	338.5	16	75
831	S<383>	-2569	438.5	16	75
832	S<384>	-2583	338.5	16	75
833	S<385>	-2597	438.5	16	75
834	S<386>	-2611	338.5	16	75
835	S<387>	-2625	438.5	16	75
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837	S<389>	-2653	438.5	16	75
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845	S<397>	-2765	438.5	16	75
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848	VBD<2>	-2807	338.5	16	75
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851	NC	-2943	438.5	17	75
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854	NC	-3006	338.5	17	75
855	NC	-3027	438.5	17	75
856	NC	-3048	338.5	17	75
857	GD<3>	-3069	438.5	17	75
858	G<299>	-3090	338.5	17	75
859	G<297>	-3111	438.5	17	75
860	G<295>	-3132	338.5	17	75
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862	G<291>	-3174	338.5	17	75
863	G<289>	-3195	438.5	17	75
864	G<287>	-3216	338.5	17	75
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870	G<275>	-3342	338.5	17	75
871	G<273>	-3363	438.5	17	75
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874	G<267>	-3426	338.5	17	75
875	G<265>	-3447	438.5	17	75
876	G<263>	-3468	338.5	17	75
877	G<261>	-3489	438.5	17	75
878	G<259>	-3510	338.5	17	75
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880	G<255>	-3552	338.5	17	75
881	G<253>	-3573	438.5	17	75

#	Pad	X	Y	W	H
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885	G<245>	-3657	438.5	17	75
886	G<243>	-3678	338.5	17	75
887	G<241>	-3699	438.5	17	75
888	G<239>	-3720	338.5	17	75
889	G<237>	-3741	438.5	17	75
890	G<235>	-3762	338.5	17	75
891	G<233>	-3783	438.5	17	75
892	G<231>	-3804	338.5	17	75
893	G<229>	-3825	438.5	17	75
894	G<227>	-3846	338.5	17	75
895	G<225>	-3867	438.5	17	75
896	G<223>	-3888	338.5	17	75
897	G<221>	-3909	438.5	17	75
898	G<219>	-3930	338.5	17	75
899	G<217>	-3951	438.5	17	75
900	G<215>	-3972	338.5	17	75
901	G<213>	-3993	438.5	17	75
902	G<211>	-4014	338.5	17	75
903	G<209>	-4035	438.5	17	75
904	G<207>	-4056	338.5	17	75
905	G<205>	-4077	438.5	17	75
906	G<203>	-4098	338.5	17	75
907	G<201>	-4119	438.5	17	75
908	G<199>	-4140	338.5	17	75
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910	G<195>	-4182	338.5	17	75
911	G<193>	-4203	438.5	17	75
912	G<191>	-4224	338.5	17	75
913	G<189>	-4245	438.5	17	75
914	G<187>	-4266	338.5	17	75
915	G<185>	-4287	438.5	17	75
916	G<183>	-4308	338.5	17	75
917	G<181>	-4329	438.5	17	75
918	G<179>	-4350	338.5	17	75
919	G<177>	-4371	438.5	17	75
920	G<175>	-4392	338.5	17	75
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926	G<163>	-4518	338.5	17	75
927	G<161>	-4539	438.5	17	75
928	G<159>	-4560	338.5	17	75
929	G<157>	-4581	438.5	17	75
930	G<155>	-4602	338.5	17	75
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932	G<151>	-4644	338.5	17	75
933	G<149>	-4665	438.5	17	75
934	G<147>	-4686	338.5	17	75
935	G<145>	-4707	438.5	17	75
936	G<143>	-4728	338.5	17	75
937	G<141>	-4749	438.5	17	75
938	G<139>	-4770	338.5	17	75
939	G<137>	-4791	438.5	17	75
940	G<135>	-4812	338.5	17	75

#	Pad	X	Y	W	H
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942	G<131>	-4854	338.5	17	75
943	G<129>	-4875	438.5	17	75
944	G<127>	-4896	338.5	17	75
945	G<125>	-4917	438.5	17	75
946	G<123>	-4938	338.5	17	75
947	G<121>	-4959	438.5	17	75
948	G<119>	-4980	338.5	17	75
949	G<117>	-5001	438.5	17	75
950	G<115>	-5022	338.5	17	75
951	G<113>	-5043	438.5	17	75
952	G<111>	-5064	338.5	17	75
953	G<109>	-5085	438.5	17	75
954	G<107>	-5106	338.5	17	75
955	G<105>	-5127	438.5	17	75
956	G<103>	-5148	338.5	17	75
957	G<101>	-5169	438.5	17	75
958	G<99>	-5190	338.5	17	75
959	G<97>	-5211	438.5	17	75
960	G<95>	-5232	338.5	17	75
961	G<93>	-5253	438.5	17	75
962	G<91>	-5274	338.5	17	75
963	G<89>	-5295	438.5	17	75
964	G<87>	-5316	338.5	17	75
965	G<85>	-5337	438.5	17	75
966	G<83>	-5358	338.5	17	75
967	G<81>	-5379	438.5	17	75
968	G<79>	-5400	338.5	17	75
969	G<77>	-5421	438.5	17	75
970	G<75>	-5442	338.5	17	75
971	G<73>	-5463	438.5	17	75
972	G<71>	-5484	338.5	17	75
973	G<69>	-5505	438.5	17	75
974	G<67>	-5526	338.5	17	75
975	G<65>	-5547	438.5	17	75
976	G<63>	-5568	338.5	17	75
977	G<61>	-5589	438.5	17	75
978	G<59>	-5610	338.5	17	75

#	Pad	X	Y	W	H
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980	G<55>	-5652	338.5	17	75
981	G<53>	-5673	438.5	17	75
982	G<51>	-5694	338.5	17	75
983	G<49>	-5715	438.5	17	75
984	G<47>	-5736	338.5	17	75
985	G<45>	-5757	438.5	17	75
986	G<43>	-5778	338.5	17	75
987	G<41>	-5799	438.5	17	75
988	G<39>	-5820	338.5	17	75
989	G<37>	-5841	438.5	17	75
990	G<35>	-5862	338.5	17	75
991	G<33>	-5883	438.5	17	75
992	G<31>	-5904	338.5	17	75
993	G<29>	-5925	438.5	17	75
994	G<27>	-5946	338.5	17	75
995	G<25>	-5967	438.5	17	75
996	G<23>	-5988	338.5	17	75
997	G<21>	-6009	438.5	17	75
998	G<19>	-6030	338.5	17	75
999	G<17>	-6051	438.5	17	75
1000	G<15>	-6072	338.5	17	75
1001	G<13>	-6093	438.5	17	75
1002	G<11>	-6114	338.5	17	75
1003	G<9>	-6135	438.5	17	75
1004	G<7>	-6156	338.5	17	75
1005	G<5>	-6177	438.5	17	75
1006	G<3>	-6198	338.5	17	75
1007	G<1>	-6219	438.5	17	75
1008	GD<1>	-6240	338.5	17	75
1009	NC	-6261	438.5	17	75
1010	NC	-6282	338.5	17	75
1011	NC	-6303	438.5	17	75
1012	NC	-6324	338.5	17	75
1013	NC	-6345	438.5	17	75