Datasheet from	http://www.titanmec.com/index.php/en/product/lists/typeid/88/p/4.html
	http://www.titanmec.com/index.php/en/project/download/id/542.html
Translated using	https://translate.google.com

Characteristic description

TM1652 is a LED (light emitting diode, digital tube, point array screen) drive control special chip, built-in digital communication circuit, decoder circuit, data lock, oscillator, LED driver circuit. The communication method uses the UART protocol.

Receive data from the single-chip machine, only need one TX port of the single-chip machine to send data to the chip, achieve single-line communication; in the display driver

On the other hand, the chip adopts dynamic scanning method, two display modes can be selected, 8-level segment drive current adjustable, 16-level segment occupancy ratio adjustable; TM1652 Built-in extinguishing processing optimization circuit.

This product is applied to various consumer electronic products, very widely used, such as: air conditioner panel, washing machine panel, DVD display panel, top box display etc. This product has excellent performance, reliable quality..

Functional characteristics

- o Use power CMOS technology
- o Typical working voltage: 5V
- o Support for digital display
- o Two display modes (7 segments × 6 bits, 8 segments × 5 bits)
- o Brightness adjustment circuit (Bit duty cycle 16 level adjustable, segment driving current 8 level adjustable)
- o Serial interface (SDA), compatible with serial communication (UART) protocol, support baud rate 19200bps
- o Built-in OSC frequency 2.5M
- o Built-in electric reset circuit
- o Built-in optimization circuit for dark and bright problem
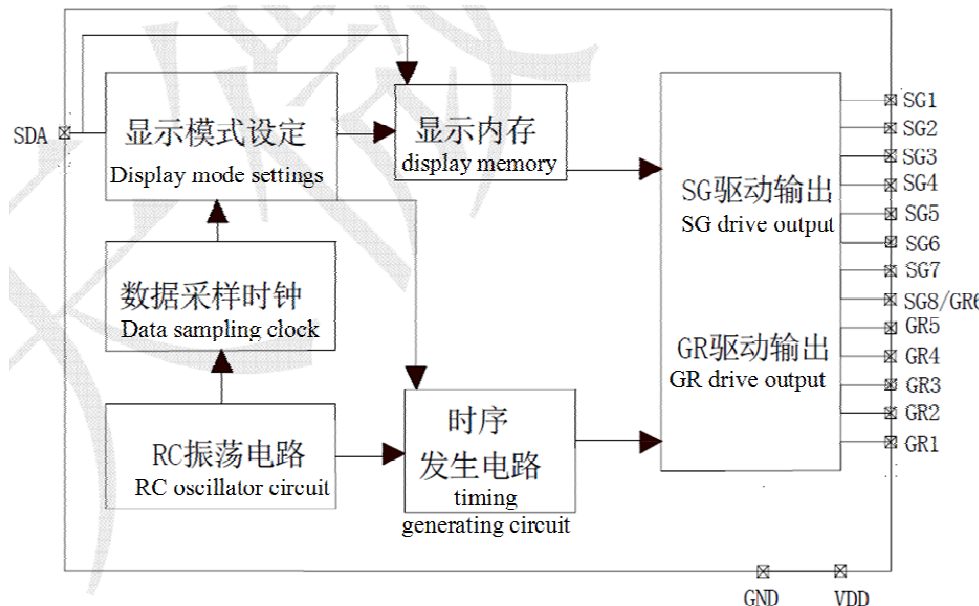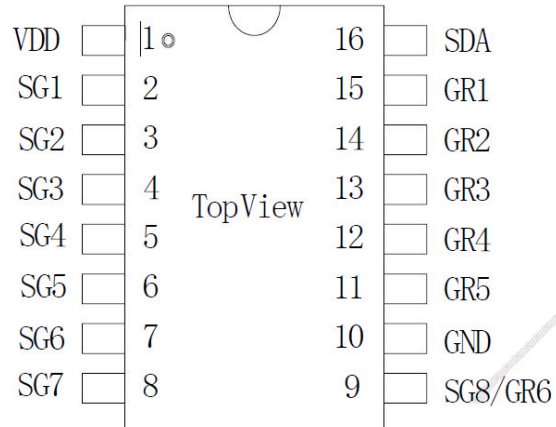- o Package format: SOP16

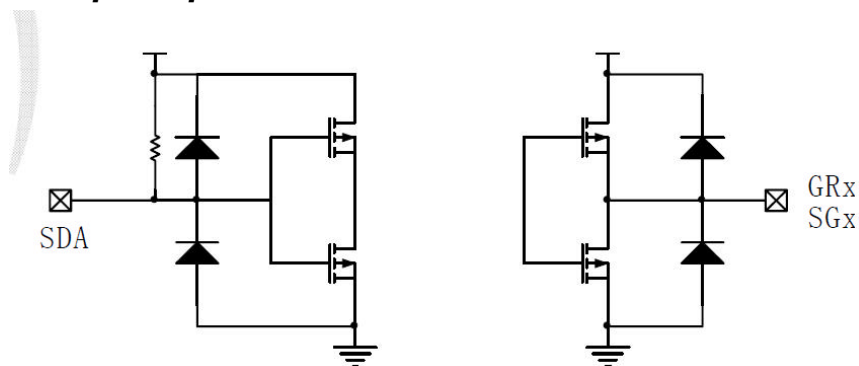## Internal structure block diagram

figure 1

Pin information

Pin function

Pin Name	Pin No.	I/O	Function Description
VDD	1	--	power positive
SG1~SG7	2~8	O	Segment output, built-in PMOS 8-level drive current adjustable for driving LED source current output
SG8/GR6	9	O	Segment/bit multiplexing output, taking into account the functions of SEG and GRID, by software configuration
GR1~GR5	11~15	O	Bit output, built-in NMOS 16-level adjustable duty cycle, as a driver LED sink current output
GND	10	--	power ground
SDA	16	I	Data input pin

Note: The SG8/GR6 multiplexed output pin cannot be connected to the segment drive pin and the bit drive pin of the digital tube at the same time. Display is abnormal.

Input and output equivalent circuit

Integrated circuits are electrostatic sensitive devices, which are prone to generate a lot of static electricity when used in dry seasons or in dry environments. Electrostatic discharge may damage the integrated circuits. Titan Microelectronics recommends taking all appropriate integrated circuit preventive measures, improper operation and soldering may cause ESD damage or performance degradation, and the chip cannot work properly.

Limit parameters

Parameter name	Parameter symbol	Limit value	Unit
Logic Supply Voltage	VDD	+7.0	V
Logic input voltage	VI1	VDD + 0.5	V
GR drive output current	IO2	170mA@0.3V	mA
Power loss	PD	400	mW
Working temperature	Topt	-40 ～ +80	℃
Storage temperature	Tstg	-65 ～+150	℃
ESD	Human Body Model (HBM)	3000	V
	Machine Mode (MM)	200	V

(1) When the chip works under the above limit parameters for a long time, the reliability of the device may be reduced or permanent damage may be caused, which parameter reaches or exceeds these limits.
(2) All voltage values are tested with respect to system ground.

Recommended working conditions

Tested at -45℃~+85℃, unless otherwise specified   TM1652

Parameter Name	Parameter Symbol	Test Condition	Min	Typical	Max	unit
Logic Supply Voltage	VDD	—	3	5	6	V
High level input voltage	VIH	—	0.7VDD	—	VDD	V
Low level input voltage	VIL	—	0	—	0.3VDD	V

Electrical Characteristics

Tested at -20℃~+85℃, unless otherwise specified; VDD = 5V, GND = 0V   TM1652

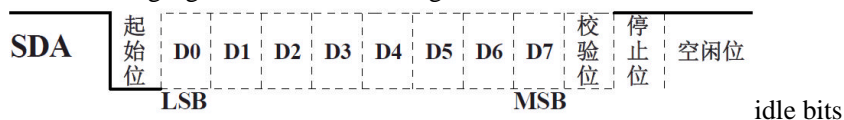| Parameter name	Parameter symbol	Test condition	Min.	Typ.	Max.	unit
SG high level output current	Ioh1	SG drive strength 8/8, SG1~SG8 ports Boost 3V when high test	20	25	30	mA
	Ioh2	SG drive strength 8/8, SG1~SG8 port Boost 2V when high test	20	30	40	mA
GR low level input current	IOL1	GR1~GR6 ports are low Voltage 0.3V when level test	80	140	—	mA
SDA input current	Isda	VDD=5V, other pins are suspended null	—	—	±1	μA
High level input voltage	VIH	VDD=5V	0.7 VDD	—	—	V
Low level input voltage	VIL	VDD=5V	—	—	0.3 VDD	V
Hysteresis voltage	VH	VDD=5V	—	0.35	—	V
Dynamic current consumption	IDDdyn	no load, display off	—	—	5	mA

Switching Characteristics

Tested at -20℃~+85℃, unless otherwise stated VDD=5V, GND=0V   TM1652

Parameter Name	Parameter Symbol	Test Condition	Min	Typ	Max	unit
Internal oscillator frequency	fosc	—	—	2.5	—	MHz
GR scan period	Fgr	SG8*GR5 mode	450	500	550	Hz
		SG7*GR6 mode	370	420	470	
Baud rate bit width	Bsda	VDD=5V	47	52	57	μs
SDA data frequency	Fmax	duty cycle 50%	1	—	—	MHz
SDA input capacitance	CI	—	—	—	15	pF

Function Description

1. Communication protocol

This chip adopts asynchronous serial communication (UART) protocol. The working principle is to transfer each character of the transmitted data one by one in serial mode transmission. The following figure shows its working mode:

The time of each bit of TM1652 is: 52us.

The meaning of each bit is as follows:

▲Start bit: from high to low, the low level time is one bit time, indicating the beginning of the transmission character.

▲Data bit: Immediately after the start bit, D0-D7, the low bit is sent first.

▲Check bit: It is a time of one bit. If the number of 1 in the 8-bit data bit is odd, the bit is set to 0 (set low), otherwise it is 1 (set high level).

▲Stop position: set high. The time is one bit time, which is the end mark of sending one character data.

▲Idle bit: set high. If the idle position is high for more than 3ms, TM1652 considers that this data frame is over, and this time the data is transferred from the scratchpad.

Enter the corresponding register to control the chip output. If a frame of data transmission does not end, it is recommended to set the idle bit time range within S0-0.5ms.

One frame of TM1652 data includes the following two forms:
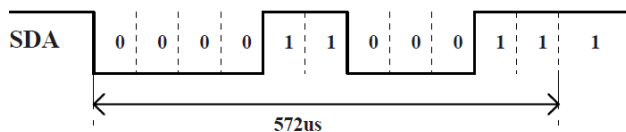
⑴ Display address command + display data;

⑵ Display control command + display control adjustment command.

Baud rate: is a pointer to measure the data transfer rate. Expressed as the number of binary digits (bits) transmitted per second. e.g. data transfer rate is 120 characters/second, and each character is 11 bits, then the baud rate of its transmission is 11×120=1320 bit/second=1320 baud. The baud rate range supported by TM1652 is: 17500bps ~ 21200bps, here we recommend using 19200bps

The time is: 1s (seconds)/19200≈52us (microseconds). So the time range of each bit supported by TM1652 is: 47us～57us.

When using IO to simulate UART communication, the bit width of SDA data should meet the provided bit width range.

Let's take the baud rate of 19200bps as an example, and send the display control command "0X18" to the SDA pin. The timing waveform diagram is as follows:

As shown in Figure 5 above, a total of 11 bits of "0x18" are sent, from left to right are 1 start bit, 8 data bits, 1 check bit, and 1 stop bit. The time of each bit is about 52us, and the total time of 11 bits is about 572us. From the above figure, we read binary data as "00011000", which is converted to base sixteen as "0x18".

Note: TM1652 can also receive control signals from MCU powered by 3.3V in addition to receiving control signals from MCU powered by 5V. It is recommended to use a system with a different power supply.

2. Display command description

MSB   LSB

B7	B6	B5	B4	B3	B2	B1	B0	Description
address bit			0	1	0	0	0	show address command
0	0	0	1					Display control commands

B3 to B0 are 1000 fixed data for internal clock correction.

3. Display data description

MSB   LSB

B7	B6	B5	B4	B3	B2	B1	B0
SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1

Corresponding to the BIT bit, setting "0" means invalid and outputting low level, setting "1" means valid and outputting high level. For example, "0x01" means SG1 output is high.

4. Display address command description

MSB   LSB

B7	B6	B5	B4	B3	B2	B1	B0	Display address
0	0	0	0	1	0	0	0	GR1 address
1	0	0						GR2 address
0	1	0						GR3 address
1	1	0						GR4 address
0	0	1						GR5 address
1	0	1						GR6 address

B3 ~ B0 are 1000 fixed data for internal clock correction. Setting B4 to "0" indicates that the current data is the display address command

5. Display control adjustment command description

MSB   LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	Description
0	0	0	0					Display switch	setting Screen off
1	0	0	0					Bit drive duty cycle setting set	Set the duty cycle to 1/16
0	1	0	0						Set the duty cycle to 2/16
1	1	0	0						Set the duty cycle to 3/16
0	0	1	0						Set the duty cycle to 4/16
1	0	1	0						Set the duty cycle to 5/16

0	1	1	0						Set the duty cycle to 6/16
1	1	1	0						Set the duty cycle to 7/16
0	0	0	1						Set the duty cycle to 8/16
1	0	0	1						Set the duty cycle to 9/16
0	1	0	1						Set the duty cycle to 10/16
1	1	0	1						Set the duty cycle to 11/16
0	0	1	1						Set the duty cycle to 12/16
1	0	1	1						Set the duty cycle to 13/16
0	1	1	1						Set the duty cycle to 14/16
1	1	1	1						Set the duty cycle to 15/16
				0	0	0		Segment drive current setting	Set segment drive current to 1/8
				1	0	0			Set segment drive current to 2/8
				0	1	0			Set segment drive current to 3/8
				1	1	0			Set segment drive current to 4/8
				0	0	1			Set segment drive current to 5/8
				1	0	1			Set segment drive current to 6/8
				0	1	1			Set segment drive current to 7/8
				1	1	1			Set segment drive current to 8/8
							0	Display Mode Settings	Set 8-segment 5-bit output
							1		Set 7-segment 6-bit output

This command is used to set the bit duty cycle, segment drive current and display mode selection.
Note: When the segment drive current is 1/8, the current provided by the chip is not enough to light the ordinary digital tube, so it is recommended to set the segment drive current to 2/8 at least.

Application Information

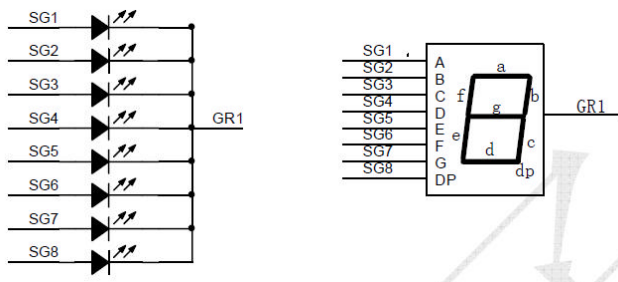### 1. TM1652 command data definition

The first Byte data is set for the control command, and the low bit is sent first. Among them, the lower four bits B3 ~ B0 are 1000 fixed data. B4 is to send Register type selection, "1" selects display control command, "0" selects display address command. B7～B5 are the setting display addresses.

The data starts from the second Byte data, and is sent to the corresponding temporary register according to the address in the first Byte control command. The second Byte must be the display control adjustment command. If it is a display address command, it can be multi-byte data, and subsequent bytes the address is incremented by 1 and placed in the corresponding scratchpad. If the address exceeds the corresponding valid address, the address above 101 will be displayed, and part of the data will be exceeded.
Invalid, if the address contained in the first Byte exceeds the corresponding valid address or invalid address, this data is invalid. It is recommended to apply Send display data, and then send control data (on display), if the control data (on display) is sent first, the display register is not cleared.
When the random data in the display register is output, the digital tube displays garbled characters until the display register receives the correct display data.

2. Drive common cathode digital tube:

The figure above shows the connection diagram of the common cathode nixie tube. If the nixie tube displays "0", it is necessary to set SG1 when GR1 is low.

SG2, SG3, SG4, SG5, SG6 are high level, set SG7, SG8 to low level, check the address table below, just display the ground at 00H.

The address unit can write data 3FH to make the digital tube display "0". The detailed data packet is: first send the address command "0X08", followed by the display data "0X3F" means to store "0X3F" in the address 00H and output it through the SG pin. Other addresses are not allowed to send "0X00" to make the digital tube not display, and then the SDA pin is set high for at least 3ms, and then the display control command and display control adjustmec command are sent. After sending, the SDA pin is set high for at least 3ms. At this time the nixie tube displays "0".

SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	
0	0	1	1	1	1	1	1	0x3F
B7	B6	B5	B4	B3	B2	B1	B0	

3. Data packet transmission method

3.1 The address is automatically incremented by 1 mode

Using the address auto-add 1 mode, setting the address is actually setting the starting address where the transmitted data stream is stored. Start address command word

After the transmission is completed, the data is sent immediately, up to 6BYTE, and the data line is set high after the data is sent.

| SDA | Command1 | Data1 | Data2 | ...... | Data n | Time | CommandX | CommandY | Time | |

Command1: Select display address command (0x08)
Data1~Data n: Send display data (up to 6bytes)
Time: Data line high time (minimum time is 3ms)
CommandX: select display control command (0x18)
CommandY: Send display control adjustment commands (including bit duty cycle, segment drive current, and display mode settings)

3.2 Fixed address mode

Using the fixed address mode, setting the address is actually setting the address where the 1BYTE display data to be sent is stored. After sending the address,
Immediately after sending 1BYTE display data, after the data is sent, set the number of data high for at least 3ms, and then send the address, followed by
Send 1BYTE display data, followed by setting the data line high for at least 3ms, and so on, until the address and data are sent.

| SDA | Command1 | Data1 | Time | ...... | Command n | Data n | Time | CommandX | CommandY | Time | |

Command1~Command n: Send display address command, address 1~n (up to 6 addresses can be set)
Data1~Data n: Send display data (up to 6 bytes)
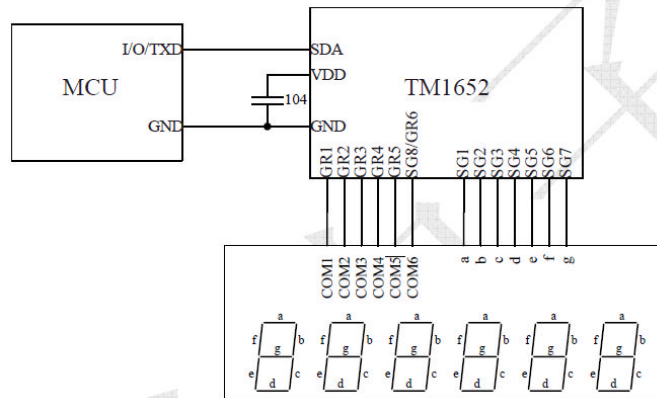Time: Data line high time (minimum time is 3ms)
CommandX: Send display control command (0x18)
CommandY: Send display control adjustment commands (including bit duty cycle, segment drive current, and display mode settings)
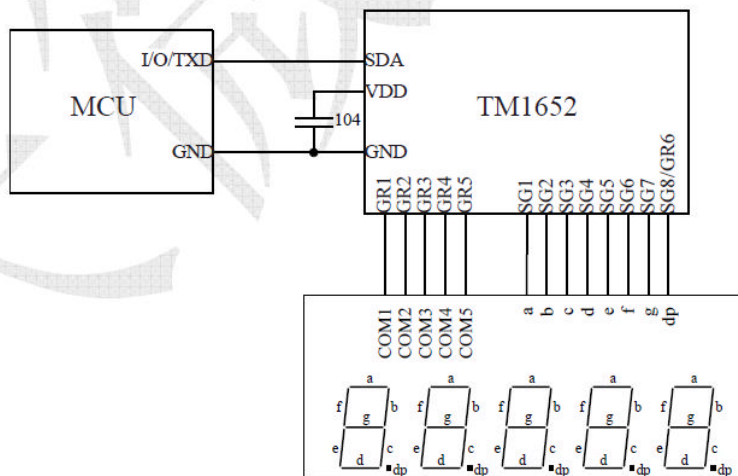The chip does not need commands to set whether the chip works in the address auto-add 1 mode or the fixed address mode. Strictly speaking, it has only one ground.
The address is automatically incremented by 1. The division here is to better explain that the chip can also write display data to a certain display register address separately. If display data is written to a single display address. After writing the display address, only one display data can be written, and set the signal line high for at least 3ms. If several display data are written next, then after the chip receives the first data, the display address will be automatically at the specified address, incremented by 1, and then receive the second display data, until the display data of the last display address is received.

4. 7-segment × 6-bit application circuit connection:

5. 8-segment × 5-bit application circuit connection:

Note: Please add a 104 decoupling capacitor to the chip VDD and GND during application. The shorter the connection between the decoupling capacitor and the chip VDD and GND, the better the decoupling effect, and the more stable the chip works.
The chip is designed for common-cathode digital tube drive and is not suitable for common-anode digital tube drive.

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Package Diagram (SOP16)