

2-Wire Serial EEPROM

32(4096 × 8)

64(8192 × 8)

Features:

- Low-Voltage and Standard-Voltage Operation
 - 5.0(V_{CC} = 4.5V to 5.5V)
 - 2.7(V_{CC} = 2.7V to 5.5V)
 - 2.5(V_{CC} = 2.5V to 5.5V)
 - 1.8(V_{CC} = 1.8V to 5.5V)
- Low-Power Devices (I_{SB} - 2 μA @ 5.5V) Available
- Internally Organized 4096 × 8, 8192 × 8
- 2-wire serial interface
- Schmitt Trigger, Filtered inputs for noise suppression
- Bidirectional Data Transfer Protocol
- 100kHz (1.8V, 2.5V, 2.7V) and 400 kHz (5V) compatibility
- Write protect Pin for Hardware Data Protection
- 32-Byte Page Write Mode (Partial Page Writes Allowed)
- Self-Timed Write Cycle(10ms max)
- High Reliability
 - Endurance: 1 Million Write Cycles
 - Data Retention: 100 Years
 - ESD Protection: >3000V
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin JEDEC PDIP, 8-Pin and 14-Pin JEDEC SOIC, 8-Pin EIAJ SOIC, and 8-pin TSSOP Packages

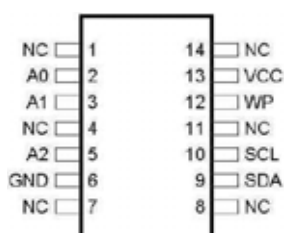
Description:

The 24LC32/64 provides 32,768/65,536 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 4096/8192 words of 8 bits each. The device's cascable feature allows up to 8 devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The 24LC32/64 is available in space saving 8-pin JEDEC PDIP, 8-pin and 14-pin JEDEC SOIC, 8-pin EIAJ SOIC, and 8-pin TSSOP packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V), 2.5V (2.5V to 5.5V) and 1.8V(1.8V to 5.5V) versions.

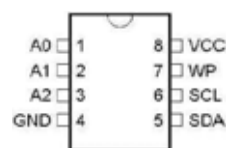
Pin Configurations

Pin Name	Function
A0 to A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect

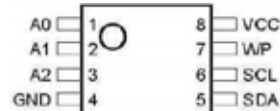
14-Pin SOIC



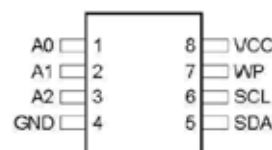
8-Pin PDIP



8-Pin TSSOP



8-Pin SOIC



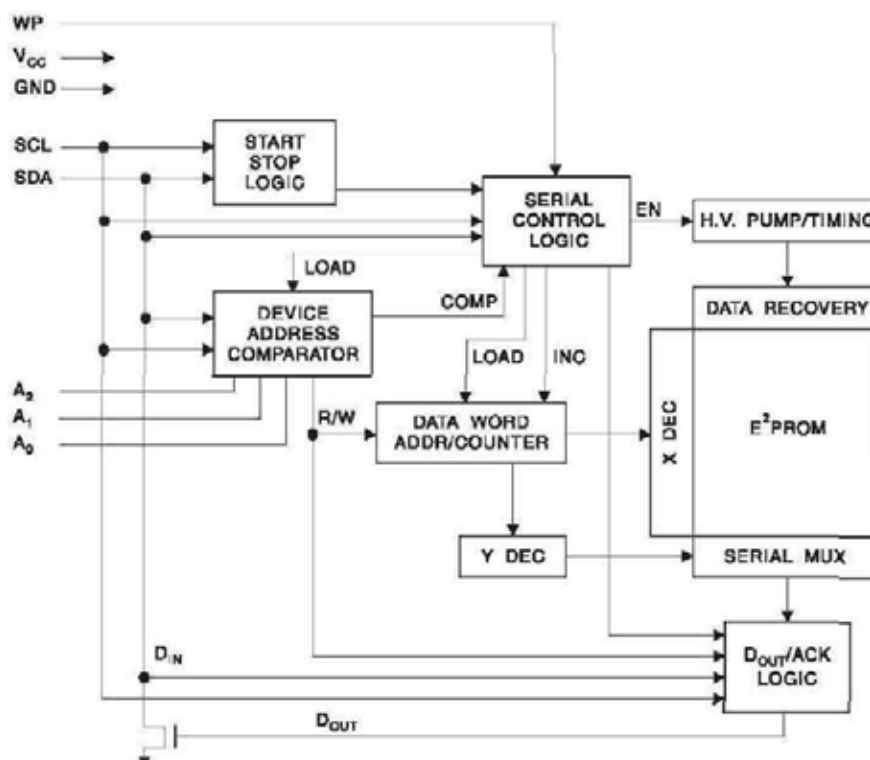
Absolute Maximum Ratings*

Operating Temperature.....-55 to +125
 Storage Temperature.....-65 to +150
 Voltage on Any Pin
 With Respect to Ground.....-1.0V to +7.0V

Maximum Operating Voltage.....6.25V
 DC Output Current.....5.0mA

***NOTICE:** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hard wired or left not connected for hardware compatibility with AT24C16. When the pins are hardwired, as many as eight 32K/64K devices may be

addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). When the pins are not hardwired, the default A₂, A₁, and A₀ are zero.

WRITE PROTECT (WP): The write protect input, when tied to GND, allows normal write operations. When WP is tied high to V_{CC}, all write operations to the upper quadrant (8/16K bits) of memory are inhibited. If left unconnected, WP is internally pulled down to GND.

Memory Organization

24LC32/64, 32K/64K SERIAL EEPROM: The 32K/64K is internally organized as 256 pages of 32 bytes each. Random word addressing requires a 12/13 bit data word address.

Pin Capacitance ⁽¹⁾

Applicable over recommended operating range from $T_A = 25$, $f = 1.0\text{MHz}$, $V_{CC} = +1.8\text{V}$.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance(SDA)	8	pF	$V_{I/O} = 0\text{V}$
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	$V_{IN} = 0\text{V}$

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: $T_{AI} = -40$ to $+85$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$, $T_{AC} = 0$ to $+70$,

$V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$ (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		1.8		5.5	V
V_{CC2}	Supply Voltage		2.5		5.5	V
V_{CC3}	Supply Voltage		2.7		5.5	V
V_{CC4}	Supply Voltage		4.5		5.5	V
V_{CC1}	Supply Current $V_{CC} = 5.0\text{V}$	READ at 100KHz		0.4	1.0	mA
V_{CC2}	Supply Current $V_{CC} = 5.0\text{V}$	WRITE at 100KHz		2.0	3.0	mA
I_{SB1}	Standby Current (1.8V option)	$V_{CC}=1.8\text{V}$	$V_{IN} = V_{CC} \text{ or } V_{SS}$		0.1	μA
		$V_{CC}=5.5\text{V}$			2.0	
I_{SB2}	Standby Current (2.5V option)	$V_{CC}=2.5\text{V}$	$V_{IN} = V_{CC} \text{ or } V_{SS}$		0.5	μA
		$V_{CC}=5.5\text{V}$			2.0	
I_{SB3}	Standby Current (2.7V option)	$V_{CC}=2.7\text{V}$	$V_{IN} = V_{CC} \text{ or } V_{SS}$		0.5	μA
		$V_{CC}=5.5\text{V}$			2.0	
I_{SB4}	Standby Current (5V option)	$V_{CC}=4.5-5.5\text{V}$	$V_{IN} = V_{CC} \text{ or } V_{SS}$	20	35	μA
I_{LI}	Input Leakage Current	$V_{IN} = V_{CC} \text{ or } V_{SS}$		0.10	3.0	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC} \text{ or } V_{SS}$		0.05	3.0	μA
V_{IL}	Input Low Level ⁽¹⁾		-0.6		$V_{CC} \times 0.3$	V
V_{IH}	Input High Level ⁽¹⁾		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL2}	Output Low Level $V_{CC} = 3.0\text{V}$	$I_{OL} = 2.1 \text{ mA}$			0.4	V
V_{OL1}	Output Low Level $V_{CC} = 1.8\text{V}$	$I_{OL} = 0.15 \text{ mA}$			0.2	V

Notes: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from $T_A = -40$ to $+85$, $V_{CC} = +1.8V$ to $+5.5V$, $CL=1TTL$ Gate and $100 pF$ (unless otherwise noted).

Symbol	Parameter	1.8-volt		2.7-, 2.5-volt		5.0-volt		Units
		Min	Max	Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		100		100		400	KHz
t_{LDW}	Clock Pluse Width Low	4.7		4.7		1.2		μs
t_{HIGH}	Clock Pulse Width High	4.0		4.0		0.6		μs
t_I	Noise Suppression Time ⁽¹⁾		100		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	4.5	0.1	4.5	0.1	0.9	μs
t_{BUF}	Time the bus must be free Before a new transmission can start ⁽¹⁾	4.7		4.7		1.2		μs
$t_{HD.STA}$	Start Hold Time	4.0		4.0		0.6		μs
$t_{SU.STA}$	Start Set – up Time	4.7		4.7		0.6		μs
$t_{HD.STA}$	Data In hold time	0		0		0		μs
$t_{SU.STA}$	Data In Set-up Time	200		200		100		ns
t_R	Inputs Rise Time ⁽¹⁾		1.0		1.0		0.3	μs
t_F	Inputs Fall Time ⁽¹⁾		300		300		300	ns
$t_{SU.STO}$	Stop Set-up Time	4.7		4.7		0.6		μs
t_{DH}	Data Out Hold Time	100		100		50		ns
t_{WR}	Write Cycle Time		20		10		10	ms
Endurance ⁽¹⁾	5.0V, 25 , Page Mode	1M		1M		1M		Write Cycles

Note: 1, This parameter is characterized and is not 100% tested.

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin s normally pulled high with an external device, Data on the SDA pin may change only during SCL low time periods (refer to Data Validity timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition timing diagram).

STOP CONDITION: A low – to – high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Start and Stop Definition timing diagram).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

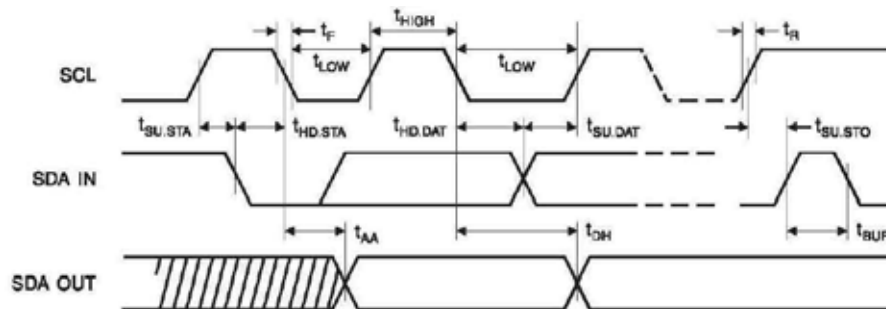
STANDBY MODE: The 24LC32/64 features a low power standby mode which is enabled : a) upon power-up and b) after the receipt of the STOP bit and the completion of any internal operations.

MEMORY RESET: After an interruption in protocol, power loss or system reset , any 2-wire part can be reset by following these steps:

(a)Clock up to 9 cycles, (b) look for SDA high in each cycle while SCL is high and then (c) create a start condition as SDA is high

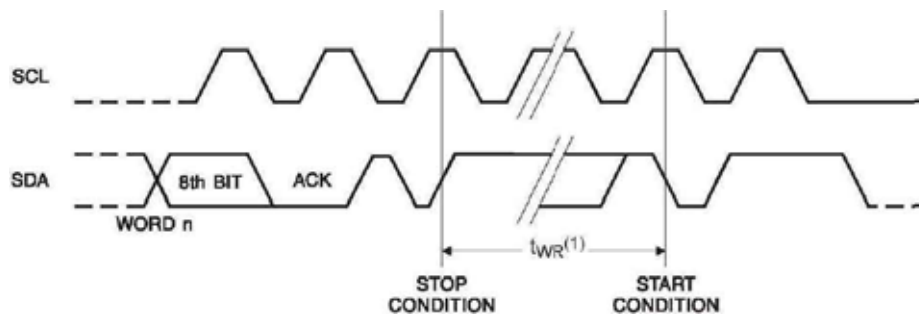
Bus Timing

SCL: Serial Clock, SDA : Serial Data I/O



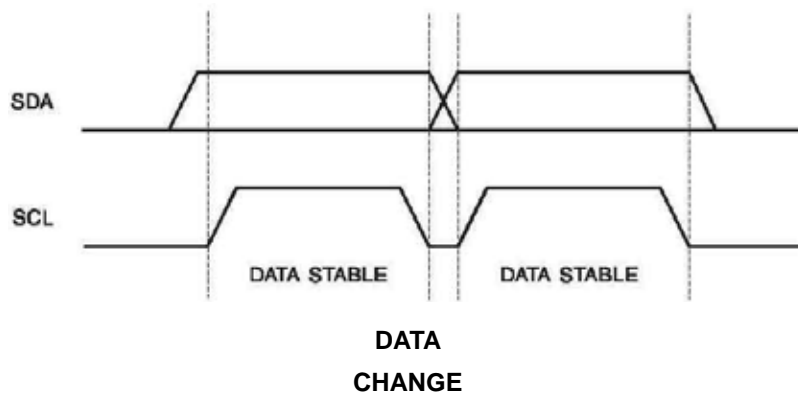
Write Cycle Timing

SCL: Serial Clock, SDA: Serial Data I/O

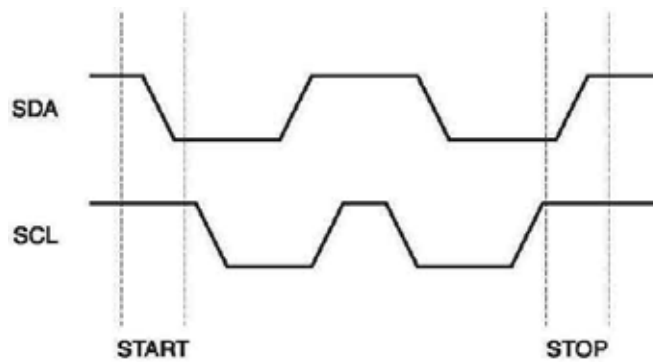


Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

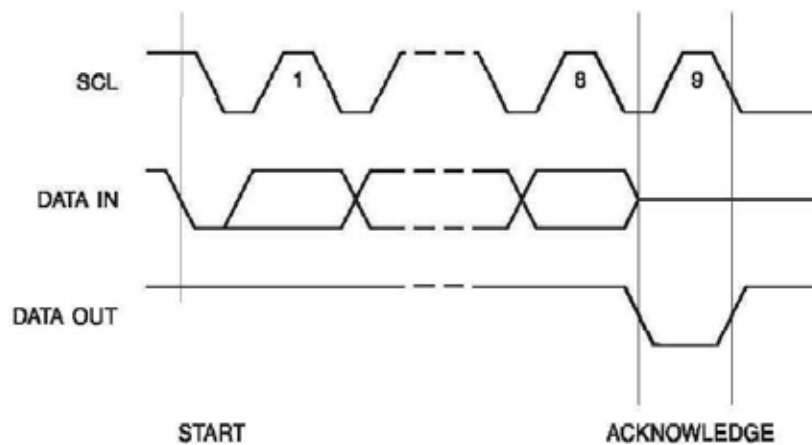
Data Validity



Start and Stop Definition



Output Acknowledge



Device Addressing

The 32k/64K EEPROM requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (refer to Figure 1). The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all 2-wire EEPROM devices.

The 32K/64k uses the three device address bits A2, A1, A0 to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins. The A2, A1, and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the device will return to standby state.

NOISE PROTECTION: Special internal circuitry placed on the SDA and SCL pins prevent small noise spikes from activating the device. A low- V_{CC} detector (5-volt option) resets the device to prevent data corruption in a noisy environment.

DATA SECURITY: The 24LC32/64 has a hardware data protection scheme that allows the user to write protect the upper quadrant (8/16K bits) of memory when the WP pin is at V_{CC} .

Write Operations

BYTE WRITE: A write operation requires two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, t_{WR} , to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (refer to Figure 2).

PAGE WRITE: The 32K/64K EEPROM is capable of 32-byte page writes.

A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 31 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 3).

The data word address lower 5 bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page

row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 32 data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero, allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address “roll over” during read is from the last byte of the last memory page, to the first byte of the first page. The address “roll over” during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 4).

RANDOM READ: A random read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 5).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “roll over” and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 6).

Figure 1. Device Address

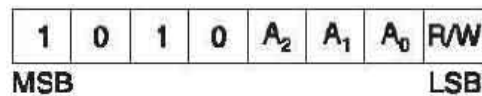


Figure 2. Byte Write

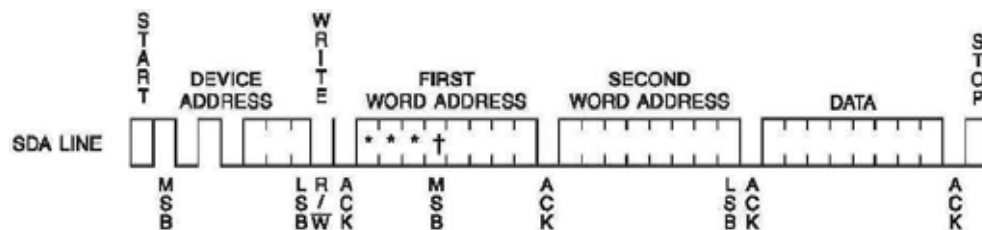
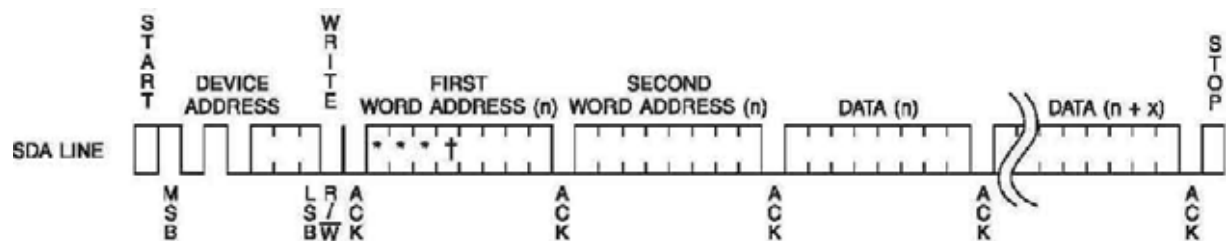


Figure 3. Page Write



Notes: 1. * = DON'T CARE bits

2. † = DON'T CARE bits for the 32K

Figure 4. Current Address Read

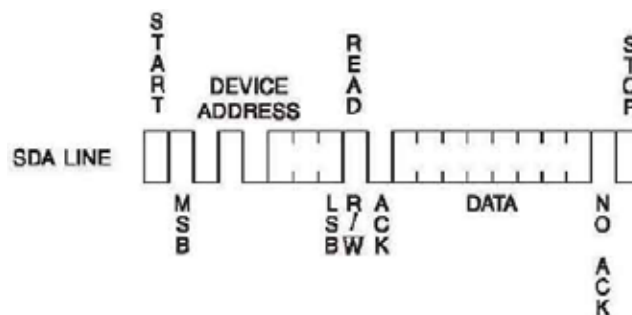
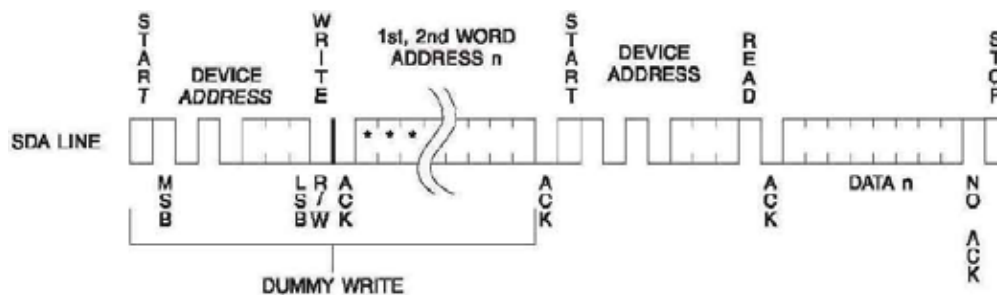
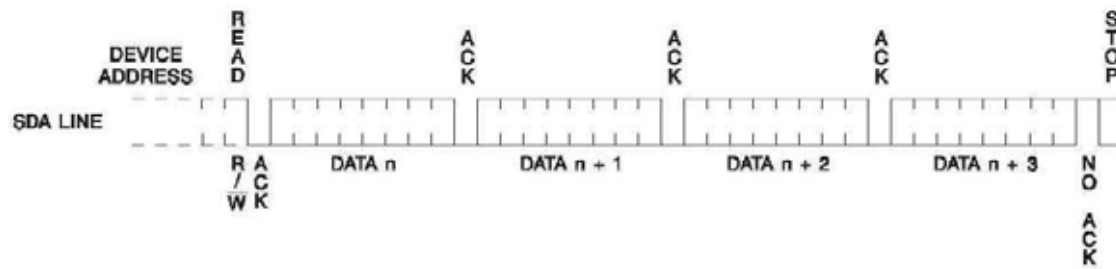


Figure 5. Random Read



Note: 1. * = DON'T CARE bits

Figure 6. Sequential Read

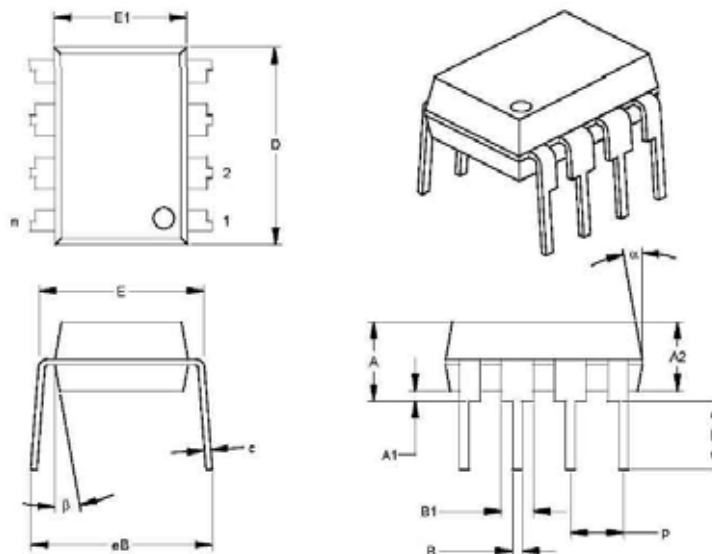


Part Number	1st Line Marking Codes					
	TSSOP	MSOP	SOT-23		DFN	
			I Temp.	E Temp.	I Temp.	E Temp.
24LC32B	4L02	4L2BT	M2NN	N2NN	224	225

Note: T=Temperature grade (I,E)
 NN=Alphanumeric traceability code

Legend: XX...X	Part number or part number code
T	Temperature (I, E)
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week '01')
NNN	Alphanumeric traceability code (2 characters for small packages)

8-Lead Plastic Dual In-line (P) -300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	P		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	C	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	a	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

*Controlling Parameter

§ Significant Characteristic

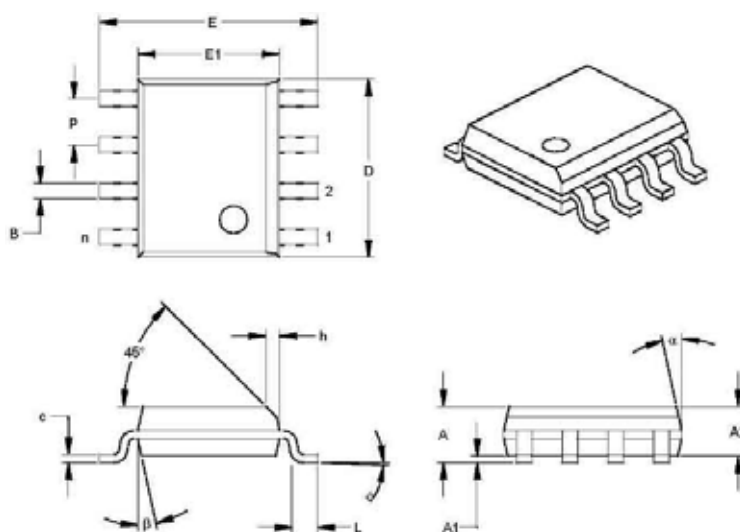
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent : MS-001

Drawing NO. C04-018

8-Lead Plastic Small Outline (SN) - Narrow, 150 mill (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.224	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	Ø	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	a	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

*Controlling parameter

§ Significant Characteristic

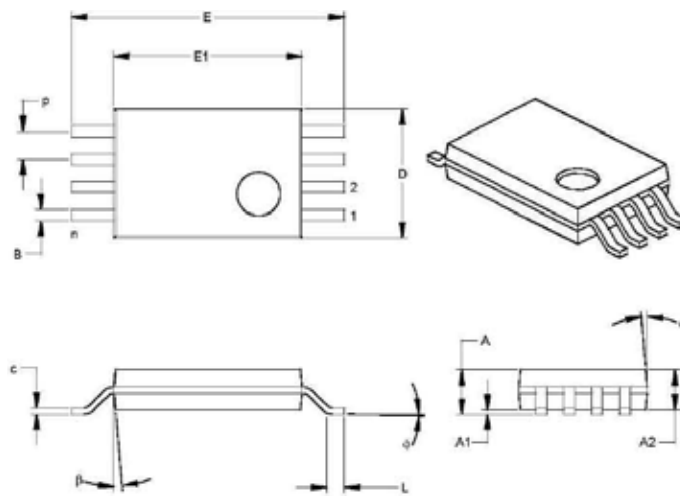
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS -012

Drawing No. C04-057

8-Lead Plastic Thin Shrink Small Outline (ST) — 4.4 mm (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	Ø	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	a	0	5	10	0	5	10
Mold Draft Angle Bottom	ß	0	5	10	0	5	10

*Controlling Parameter

§ Significant Characteristic

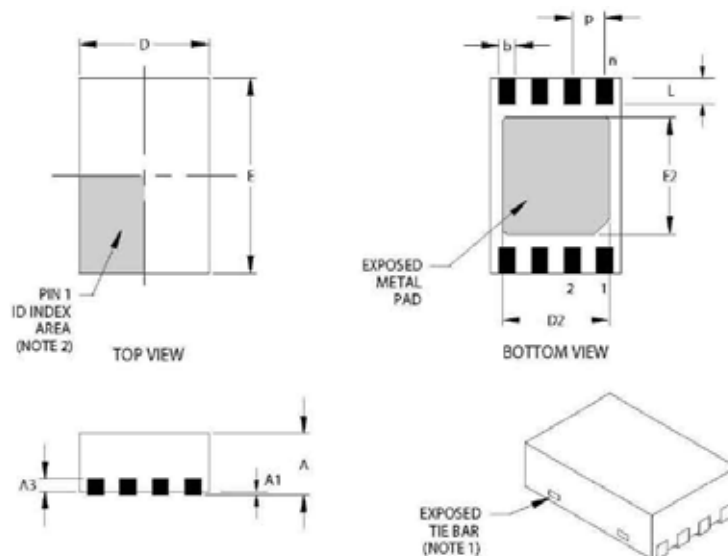
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

JEDEC Equivalent; MO-153

Drawing NO. C04-086

8-Lead Plastic Dual Flat No Lead Package (MC) 2x3x0.9 mm Body (DFN) – Saw Singulated



		Units	INCHES			MILLIMETERS*		
Dimension Limits			MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8		
Pitch	p		.020 BSC			0.50 BSC		
Overall Height	A		.031	.035	.039	0.80	0.90	1.00
Standoff	A1		.000	.001	.002	0.00	0.02	0.05
Contact Thickness	A3		.008REF			0.20 REF		
Overall Length	D		.079BSC			2.00 BSC		
Exposed Pad Length (Note3)	D2		.055	--	.064	1.39	--	1.62
Overall Width	E		.118BSC			3.00 BSC		
Exposed Pad Width (Note 3)	E2		.047	--	.071	1.20	--	1.80
Contact Width	b		.008	.010	.012	0.20	0.25	0.30
Contact Length	L		.012	.016	.020	0.30	0.40	0.50

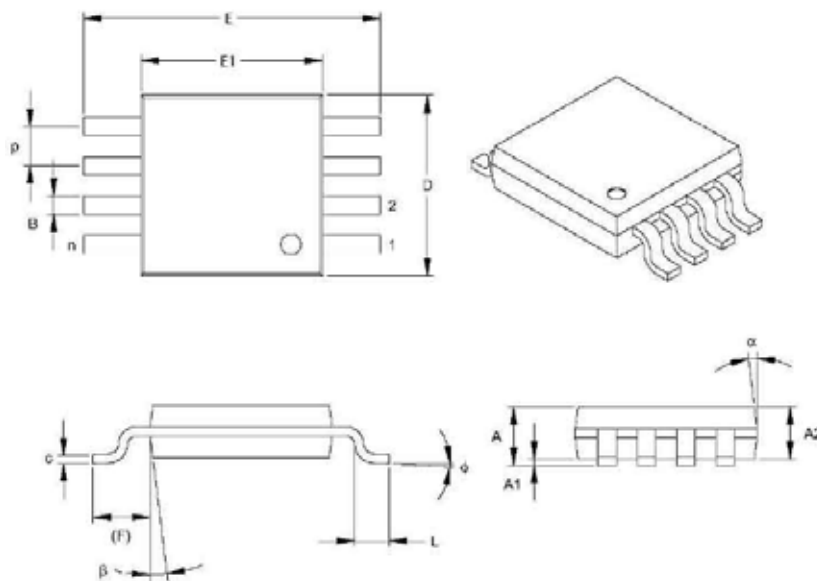
*Controlling Parameter

Notes:

1. Package May have one or more exposed tie bars at ends.
2. Pin 1 visual index feature may vary, but must be located within the hatched area.
3. Exposed pad dimensions vary with paddle size.
4. JEDEC equivalent: MO-229

Drawing No.C04-123

8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p	.026 BSC			0.65 BSC		
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E	.193 TYP			4.90 BSC		
Molded Package Width	E1	.118 BSC			3.00 BSC		
Overall Length	D	.118 BSC			3.00 BSC		
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F	.037 REF			0.95 REF		
Foot Angle	Ø	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	a	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°	5°	-	15°

*Controlling Parameter

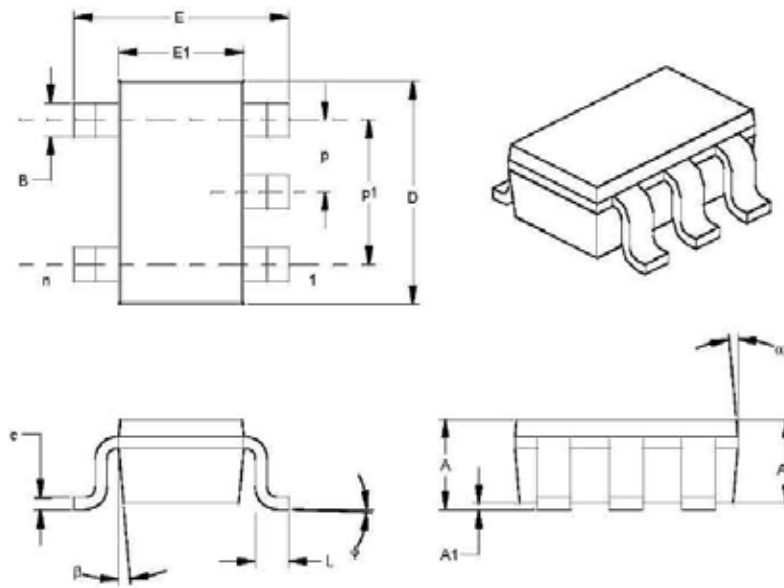
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-187

Drawing No. C04-111

5-Lead Plastic Small Outline Transistor (OT) (SOT-23)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		5			5	
Pitch	p		.038			0.95	
Outside lead pitch (basic)	p1		.075			1.90	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff §	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	Ø	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	a	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

*Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010"(0.254mm) per side.

JEDEC Equivalent: MO-178

Drawing No. C04-091