Flash Memory Testing

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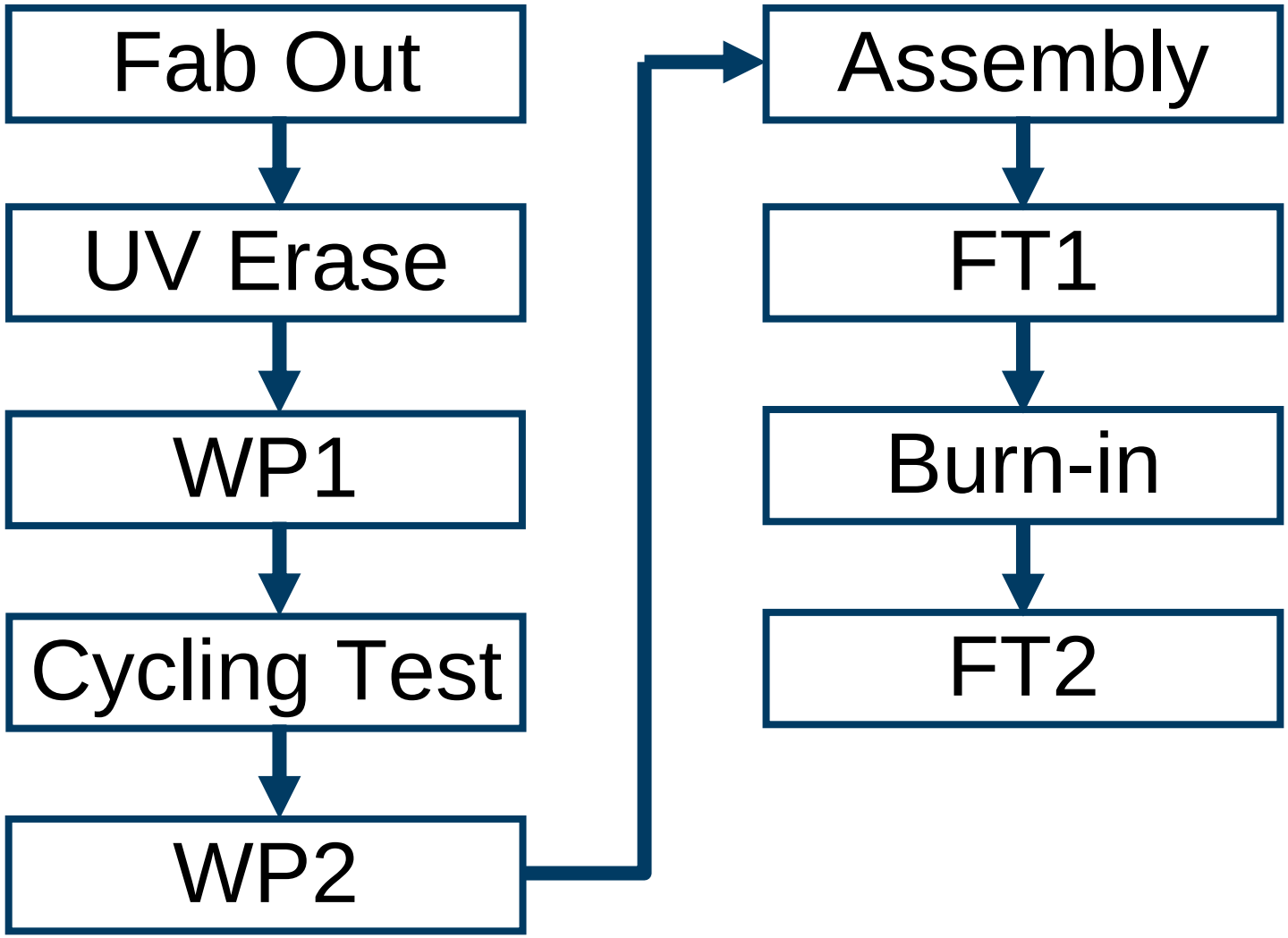
Outline

- Introduction to flash memories
- Flash memory fault models
  - Disturbance faults
  - Conventional memory faults
  - Other flash memory faults
- Flash memory test algorithms
  - March-based test algorithms
  - Diagonal test algorithms
- Flash memory fault-coverage analysis
  - RAMSES-FT
- Flash memory BIST
- Flash memory BISD
- Conclusions

Flash Memory Testing

- Testing nonvolatile memories:
  - Masked ROM---exhaustive; pseudorandom
  - PROM (OTP) & EPROM---dummy row
  - EEPROM & flash memory---dummy row?
- Testing flash memory core is hard
  - Customized core and I/O
  - Isolation (accessibility)
  - Reliability issues: disturbances, over program/erase, under program/erase, data retention, cell endurance, etc.
  - Long program/erase time

A Typical Test Flow of Flash Memories

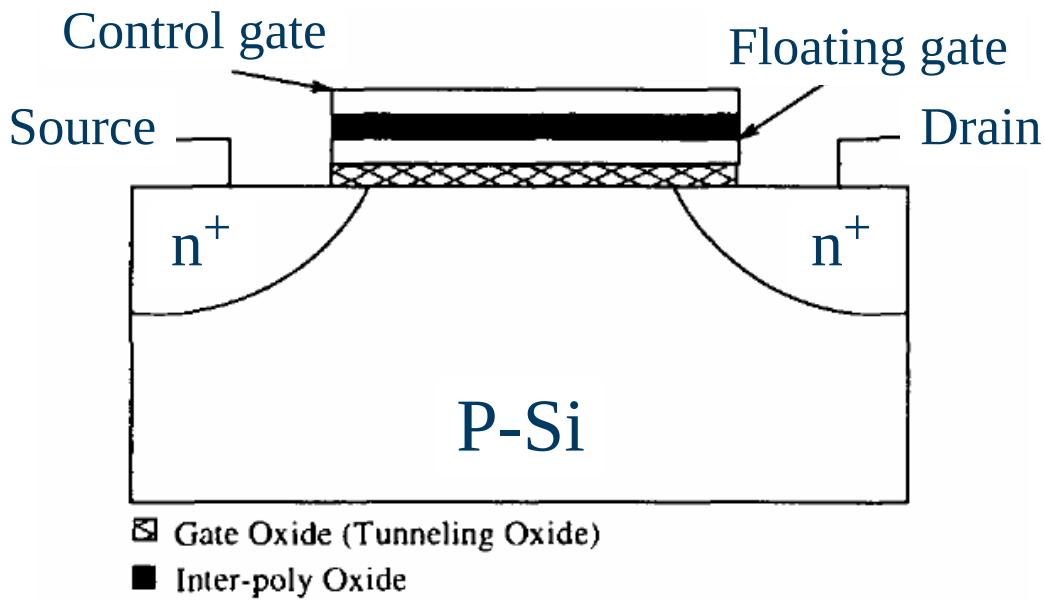


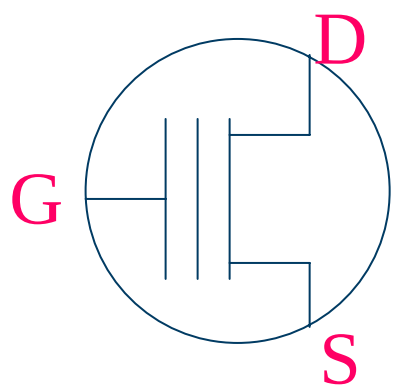
Test Approaches

- Reasonable fault models for reliability-related defects
- Efficient test algorithms to reduce test time and increase fault coverage
- Built-in self-test (BIST) circuit for embedded flash memories
  - Replace or reduce the requirement of ATE
- “Built-in self-test and built-in self-repair will be essential to test embedded memories and to maintain production throughput and yield” [ITRS 2001]

Flash Memory Overview

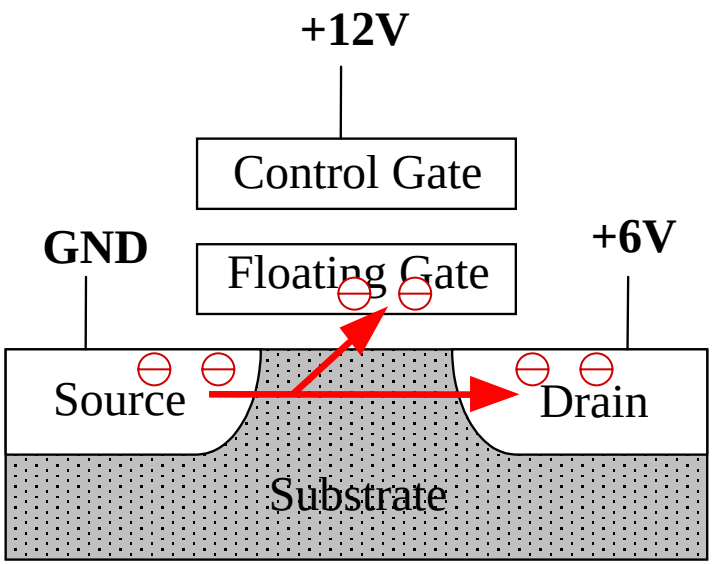
- Flash memory can be programmed and erased electrically
  - Has the advantages of EPROM and EEPROM
- A stacked gate transistor with both the control gate (CG) and floating gate (FG):





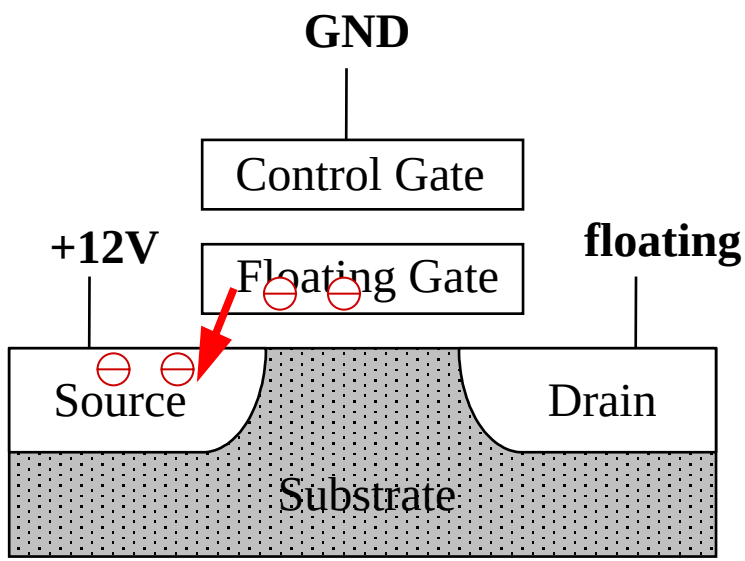
Flash Memory Program & Erase

- Program(1 to 0): channel hot-electron (CHE) injection or Fowler-Nordheim (FN) electron tunneling
- Erase (0 to 1): FN electron tunneling
  - By the entire chip or large blocks (flash erasure)
  - Different products have different program/erase mechanisms



Program: CHE injection

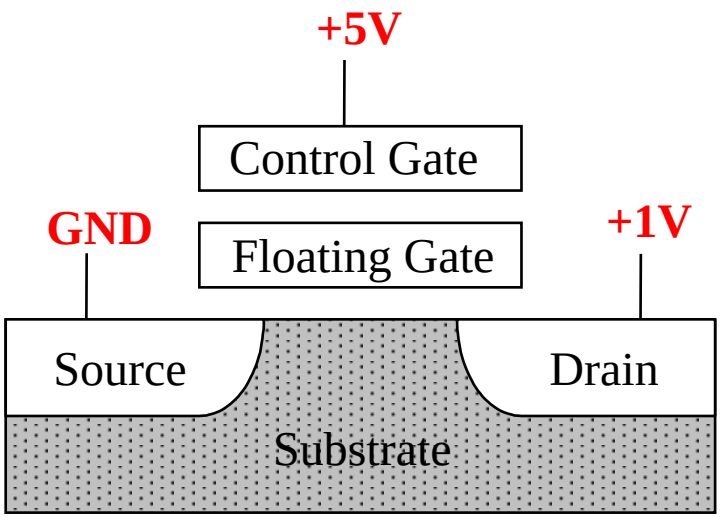
Write 0



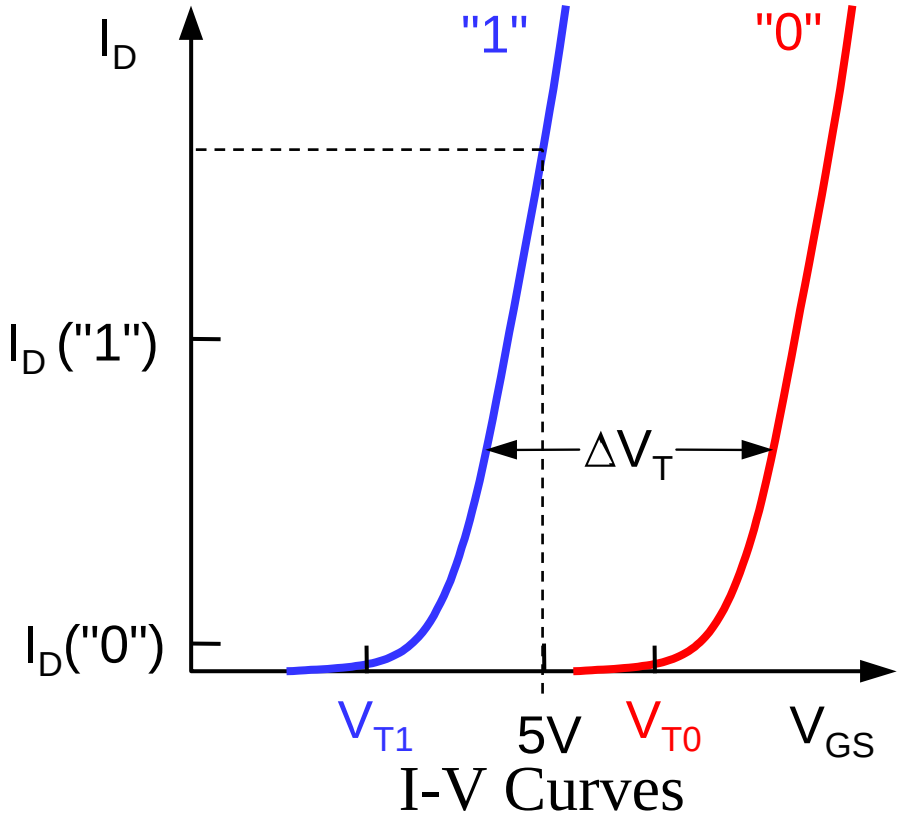
Erase: FN-tunneling

Write 1

Flash Memory Read



Read

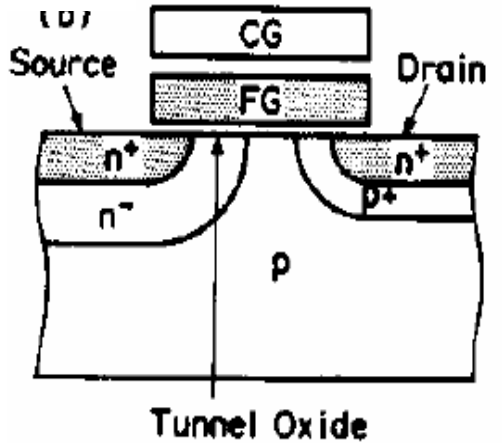


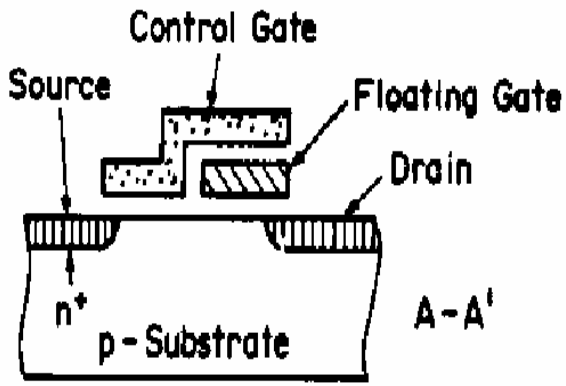
I-V Curves

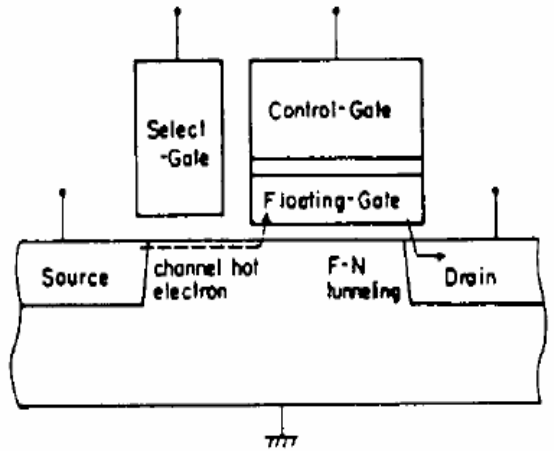
- The Erase operation is much slower than the Program operation, which in turn is slower than the Read operation

Flash Memory Cell Types

- Stacked-gate Split-gate Select-gate

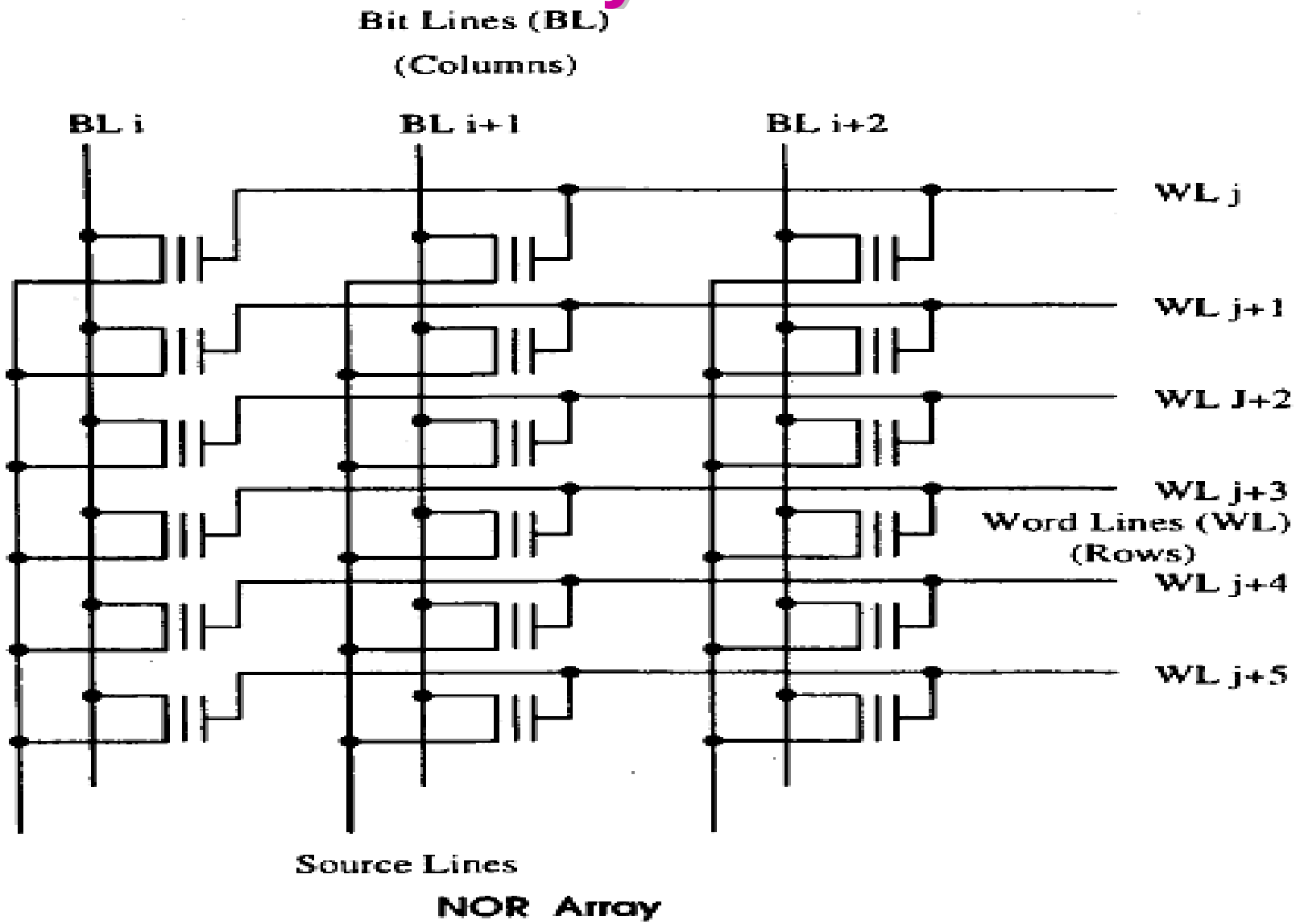




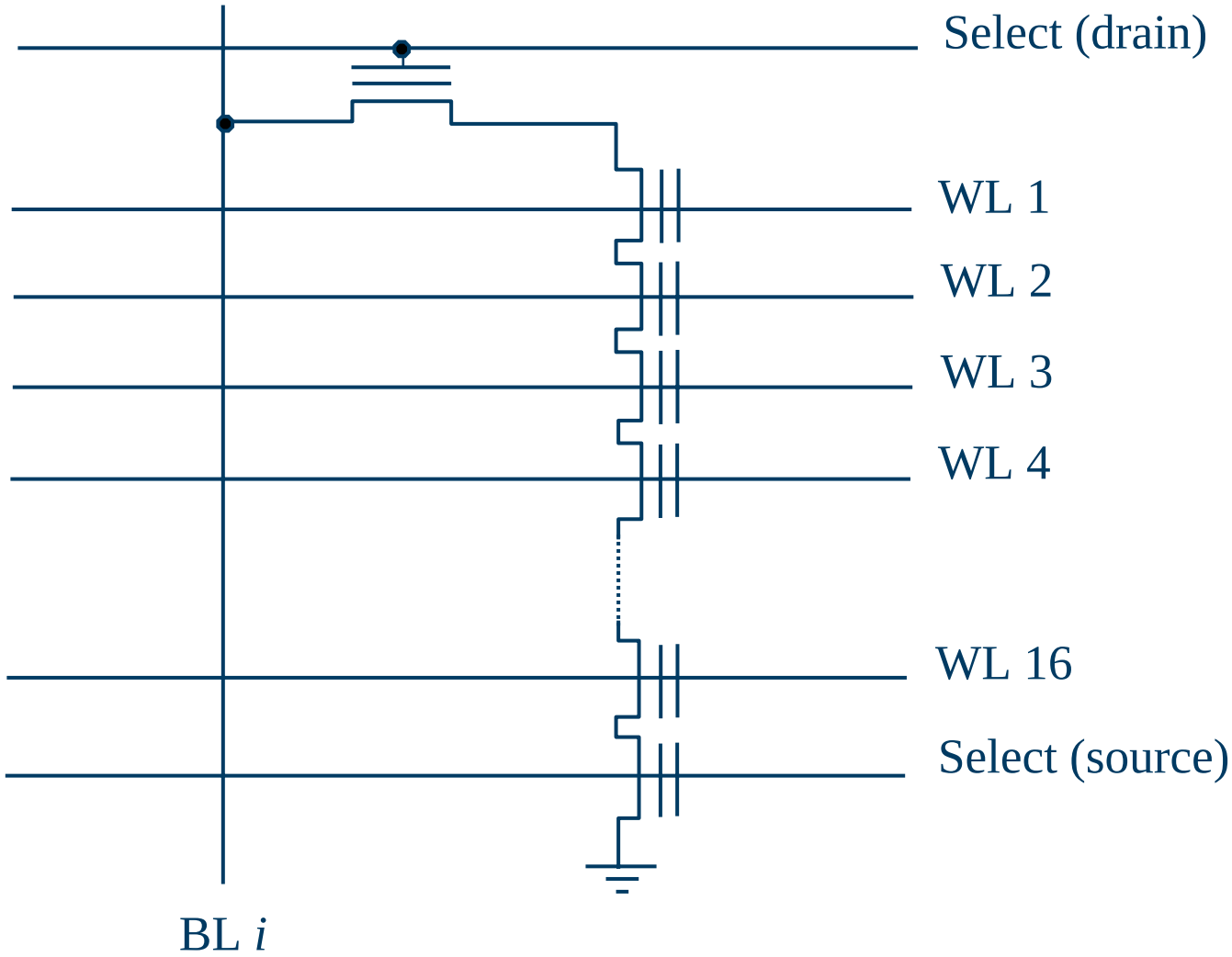


- Operations: Read, Program, Erase (Flash Erase)
  - As opposed to Read and Write in RAM

NOR-Array Structure

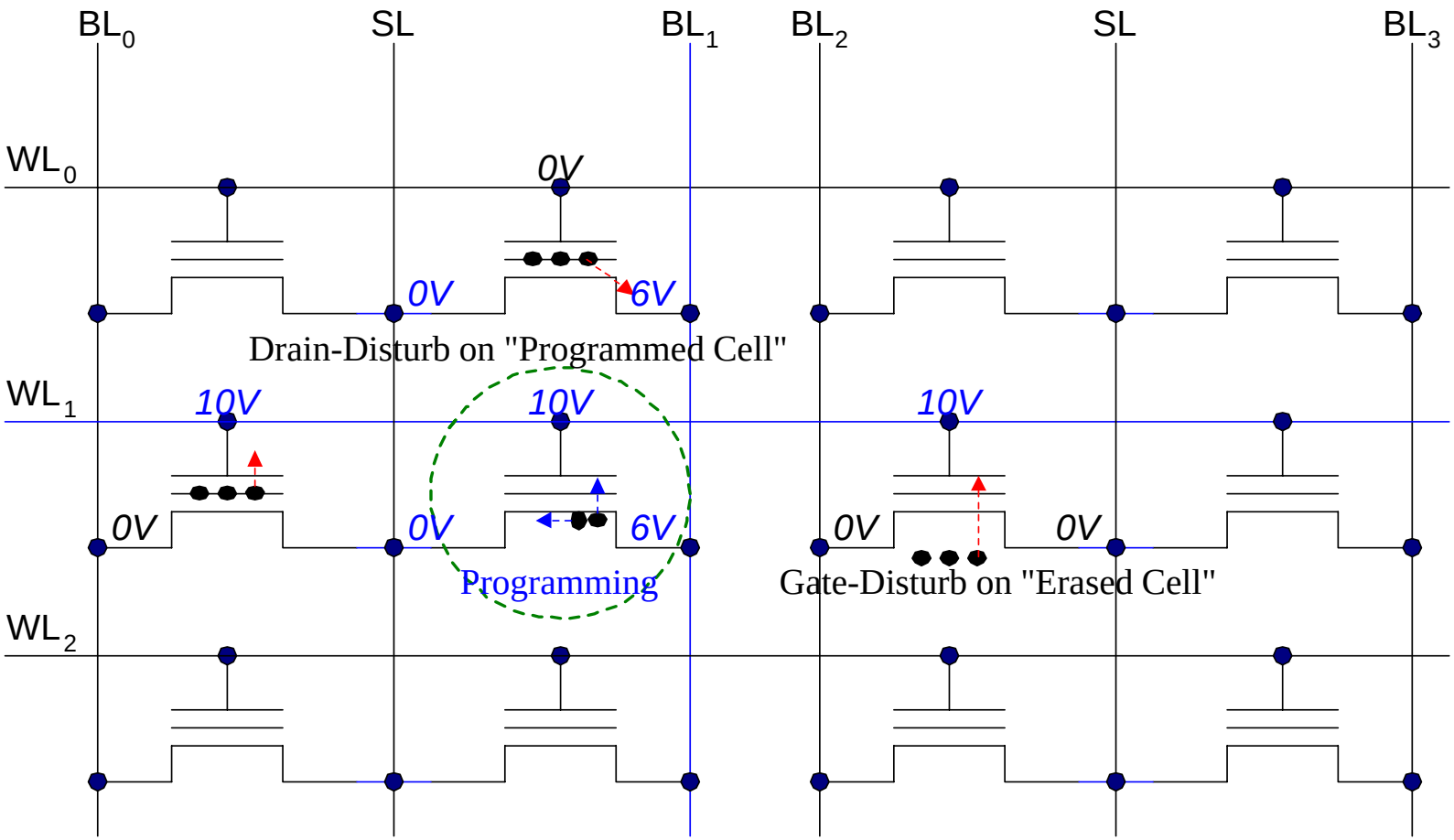


NAND-Array Structure



Disturbance Example (I)

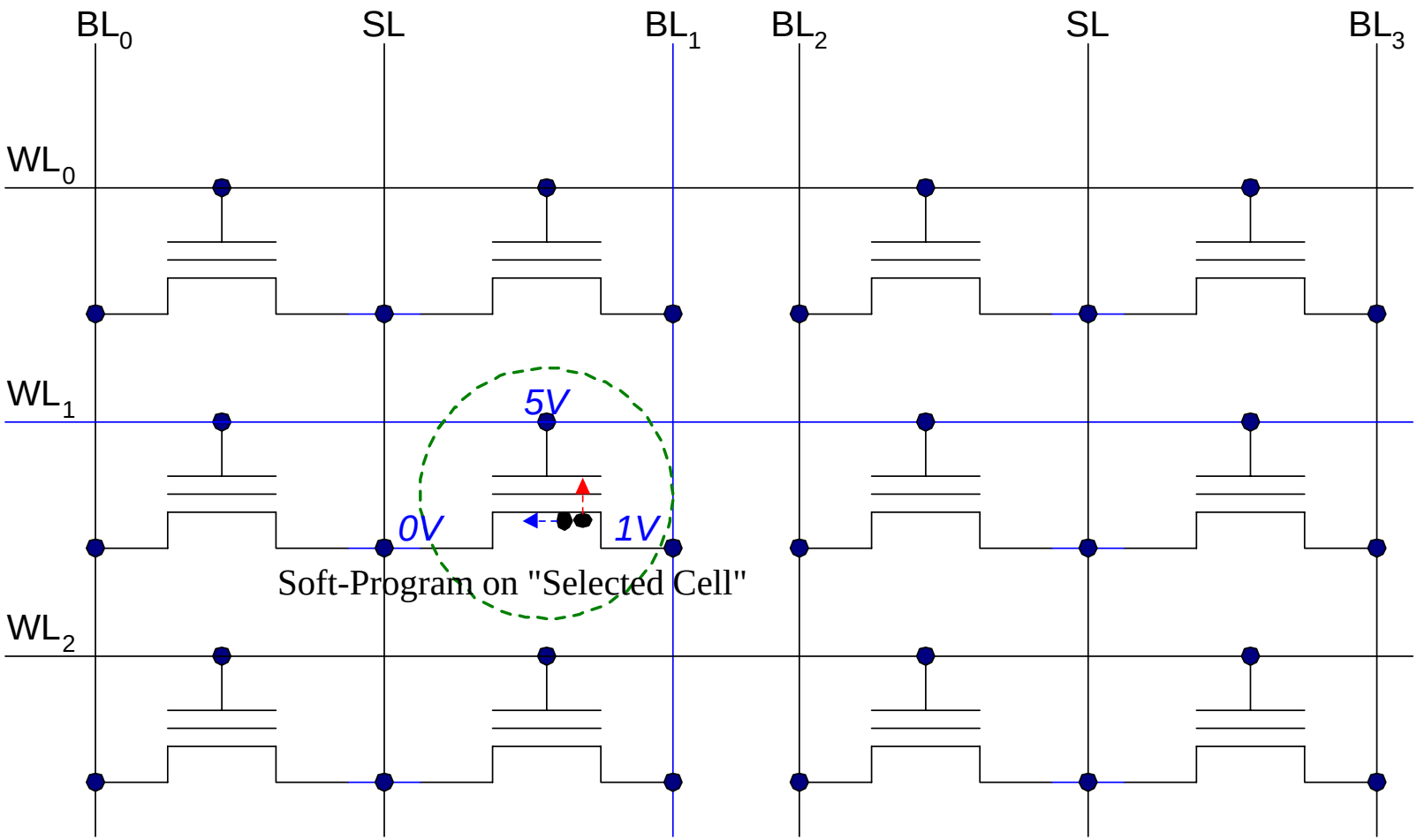
Program Disturbance



NOR-Type Common Ground – Standard (Stacked Gate)

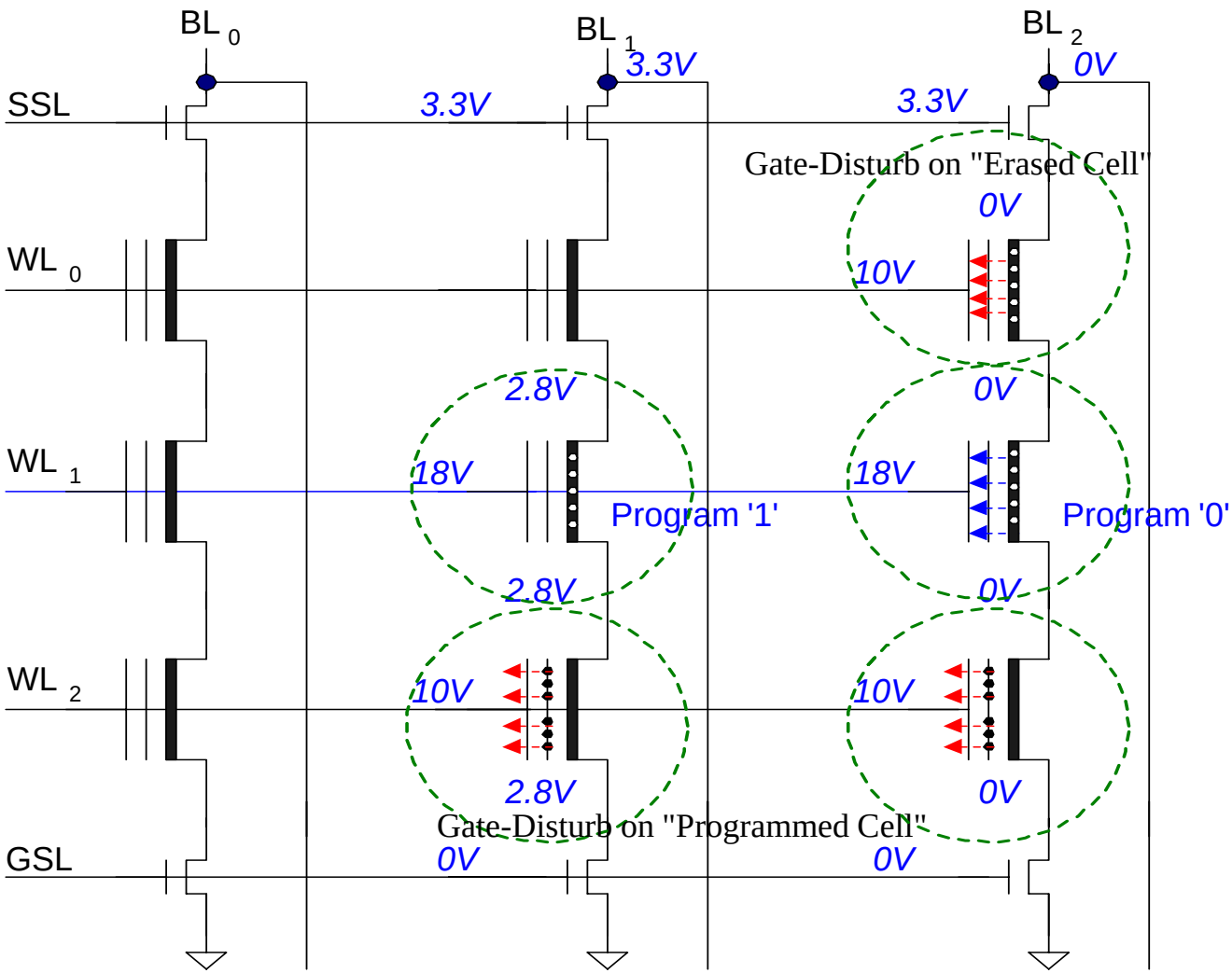
Disturbance Example (II)

Read Disturbance



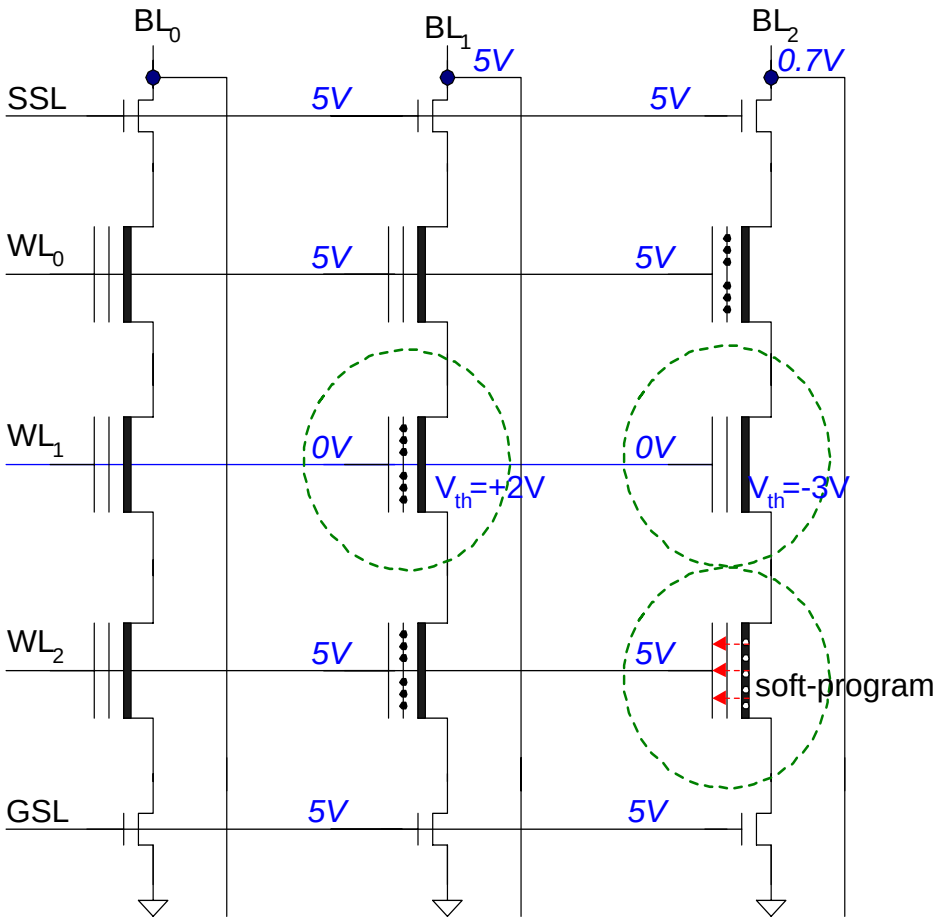
Disturbance Example (III)

Program Disturbance

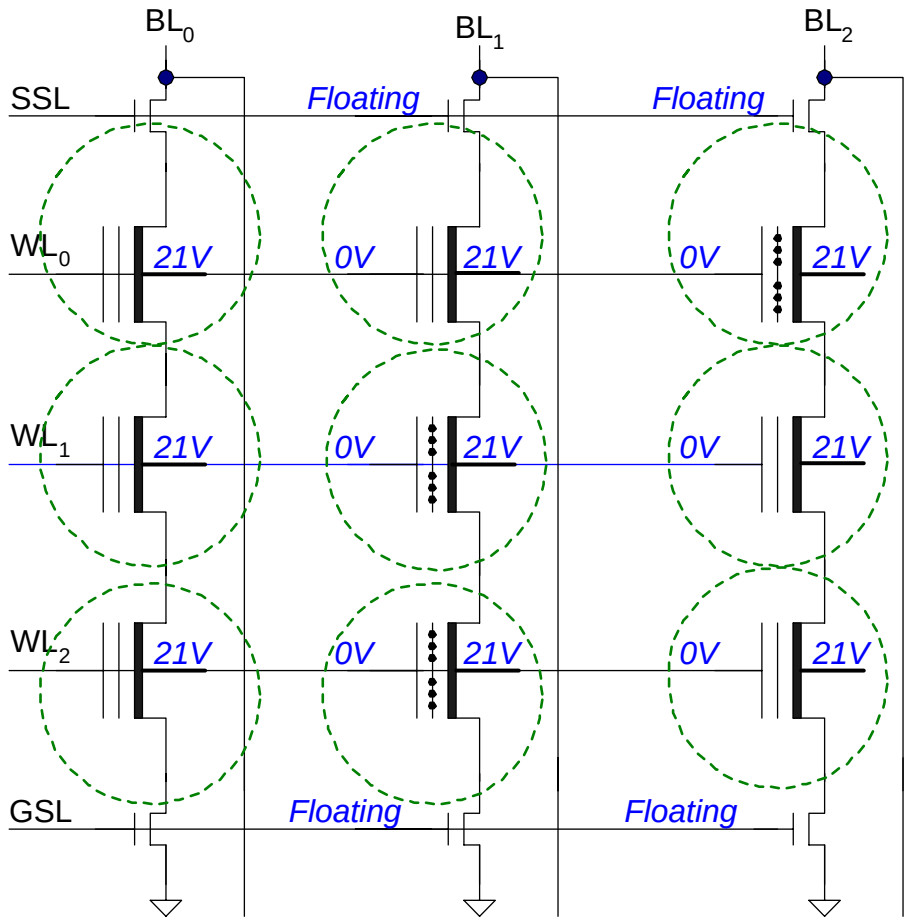


Disturbance Example (IV)

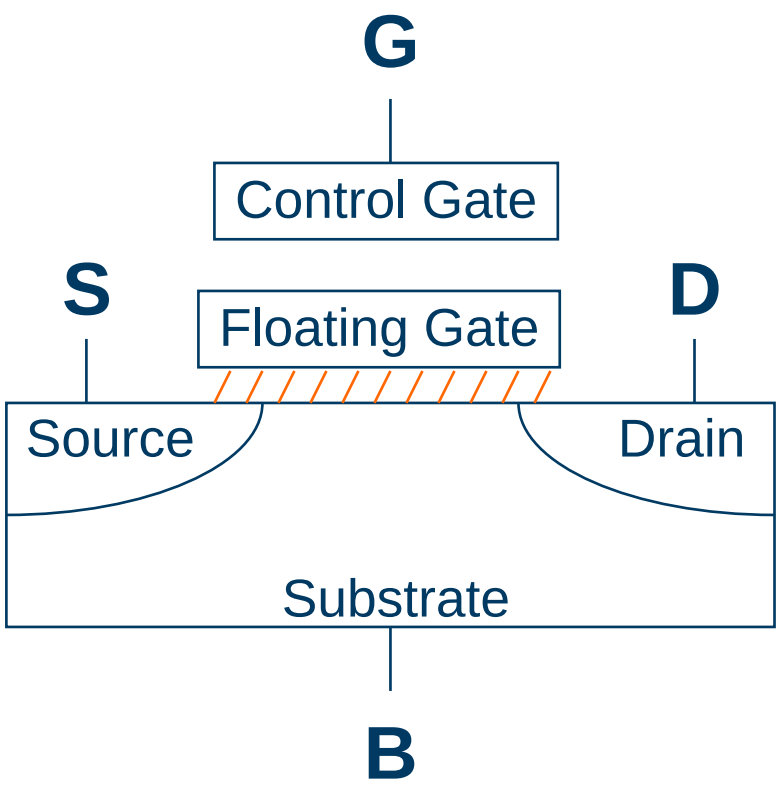
Read Disturbance



Erase Disturbance



Word-Line Program Disturb Fault (WPDF)

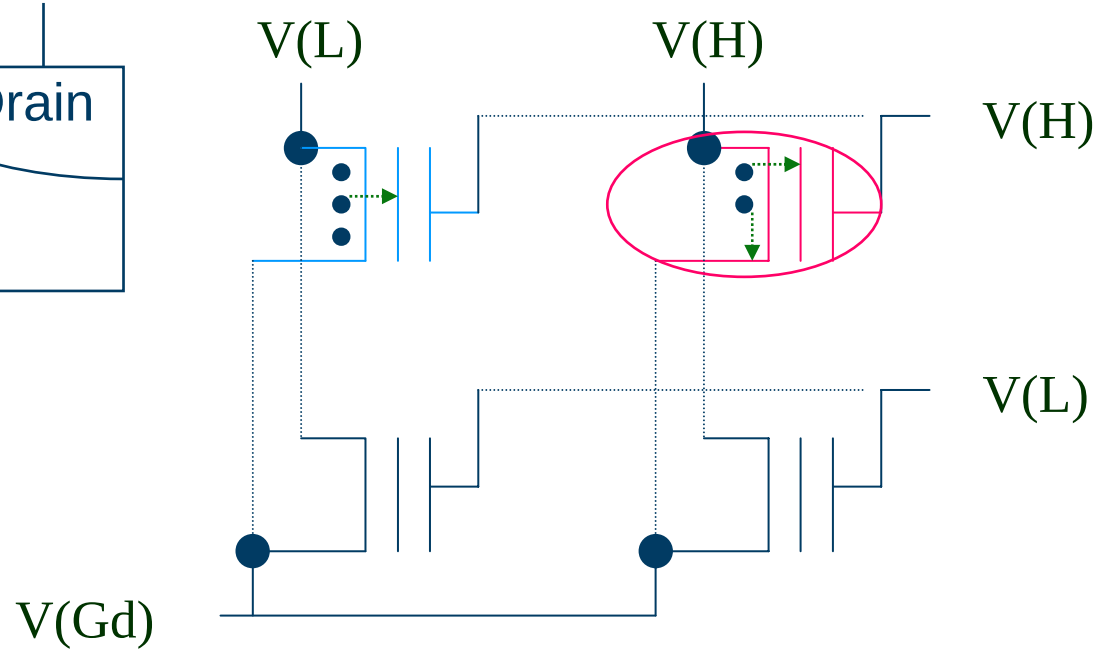


Conditions:

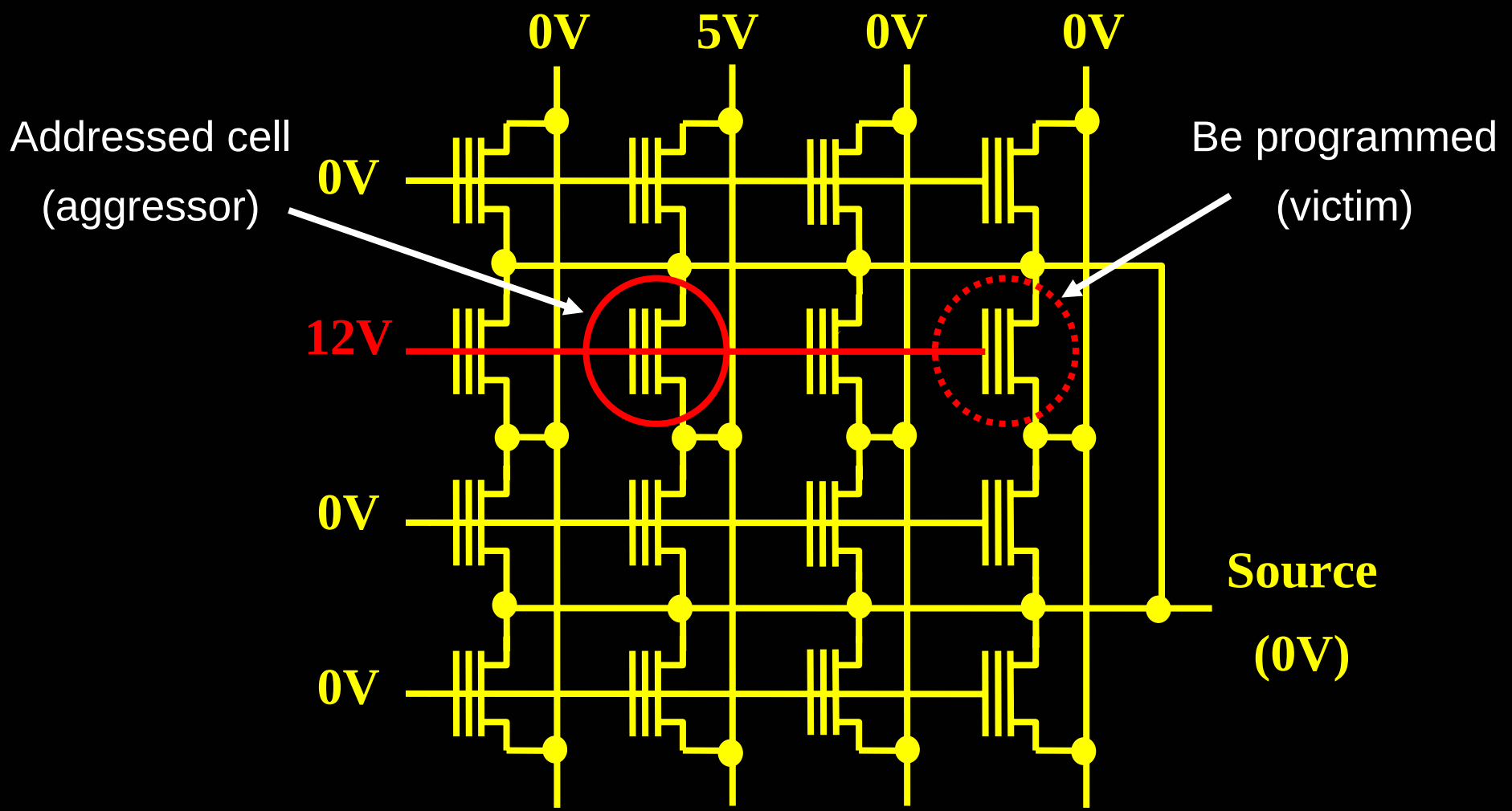
1.Victim cell initial value is a logic '1'

2.Aggressor "1→0" (program)

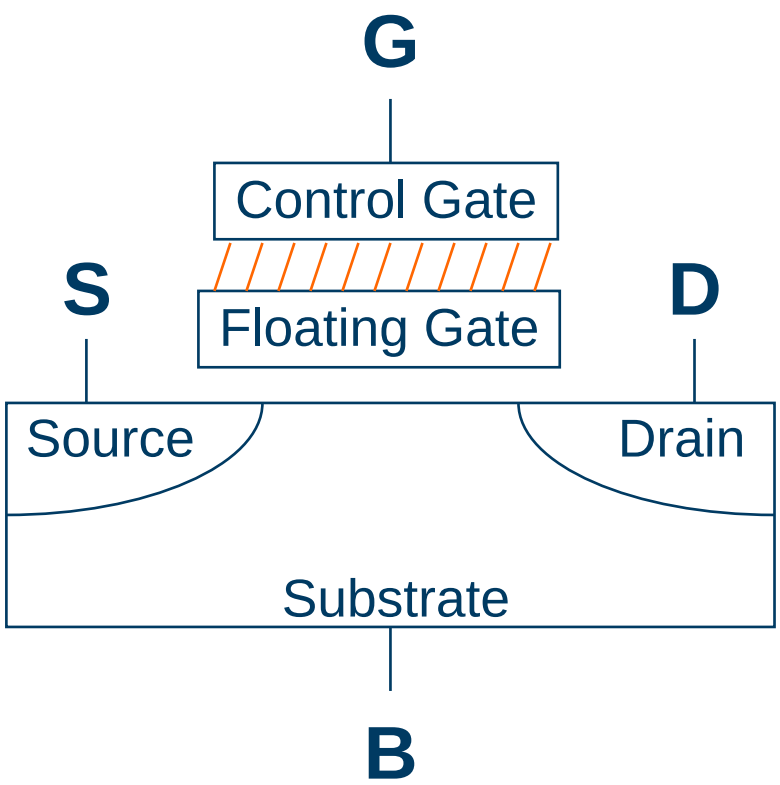
Victim "1→0" (program)



WPDF

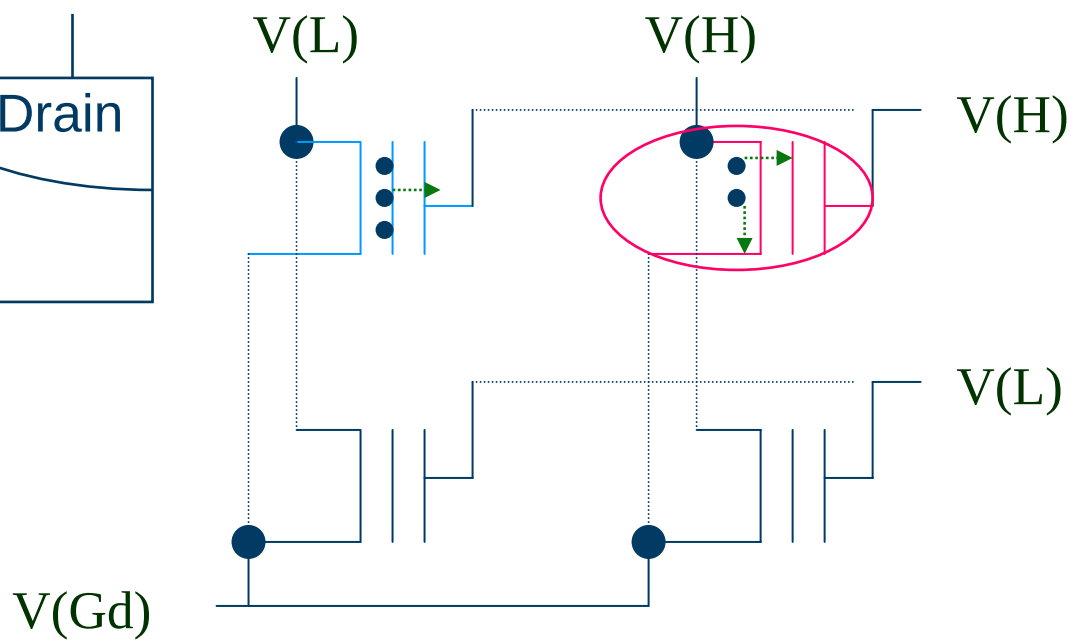

0V
5V
0V
0V
Addressed cell
(aggressor)
Be programmed
(victim)
0V
12V
0V
0V
Source
(0V)

Word-Line Erase Disturb Fault (WEDF)

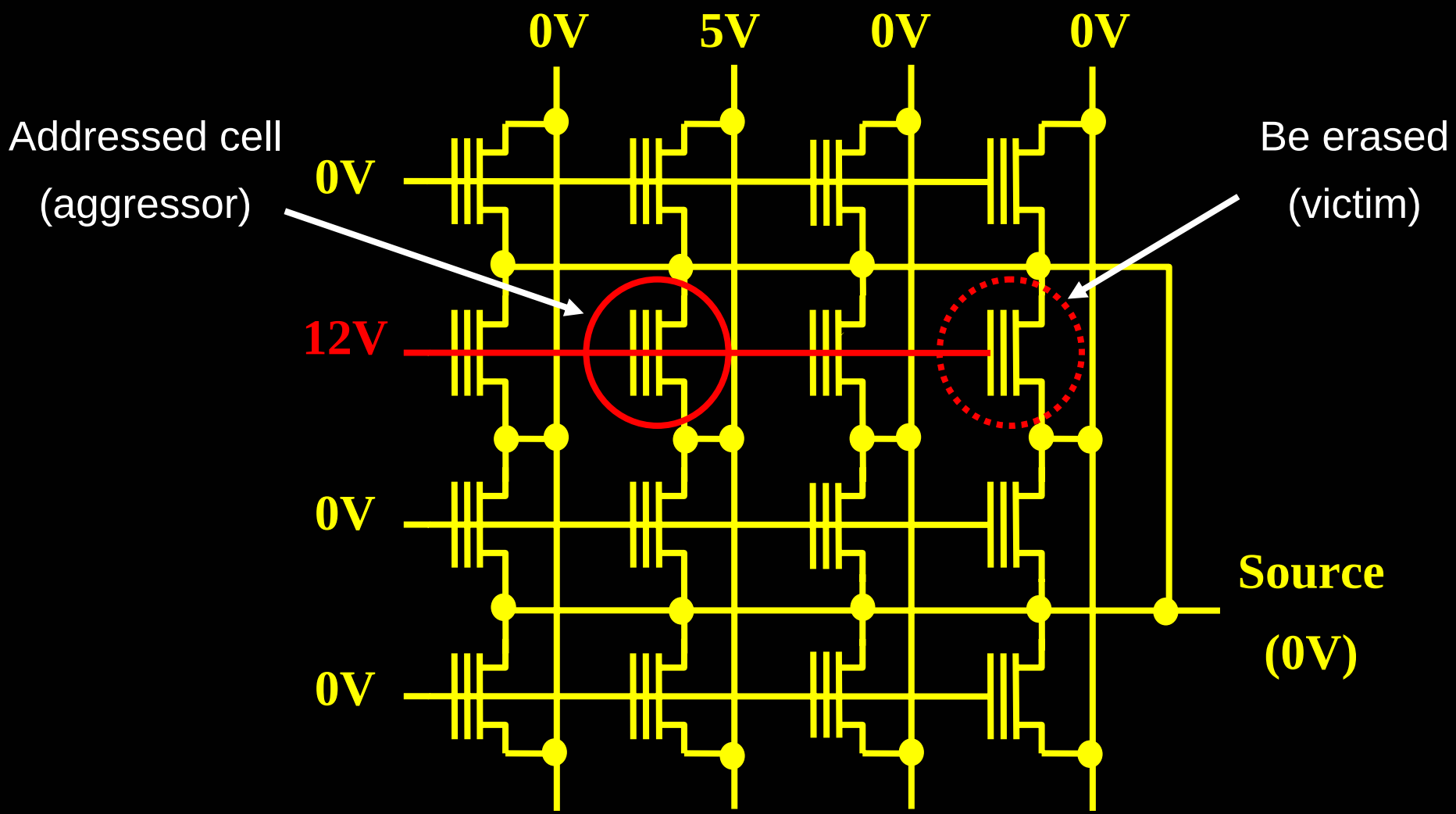


Conditions:

1. Victim cell initial value is a logic '0'
2. Aggressor "1→0" (program)
   Victim "0→1" (erase)



WEDF


0V
5V
0V
0V
Addressed cell
(aggressor)
0V
Be erased
(victim)
12V
0V
Source
(0V)
0V

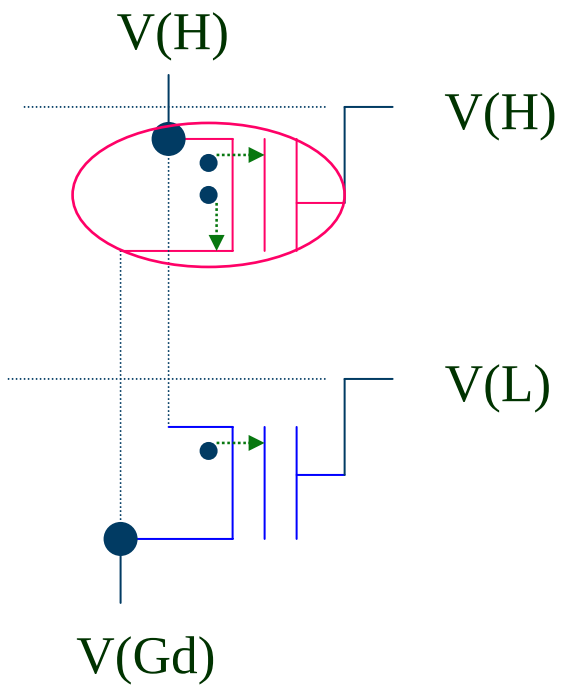
Bit-Line Program Disturb Fault (BPDF)

Conditions:

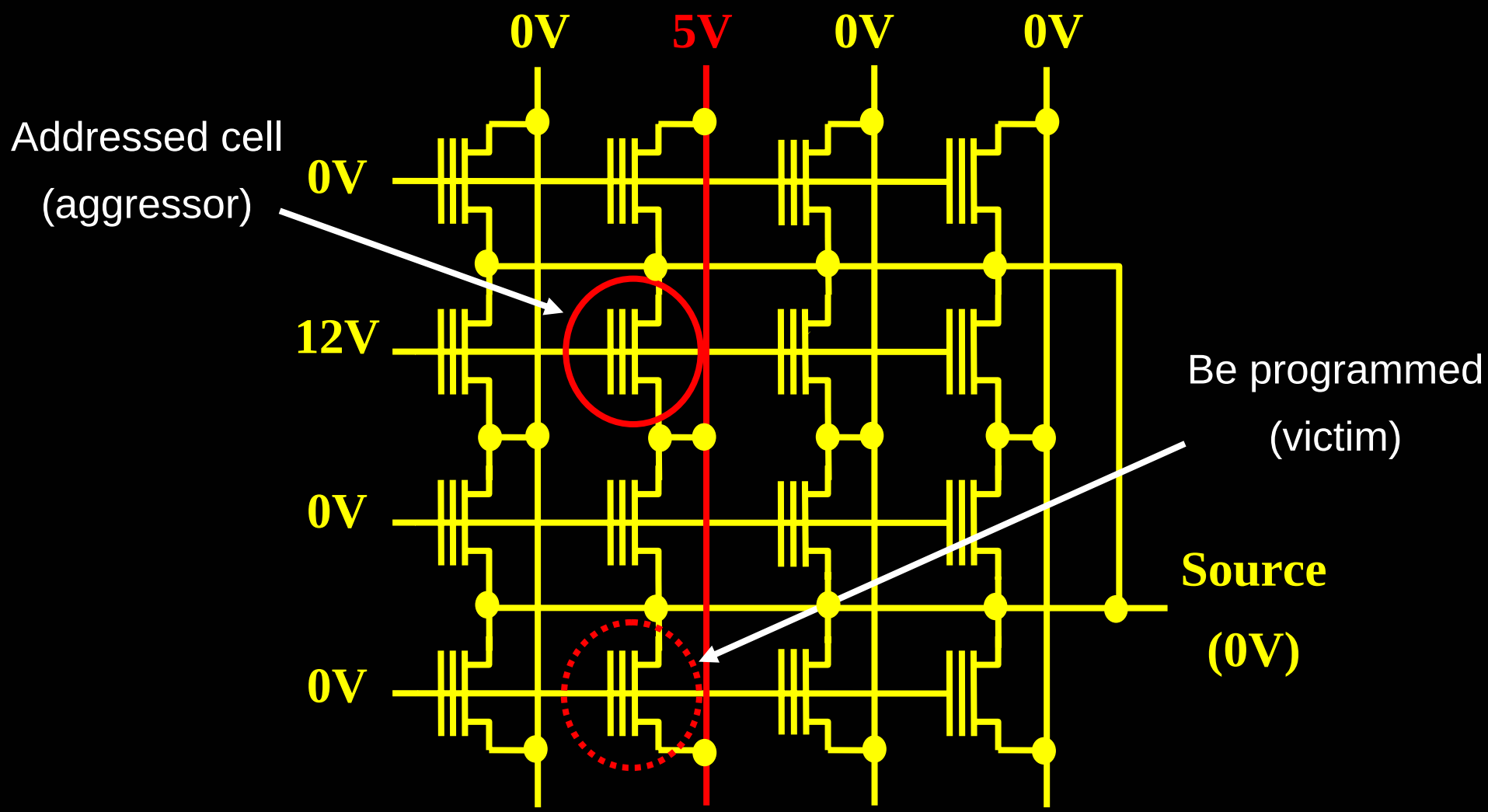
1.Victim cell initial value is a logic '1'

2.Aggressor "1→0" (program) Victim "1→0" (program)

- During programming, erased cells on unselected rows on a bit-line that is being programmed may have a fairly deep depletion region formed under them
- Electrons entering this depletion region can be accelerated by the electric field and injected over the oxide potential barrier to adjacent floating gates



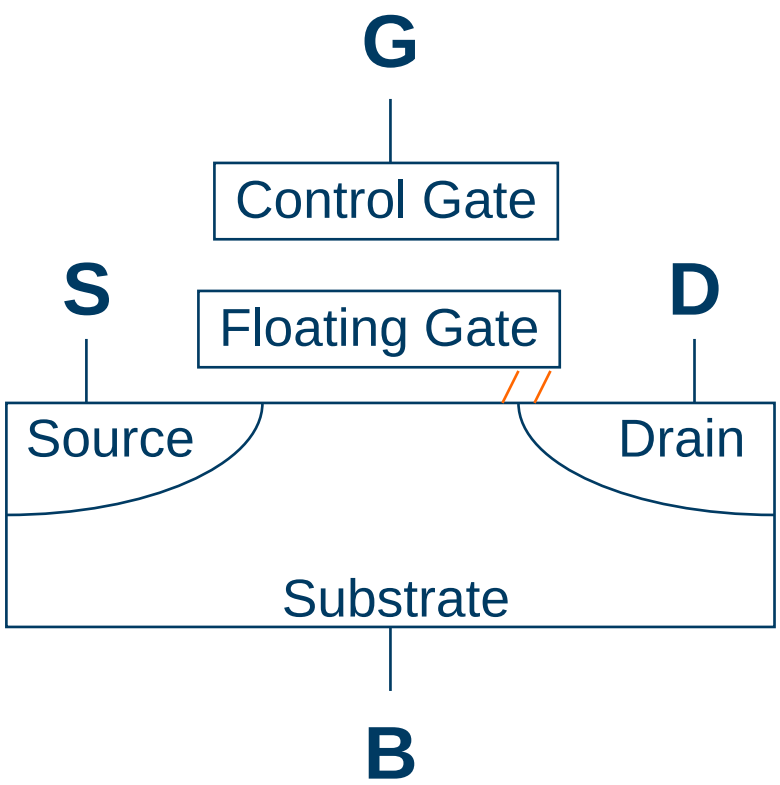
BPDF

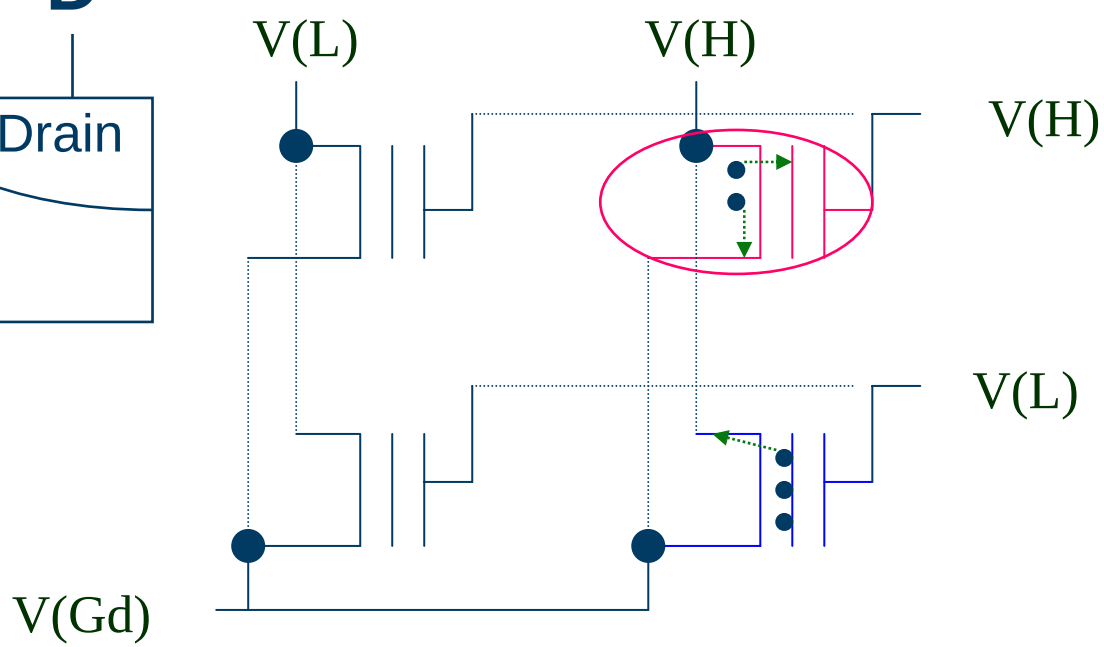

0V
5V
0V
0V
Addressed cell
(aggressor)
0V
12V
0V
0V
Be programmed
(victim)
Source
(0V)

Bit-Line Erase Disturb Fault (BEDF)

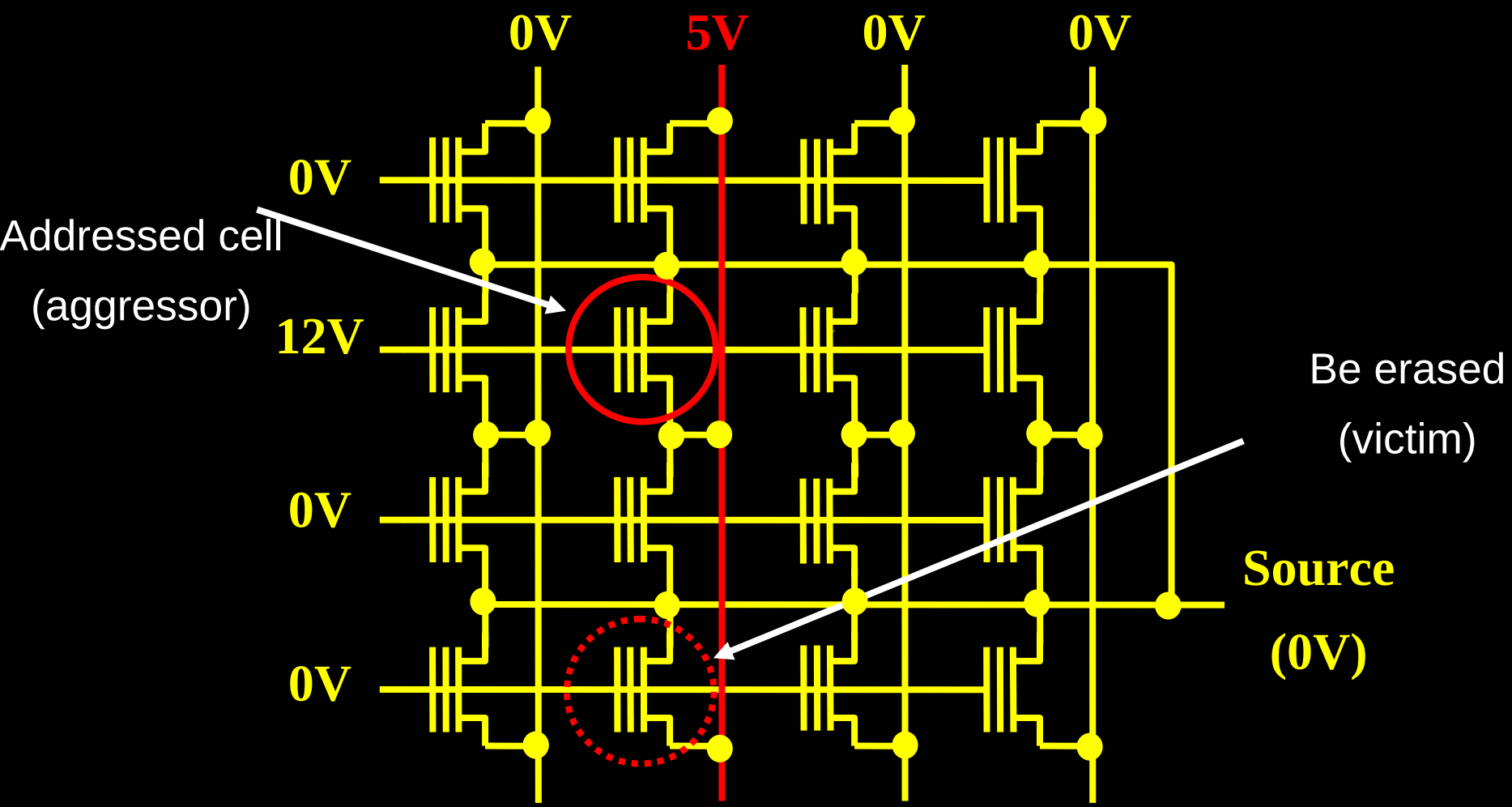
Conditions:

1. Victim cell initial value is a logic '0'
2. Aggressor "1→0" (program)
   Victim "0→1" (erase)





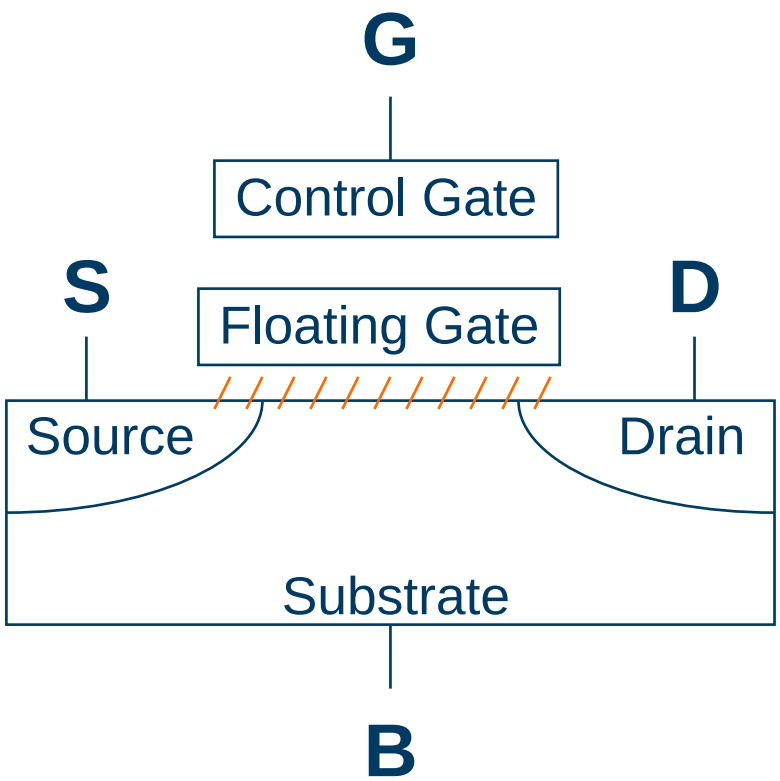
BEDF


0V
5V
0V
0V
0V
12V
0V
0V
Addressed cell
(aggressor)
Be erased
(victim)
Source
(0V)

Excitation Requirements

Fault Model	Initial Content	Excitation Operation	Faulty Value	Faulty Cell Location
WPD	1	Program (w0)	0	Word-line
WED	0	Program (w0)	1	Word-line
BPD	1	Program (w0)	0	Bit-line
BED	0	Program (w0)	1	Bit-line

Read Disturb Fault (RDF)



Conditions:

1. Occurs on the selected cell
2. Cell initial value is '1' or '0'

- Soft program: After repeated read operations, hot carriers can be injected from the channel into the FG even if at low gate voltages
- Soft erase: The selected cell is unable to maintain the state 0 after repeated reads, due to charge leakage on the FG

Over Erase Fault (OEF)

- Flash memory erase mechanism is not self-limiting
- Threshold voltage can be low enough to turn the cell into a depletion-mode transistor
- Fault behavior:
  - An unselected cell in the same bit-line has excessive source-drain leakage current; reading that cell leads to incorrect value (like DEDF)
  - Cannot be programmed correctly (like TF)

Basic RAM Faults for Flash Memory

- Address-Decoder Fault (AF)
- Stuck-At Fault (SAF)
- Transition Fault (TF)
- Stuck-Open Fault (SOF)
- Bridging Fault (BF)

➢ Coupling faults need not be considered!

  ➢ Replaced by disturb faults

Reliability Consideration

- Reliability characteristics of floating-gate ICs depend on
  - Circuit density, circuit design, and process integrity
  - Memory array type and cell structure
- Reliability stressing and testing must then be oriented toward determining the relevant failure rates for the particular array under consideration

Data Retention Fault

- Retention time: the time from data storage to the time at which a verifiable error is detected from any cause
  - Intrinsic retention times exceed millions of years in the operating temperature range
    - Months at 300°C
    - 1 million years at 150 °C
    - 120 million years at 55 °C
- Data Retention Fault (DRF)
  - Static leakage
  - Built-in data retention test circuit

Cell Endurance Fault

- Endurance: a measure of the ability to meet data-sheet specifications as a function of accumulated program/erase cycles
  - Endurance limit is a result of damage to the dielectric around the floating gate caused by electric stresses
  - In many flash devices, the end of endurance is generally caused by hot electron trapping in the charge transport oxide
- Cell Endurance Fault (CEF)
  - Threshold window shift due to increased program/erase cycles
  - Built-in stress test circuit

Composite Failure Rate Determination

- 125°C dynamic life stress
  - The 125°C dynamic life stress is the standard MOS memory continuous dynamic read in a burn-in chamber
- Endurance test
  - The endurance test is the repeated data complementing of floating-gate devices, possibly at temperature extremes
- Extended data retention stress
  - This test is constituted by a high-temperature bake with a charge polarity that is opposite to the equilibrium state on the floating gate

Testing WPDF

1. Flash
2. Program the first column
3. Read all cells except the first column
4. Flash
5. Program any column except the first
6. Read the first column

*Assume reading and programming are done column-wise

Source: Saluja, *et al.*, Int. Conf. VLSI Design, 2000

Testing WEDF

1. Flash
2. Program all cells
3. Read all cells except the last column
4. Program any column except the last
5. Read the last column

*Assume reading and programming are done column-wise

Source: Saluja, *et al.*, Int. Conf. VLSI Design, 2000

Test Coverage: Previous Results

Fault	DCP	DCE	DD	EF	GF
SAF	50%	50%	50%	100%	100%
TF	12.5%	50%	50%	87.5%	62.5%
AF	40%	0%	0%	44.5%	40%
SOF	0%	0%	0%	12.5%	6.2%
CFst	25%	25%	25%	50%	50%
WPDF	33.3%	0%	0%	100%	33.3%
WEDF	0%	100%	75%	100%	100%
BEDF	0%	75%	100%	100%	100%
BPDF	0%	0%	0%	0%	0%

Source: Saluja, *et al.*, Int. Conf. VLSI Design, 2000

March-Based Flash Test: March-FT

- {(f); ⇓(r1,w0,r0); ⇓(r0); (f); ⇑(r1,w0,r0); ⇑(r0)}

This flash memory is of NOR type (stacked gate).

Memory size (N) : 65536

Test length : 2(chip erase time) + 131072(word program time) + 393216(word read time)

Test time : 7.207173 sec

SAF : 100%	(131072 / 131072)
TF : 100%	(131072 / 131072)
SOF : 100%	(65536 / 65536)
AF : 100%	(4294901760 / 4294901760)
CFst : 100%	(17179607040 / 17179607040)
WPD : 100%	(16711680 / 16711680)
WED : 100%	(16711680 / 16711680)
BPD : 100%	(16711680 / 16711680)
BED : 100%	(16711680 / 16711680)
RD : 100%	(65536 / 65536)
OE : 100%	(65536 / 65536)

P.S.

Flash Type = NOR

Gate Type = Stack

Row Number = 256

Col Number = 256

Word Length = 1

Chip erase time = 3 sec

Word program time = 9u sec

Word read time = 70n sec

Ref: DELTA02

Test Length (Bit-Oriented)

- Notation:
  - F : Flash time
  - P : Program time
  - R : Read time
  - r : row number
  - c : column number

DCP	2(F) + **2r**(P) + rc(R)
DCE	(F) + **(c+1)r**(P) + rc(R)
DD	(F) + **(r+1)c**(P) + rc(R)
EF	2(F) + **(rc+2r+c-2)**(P) + (2rc+r+c-3)(R)
GF	2(F) + **(rc+2r+c-1)**(P) + (2rc+c+r-2)(R)
FT	2(F) + **2rc**(P) + 6rc(R)

Test Length (Word-Oriented)

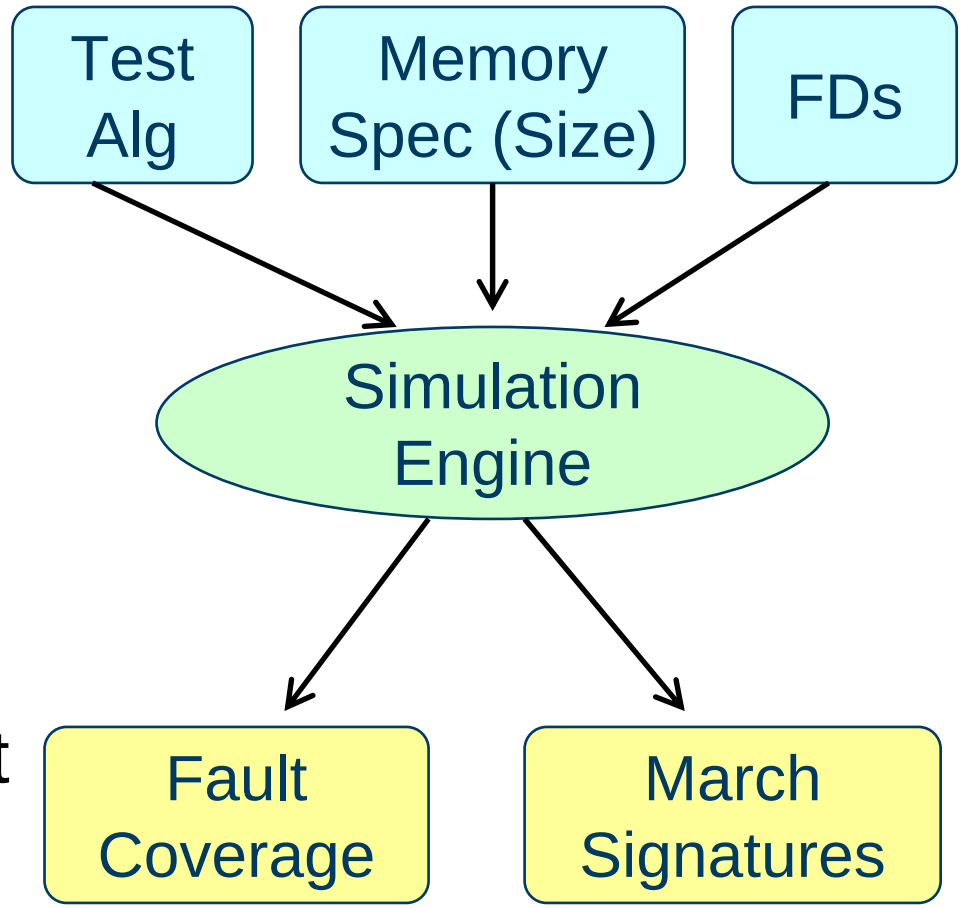
- Word length = w:
  - $2(F)+2rc(P)+6rc(R)+\log(w)[2(F)+rc(P)+rc(R)]$

    solid background testing time

    standard background testing time
  - Solid: 0000 (1111)
  - Standard: 0101 (1010), 0011 (1100)
- Ex: word length w = 4
  - 6(F) + 4rc(P) + 8rc(R)

RAMSES-FT: Fault Simulator

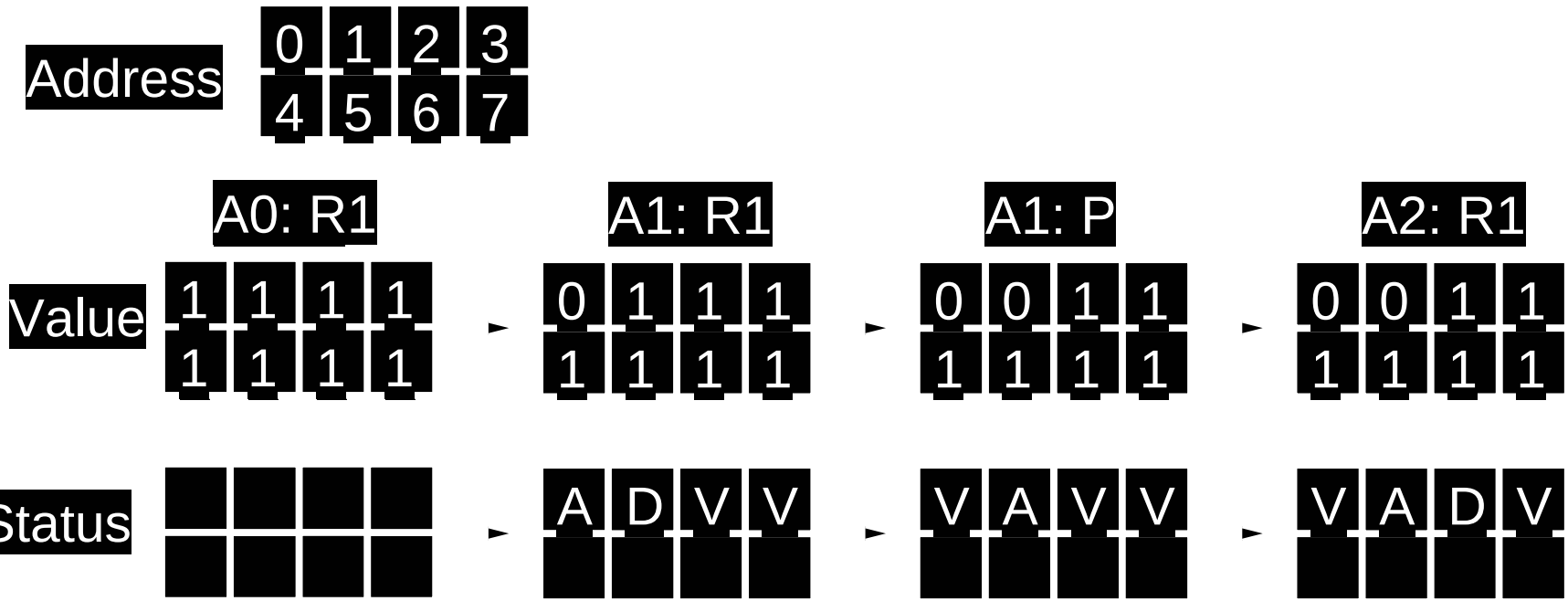
- Extended from RAMSES (for RAM)
- Fault descriptors:
  - AGR: aggressor
  - SPT: suspect
  - VTM: victim
  - RCV: recoverer
- Fault coverage report and March Signature generation



Ref: VTS02

Fault Simulation Example

- Example: WPD
  - AGR: P, SPT: w, VTM: R1, RCV: P or E
  - March-like element: ⇑ **(R1, P)**

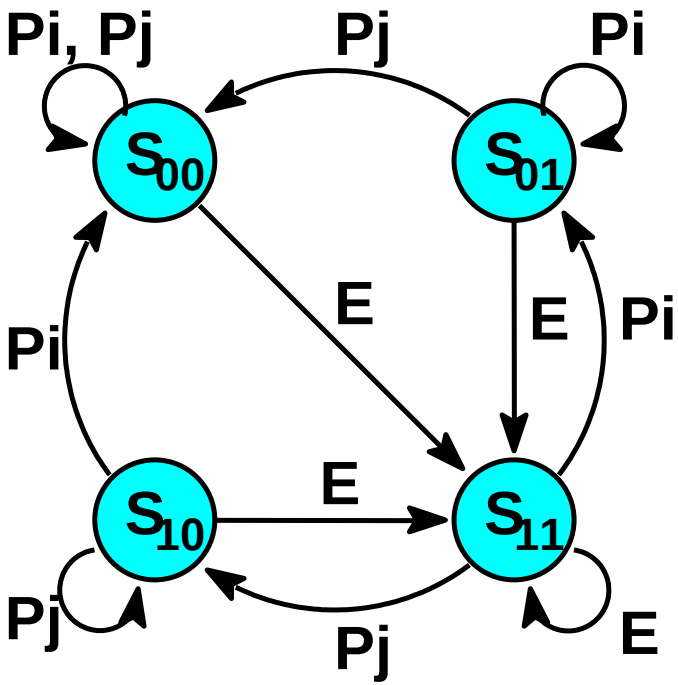


Diagnostic Algorithm

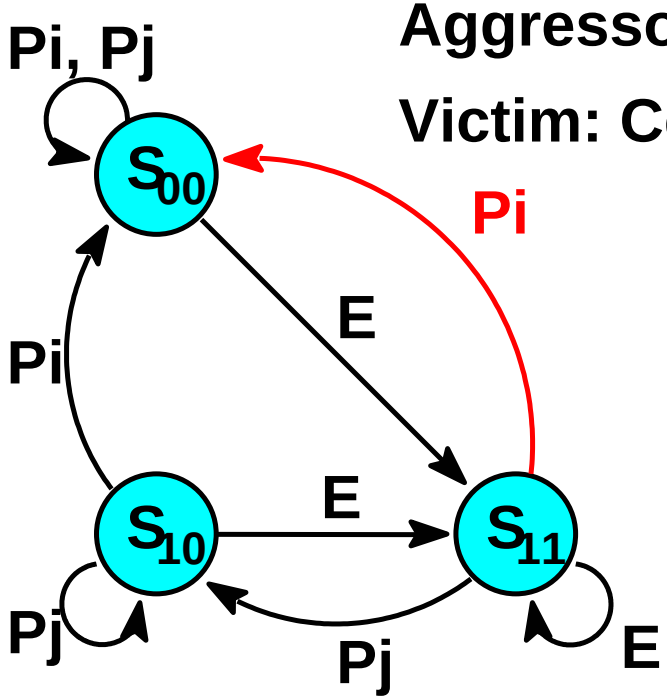
- March signature
- March-FD: $E;\Uparrow(R1);\Uparrow(R1,P,R0);E;\Uparrow(R1);\Downarrow(R1,P,R0,R0);\Uparrow(R0,P);\Uparrow(R0);$

(000010000011101)	TF(D), SAF(1)
(000000000000100)	WED_S, BED_S
(000000000000001)	WED_L, BED_L
(001000000000000)	WPD_S, BPD_S, AF_S, $CFst(0;1/0)_S$
(000000010000000)	WPD_L, BPD_L, AF_L, $CFst(0;1/0)_L$

State Transition Diagram



Fault free cells

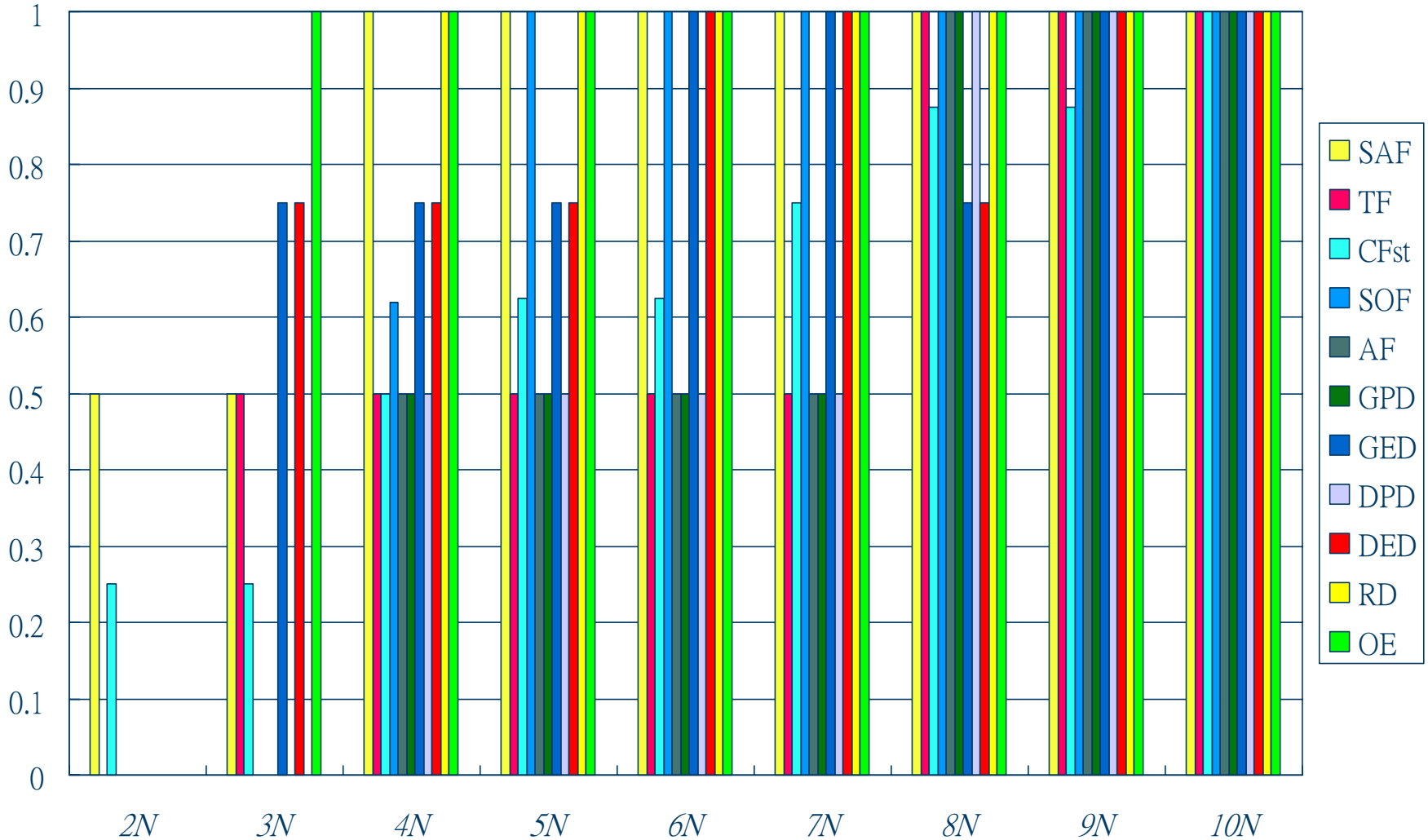


Faulty cells
(AFs, CFst(0;1/0)s, WPDs, BPDs)

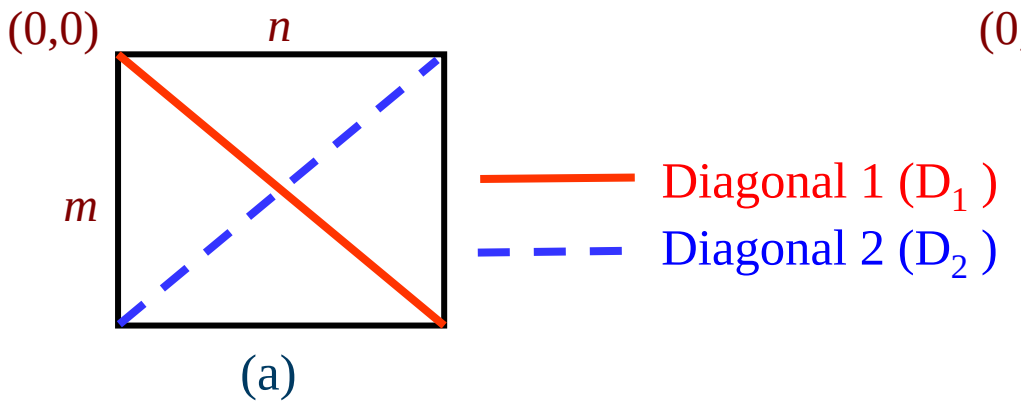
Test Algorithm Generation by Simulation (TAGS)

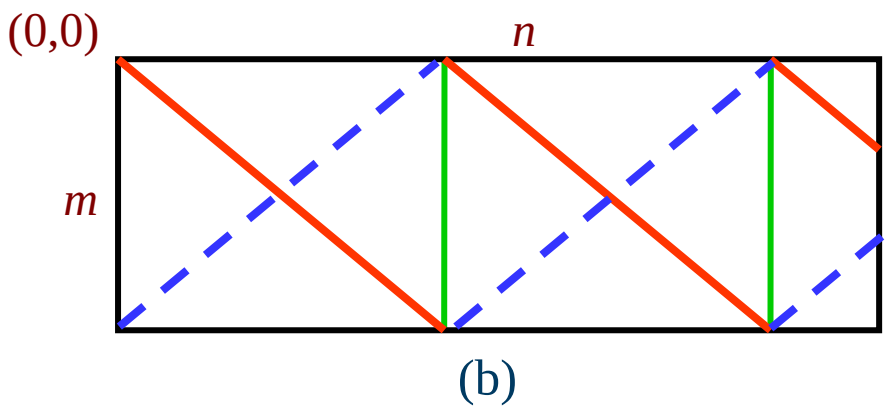
T(N)	Test algorithms
2N	(f); ⇓(r1)
3N	(f); ⇓(w0); ⇓(r0)
4N	(f); ⇓(r1,w0); ⇓(r0)
5N	(f); ⇓(r1,w0,r0); ⇓(r0)
6N	(f); ⇓(r1,w0,r0); ⇓(r0,w0)
7N	(f); ⇓(r0); ⇓(r1,w0,r0); ⇓(r0,w0)
8N	(f); ⇓(r1,w0); (f); ⇑(r1,w0,r0); ⇓(r0)
9N	(f); ⇓(r1,w0); ⇓(r0); (f); ⇑(r1,w0,r0); ⇓(r0)
10N	(f); ⇓(r1,w0,r0); ⇑(r0); (f); ⇑(r1,w0,r0); ⇓(r0)

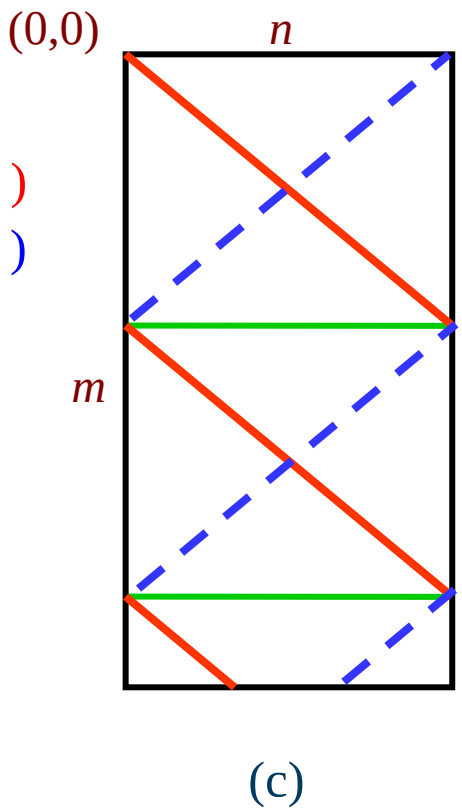
RAMSES-FT Results for TAGS



Diagonal Test Scheme



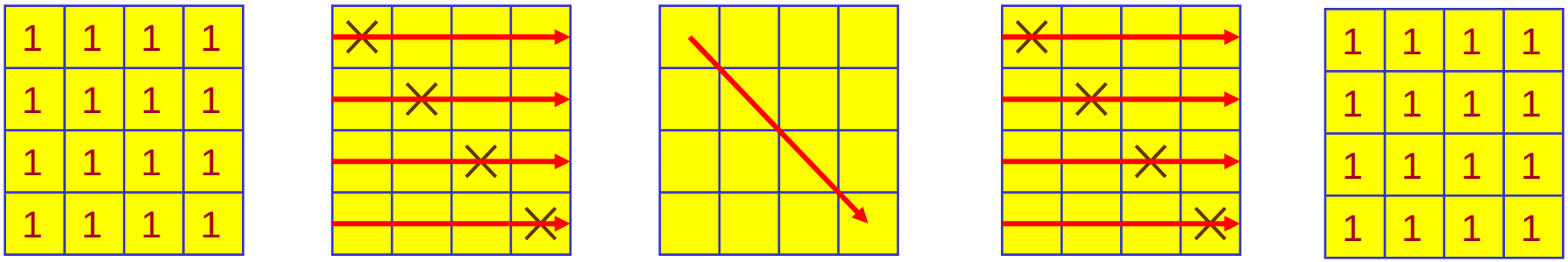




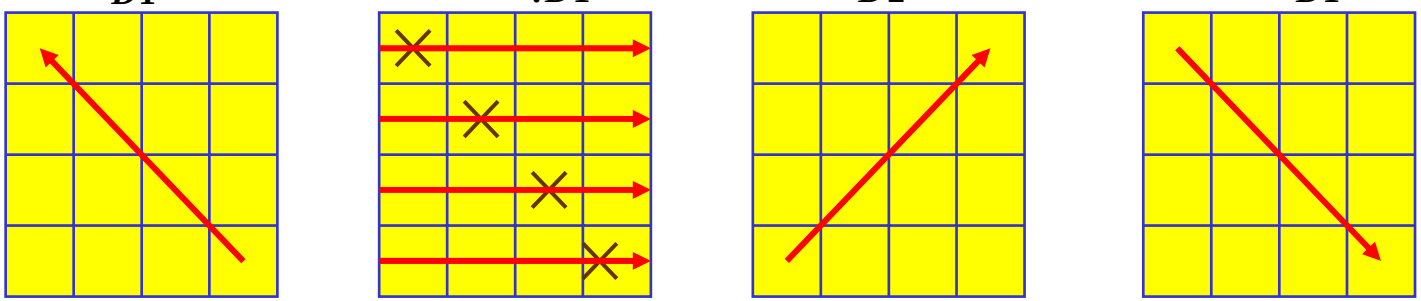
Ref: ITC02

Diagonal Flash Test

Step 1: Flash Erase **Step 2:** $\Uparrow_{!D1}(R1,P,R0)$ **Step 3:** $\Uparrow_{D1}(R1,P,R0)$ **Step 4:** $\Uparrow_{!D1}(R0)$ **Step 5: Flash Erase**



Step 6: $\Downarrow_{D1}(R1,P,R0)$ **Step 7:** $\Uparrow_{!D1}(R1)$ **Step 8:** $\Downarrow_{D2}(R1,P,R0)$ **Step 9:** $\Uparrow_{D1}(R0)$



$$Diagonal-FT:\left\{\begin{array}{l}(E);\ \Uparrow_{!D1}(R1,P,R0);\ \Uparrow_{D1}(R1,P,R0);\ \Uparrow_{!D1}(R0);\\ (E);\ \Downarrow_{D1}(R1,P,R0);\ \Uparrow_{!D1}(R1)\ \Downarrow_{D2}(R1,P,R0);\ \Uparrow_{D1}(R0)\end{array}\right\}$$

Flash Memory Fault Diagnosis

- March-FD Algorithm:

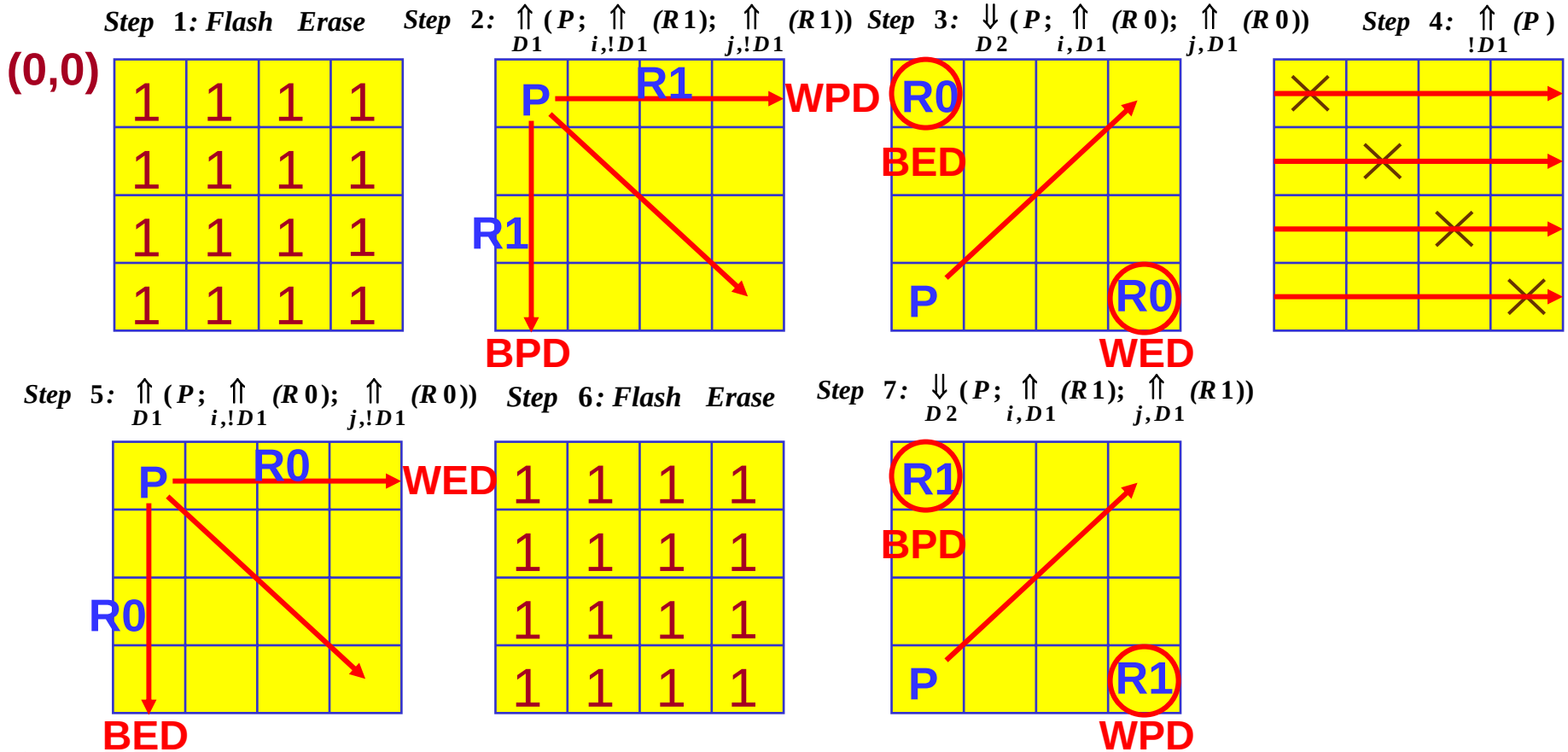
$$\left\{\begin{array}{l}(E);\Uparrow(R1);\Uparrow(R1,P,R0);(E);\Uparrow(R1);\\ \Downarrow(R1,P,R0,R0);\Uparrow(R0,P);\Uparrow(R0)\end{array}\right\}$$

Time complexity: 2e + (3N)p + (9N)r

- Indistinguishable faults and their signatures for March-FD

March Signatures	Indistinguishable faults
(00001000011101)	TF(D),SAF(1)
(00000000000100)	WED_S, BED_S
(00000000000001)	WED_L, BED_L
(00100000000000)	WPD_S, BPD_S, AF_S, $CFst(0;1/0)_S$
(00000001000000)	WPD_L, BPD_L, AF_L, $CFst(0;1/0)_L$

Diagonal Flash Diagnosis (Diagonal-FD)



$$\{(E);\ \Uparrow_{D1}(P;\ \Uparrow_{i,!D1}(R1);\ \Uparrow_{j,!D1}(R1));\ \Downarrow_{D2}(P;\ \Uparrow_{i,D1}(R1);\ \Uparrow_{j,D1}(R1));\ \Uparrow_{!D1}(P);$$
$$\Uparrow_{D1}(P;\ \Uparrow_{i,!D1}(R0);\ \Uparrow_{j,!D1}(R0));\ (E);\ \Downarrow_{D2}(P;\ \Uparrow_{i,D1}(R0);\ \Uparrow_{j,D1}(R0))\}$$

Fault Simulation: Test Time

- Fault simulator: RAMSES-FT
- DUT: industrial 2Mb (256K×8) flash memory core.

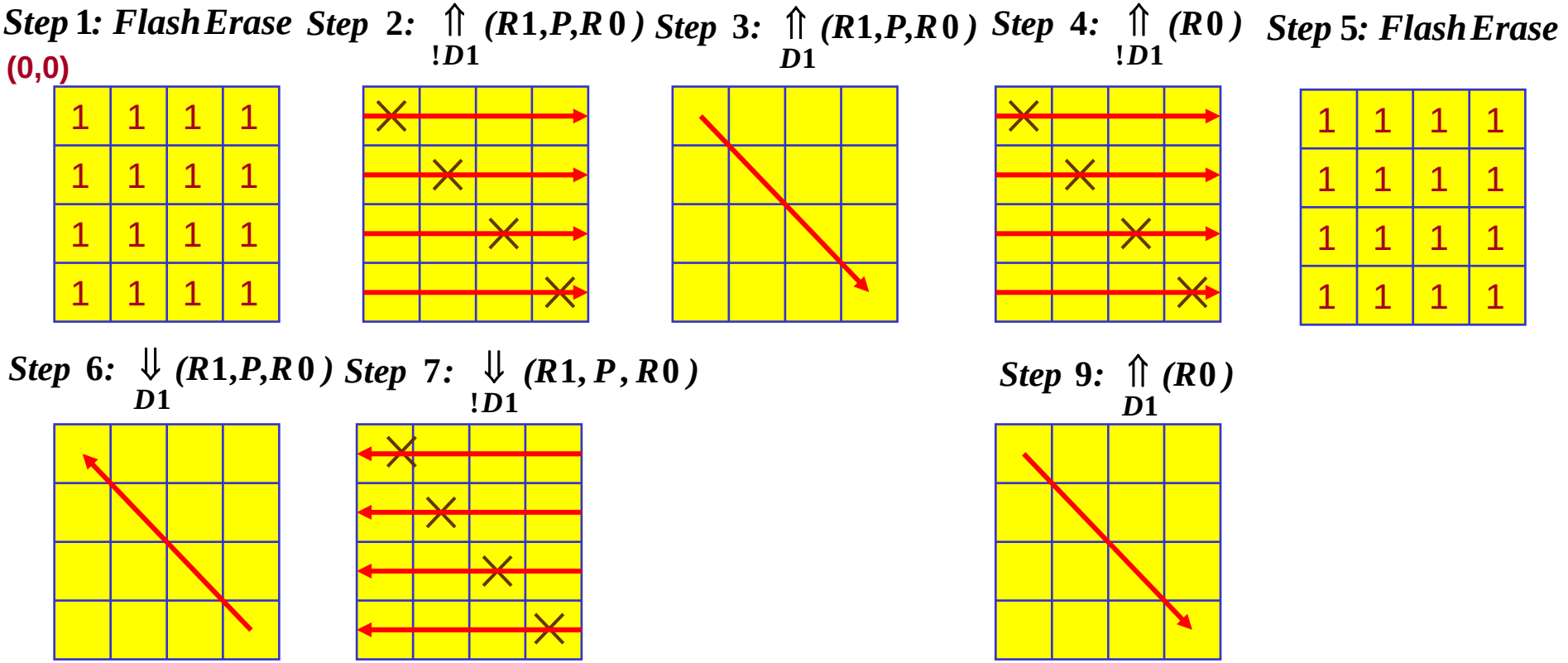
*Mass Erase Time: 200ms; Byte Program Time: 12μs; Byte Read Time: 10ns.

Algorithm	Complexity (N = m x n)			Test Time
	Erase	Program	Read	
EF	*2*	$1N + 2\sqrt{N}$	$2N + \sqrt{N}$	3.569 sec.
Flash March	*2*	*2N*	*4N*	6.702 sec.
March-FT	*2*	*2N*	*6N*	6.707 sec.
Diagonal-FT	*2*	$1N + 2\sqrt{N}$	$4N + 3\sqrt{N}$	3.569 sec.
March-FD	*2*	*3N*	*9N*	9.861 sec.
Diagonal-FD	*2*	$1N + 3\sqrt{N}$	*4N*	3.575 sec.

Fault Simulation: Fault Coverage

EF	WPD	WED	BPD	BED	OE	RD	Total
	100%	100%	0%	100%	100%	100%	72.23%
	SAF	TF	SOF	AF	CFst		
	100%	87.5%	12.5%	44.5%	50%		
Flash March	WPD	WED	BPD	BED	OE	RD	Total
	100%	100%	100%	100%	100%	100%	93.18%
	SAF	TF	SOF	AF	CFst		
	100%	100%	50%	100%	75%		
March-FT	WPD	WED	BPD	BED	OE	RD	Total
	100%	100%	100%	100%	100%	100%	100%
	SAF	TF	SOF	AF	CFst		
	100%	100%	100%	100%	100%		
Diagonal-FT	WPD	WED	BPD	BED	OE	RD	Total
	100%	100%	100%	100%	100%	100%	97.34%
	SAF	TF	SOF	AF	CFst		
	100%	100%	100%	81.6%	89.15%		

Extended Diagonal Flash Test



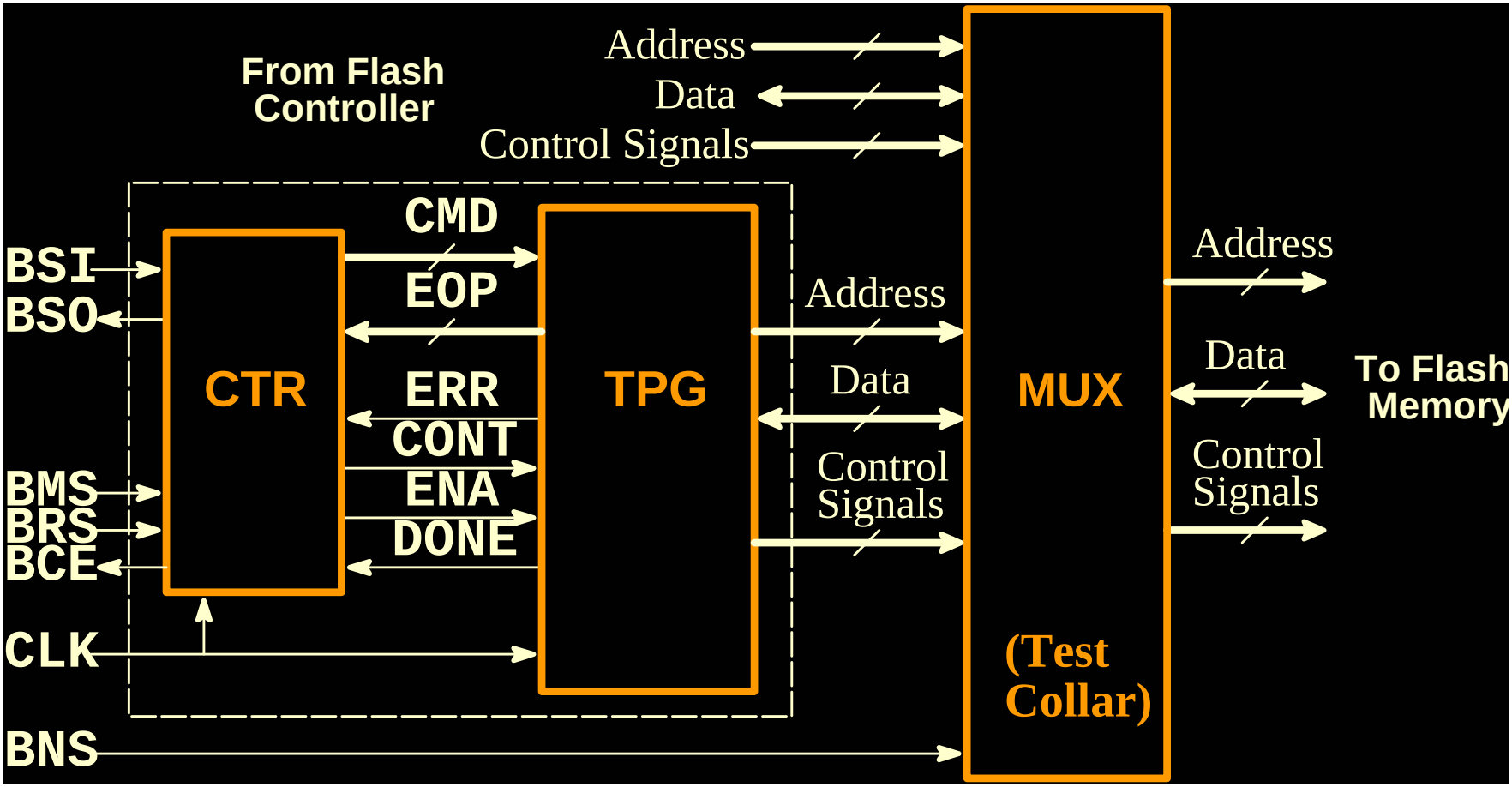
- Fault coverage can achieve 100%.
- Test length: *2e + (2N)p + (5N)r*.
- Test time for the 2Mb flash memory core: 6.705 sec.

Test Time and Area Comparison

(CMOS 1P4M 0.35um)

Algorithm	Fault Coverage	Complexity (N=mxn)			Testing Time (@100MHz)	BISD Area (gate count)
		Erase	Program	Read		
March-FT	100%	*2*	*2N*	*6N*	8.000 sec.	2,502
Diagonal-FT	97.34%	*2*	$1N + 2\sqrt{N}$	$4N + 3\sqrt{N}$	4,585 sec.	2,551
Comparison	-2.66%	*0*	$-(1N - 2\sqrt{N})$	$-(2N - 3\sqrt{N})$	-42.69%	+49
March-FD	100%	*2*	*3N*	*9N*	11.450 sec.	
Diagonal-FD		*2*	$1N + 3\sqrt{N}$	*4N*	4.591 sec.	
Total	100%	*4*	$4N + 3\sqrt{N}$	*13N*	16.041 sec.	

Built-In Self-Test Design

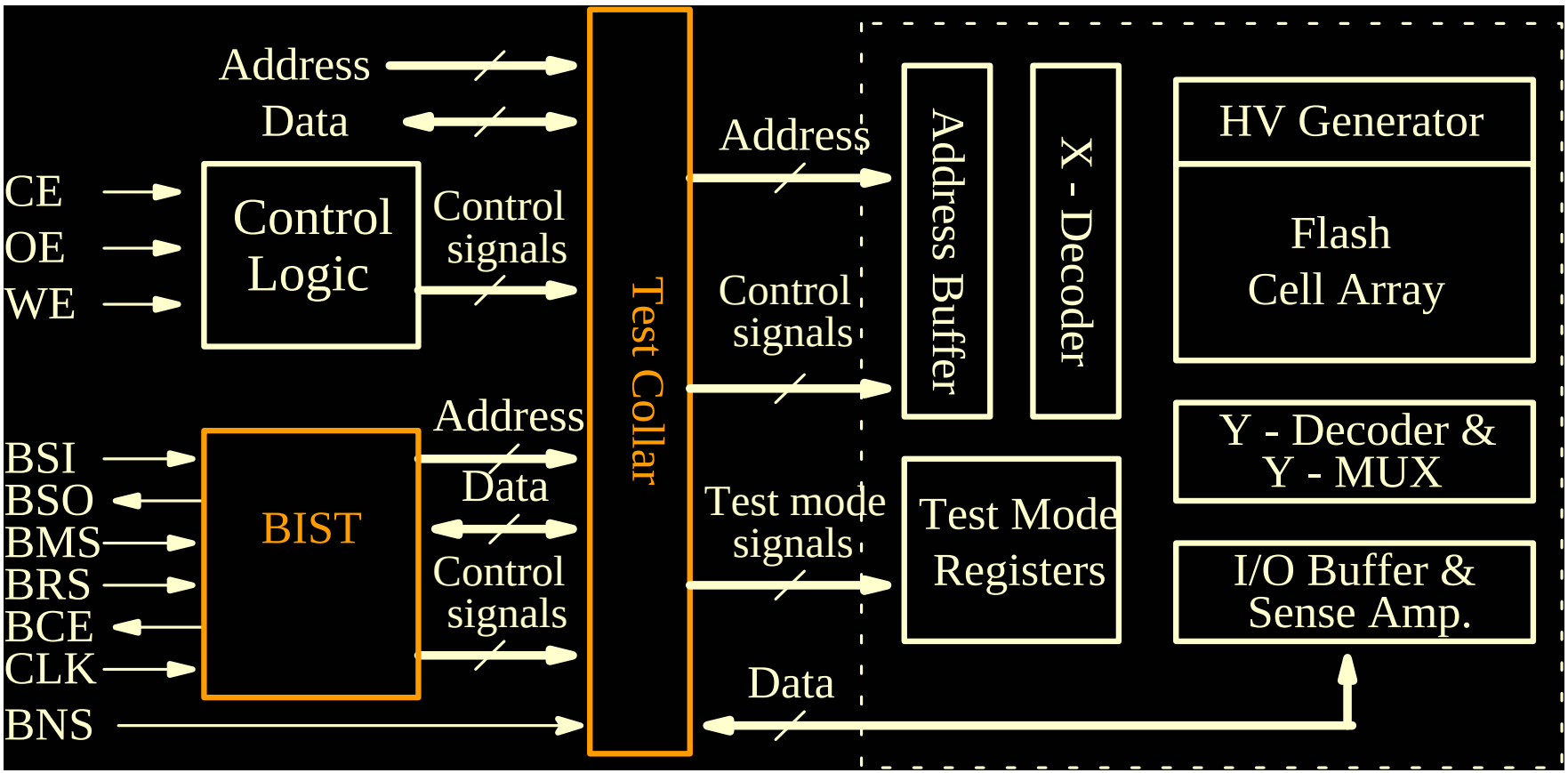


BSI: BIST serial input BSO: BIST serial output BMS: BIST mode select
BRS: BIST reset BNS: BIST/Normal select BCE: BIST commend end
CLK: System clock

Ref: DELTA02

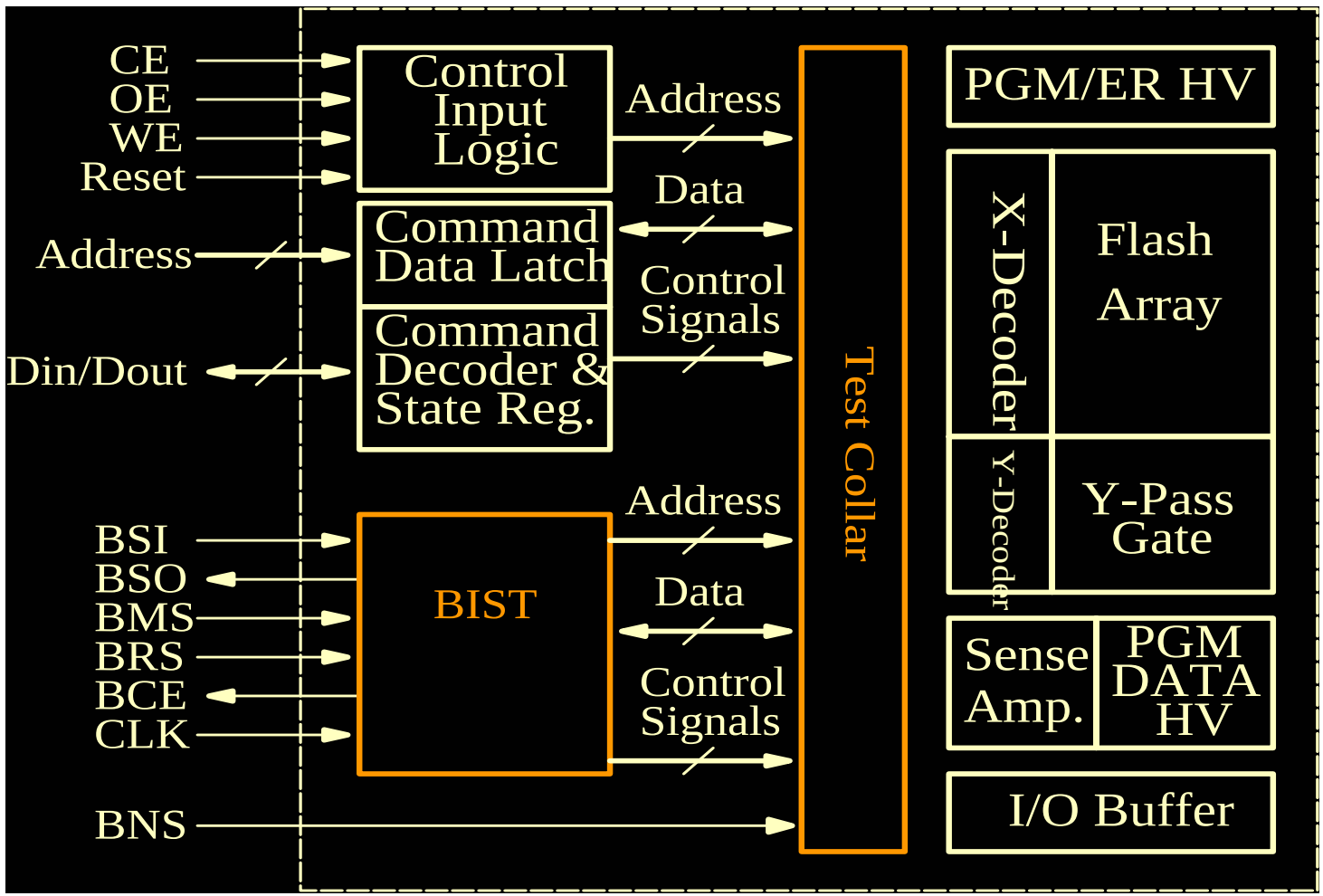
Case I

- A typical 4Mb (512K x 8) embedded flash memory core with BIST circuitry



Case II

- A commodity 1Mb (128K x 8) flash memory chip with BIST circuitry



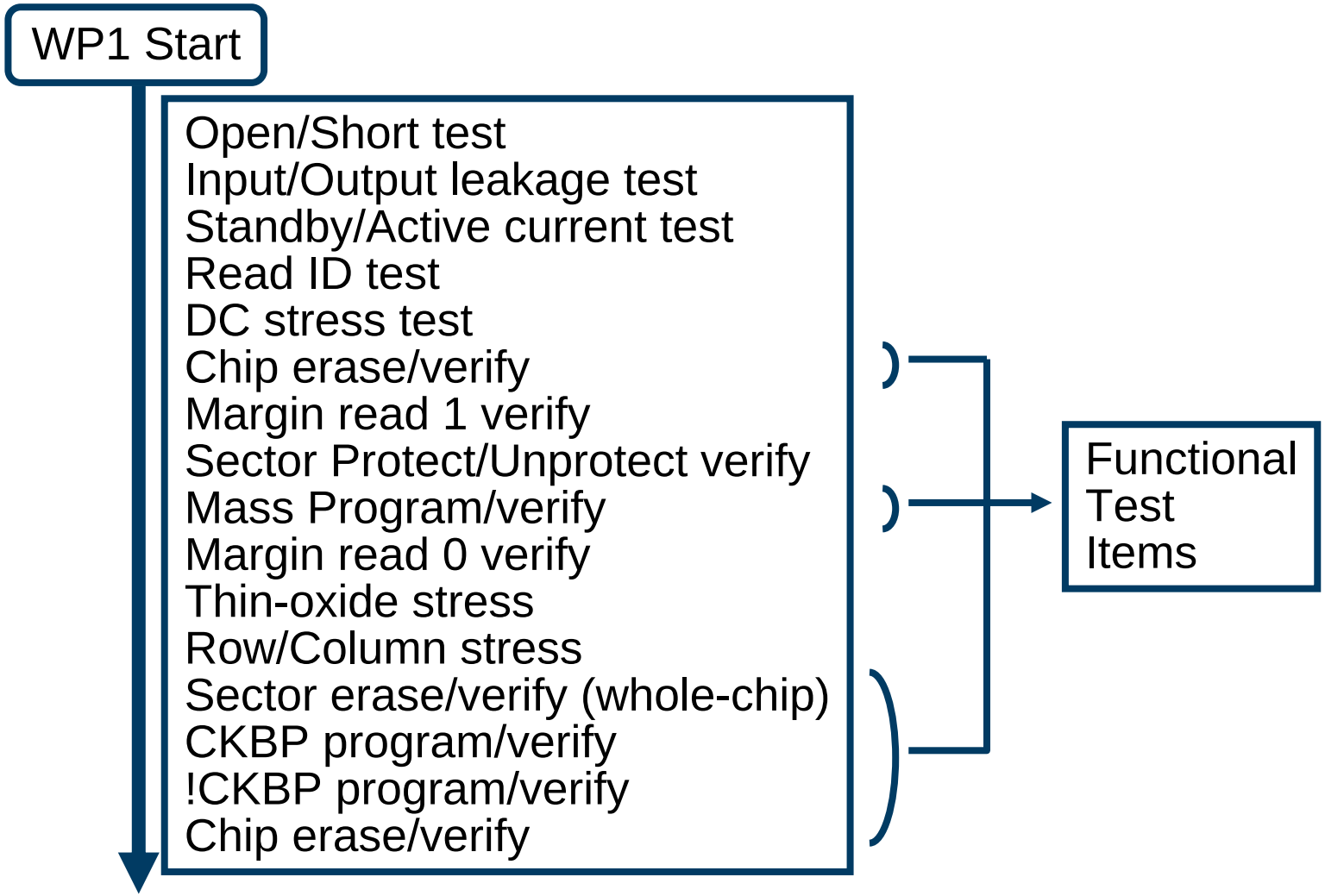
Experimental Results

	Embedded Flash Core	Commodity Flash Chip
Memory Size	512K bytes	128K bytes
Mass Erase Time	200ms	190ms
Byte Program Time	20us	8us
Erase Penalty	2.5ms	1us
Program Penalty	21us	1us
Scrambling Type	Data	Address
Built-In Test Algorithm	March FT (Only solid background)	March FT (With standard background)
Hardware Overhead	3.2%	2.28%
Testing Time	44.612 sec	13sec

Typical Test Modes (Characterization)

- Stress (row/column)
  - Reverse tunneling stress
  - Punch through stress
  - Tox stress
  - DC stress
- Mass program
- Weak erase
- Leak (thin-oxide, bit-line, etc.)
- Cell current; cell Vt
- Margin
- Etc.

Test Items in WP1



Functional Test Items

- MSCAN-like
  - **{(*f*); ⇳ (*r1*); ⇳ (*p0*);⇳ (*r0*); ⇳ (*pCB*); ⇳ (*rCB*); ⇳ (*p!CB*); ⇳(*r!CB*); }**
  - Covers SAF, TF, WPD, BPD, & OE

Notation	Operations	Notation	Address Sequence
f	Erase	⇑	Ascending
p	Program	⇓	Descending
r	Read	⇳	Either

Notation	Background	Notation	Applied Patterns
0	All-zero	***CB***	Checkerboard
1	All-one	***!CB***	Inverse Checkerboard

Test Time Improvement

- Using the March-FT* to improve test coverage and test time
  - **{(*f*); ⇕(*r1, p0, r0*); ⇕(*r0*) (*f*); ⇕(*r1, p0, r0*); ⇕(*r0*);}**
  - Covered SAF, SOF, TF, AF, CFst, WPD, WED, BPD, BED, RD, OE
- Test time reduction in WP1:

$$1 - \frac{2T_e + 2T_p + 6T_r}{3T_e + 3T_p + 6T_r}$$

T_e: erase time (ms)
T_p: program time (us)
T_r: read time (ns)

- Overall test time reduction:

$$1 - \frac{8T_e + 8T_p + 24T_r}{11T_e + 11T_p + 22T_r}$$

* Ref: “Flash Memory Built-In Self-Test Using March-like Algorithms”, DELTA 2002

Built-In Self-Test and Self-Diagnosis

- Use BIST to reduce the number of test pins
- Use BISD to support diagnosis
- Support high-voltage (High-V) mode for commodity flash devices
  - Simplify mode control
- Support cycling test and burn-in test
  - Reduce the complexity of cycling board and burn-in board

Area Overhead of BIST and BISD

- Implemented BIST and BISD on a 2Mb flash memory---7.6mm^2 (0.25um process)

	BIST	BISD	BISD with High-V	BISD with High-V and Cycling
Area (mm^2)	0.0293	0.0432	0.0511	0.0570
Gate Count	1695	2512	2957	3298
Overhead	0.39%	0.57%	0.67%	0.75%

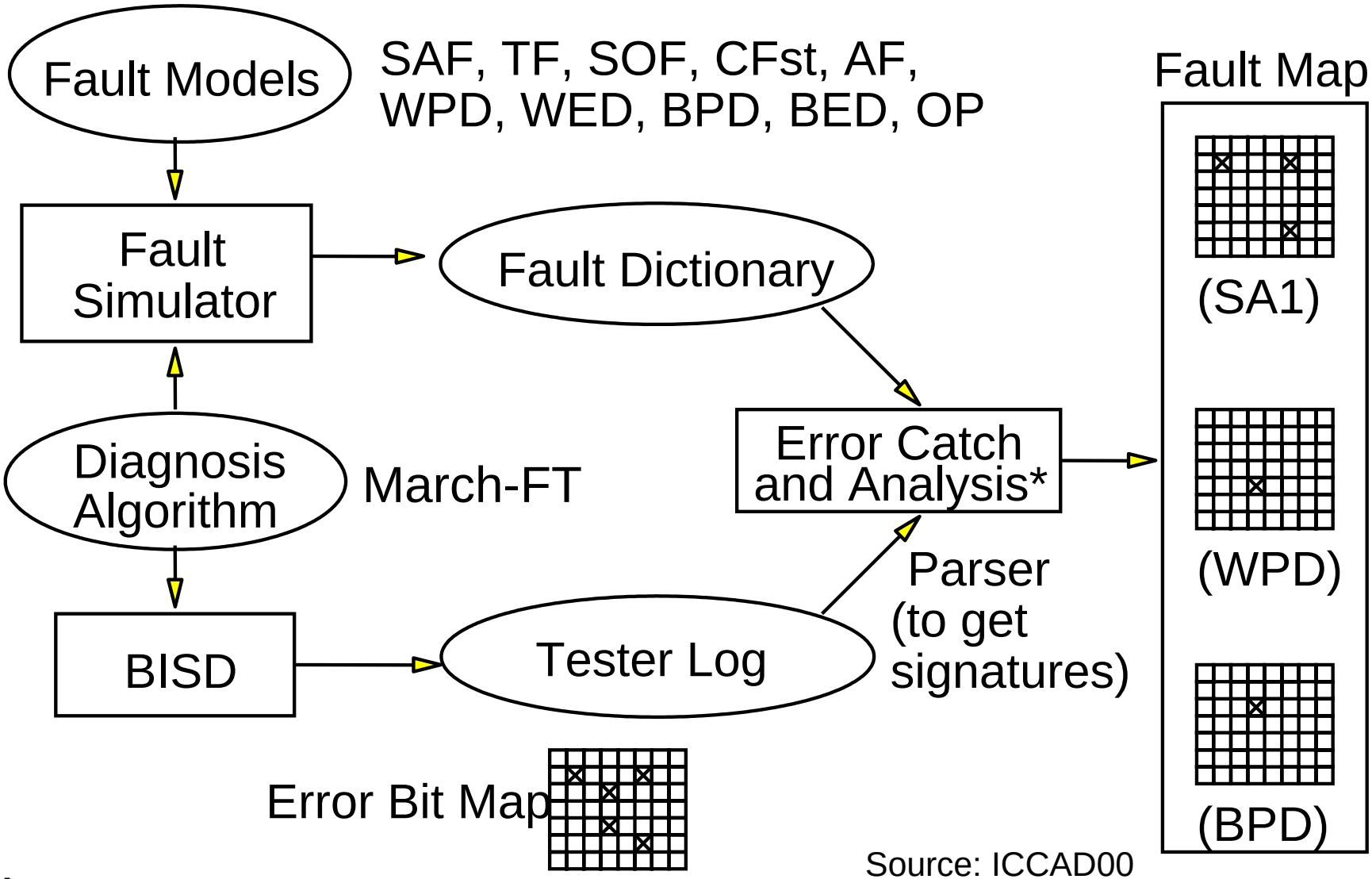
BiNOR-Type Flash Memory

- Bi-directional tunneling program/erase NOR-type flash memory
- Low power consumption and excellent reliability

	Program	Erase
NOR	V_T is raised	V_T is decreased
BiNOR	V_T is decreased	V_T is raised

Source: IEEE Trans. Electron Devices, 2001

Flash Memory Diagnosis Methodology



Source: ICCAD00

Part of the March-FT Fault Dictionary

- March-FT:
  { (f); ⇑(r1,p0,r0); (r0); (f); ⇓(r1,p0,r0); (r0); }
  < 0 0 0 1 1 0 0 0 1 1 >

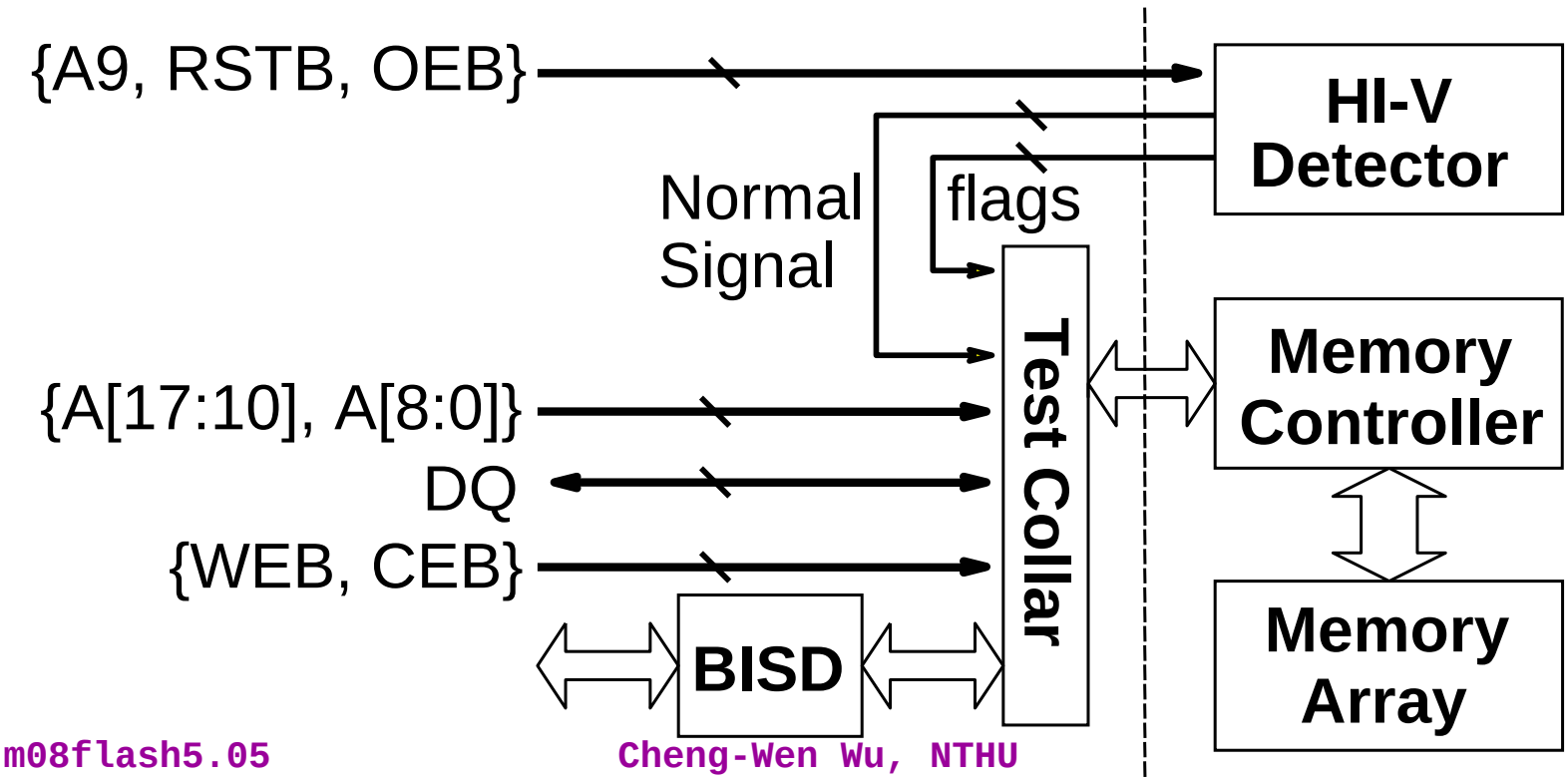
Signatures	Fault Sets	Groups
<0100001000>	SAF(0), OP_M, SOF_M, SOF_T	A
<0001100011>	SAF(1), TF(D)	B
<0000001000>	TF(U), $CFst(0;1/0)_L$, OP_H, $CFst(1;1/0)_S$, AF_L, WPD_L, BPD_L	C

BISD with Enhanced Test Mode Control

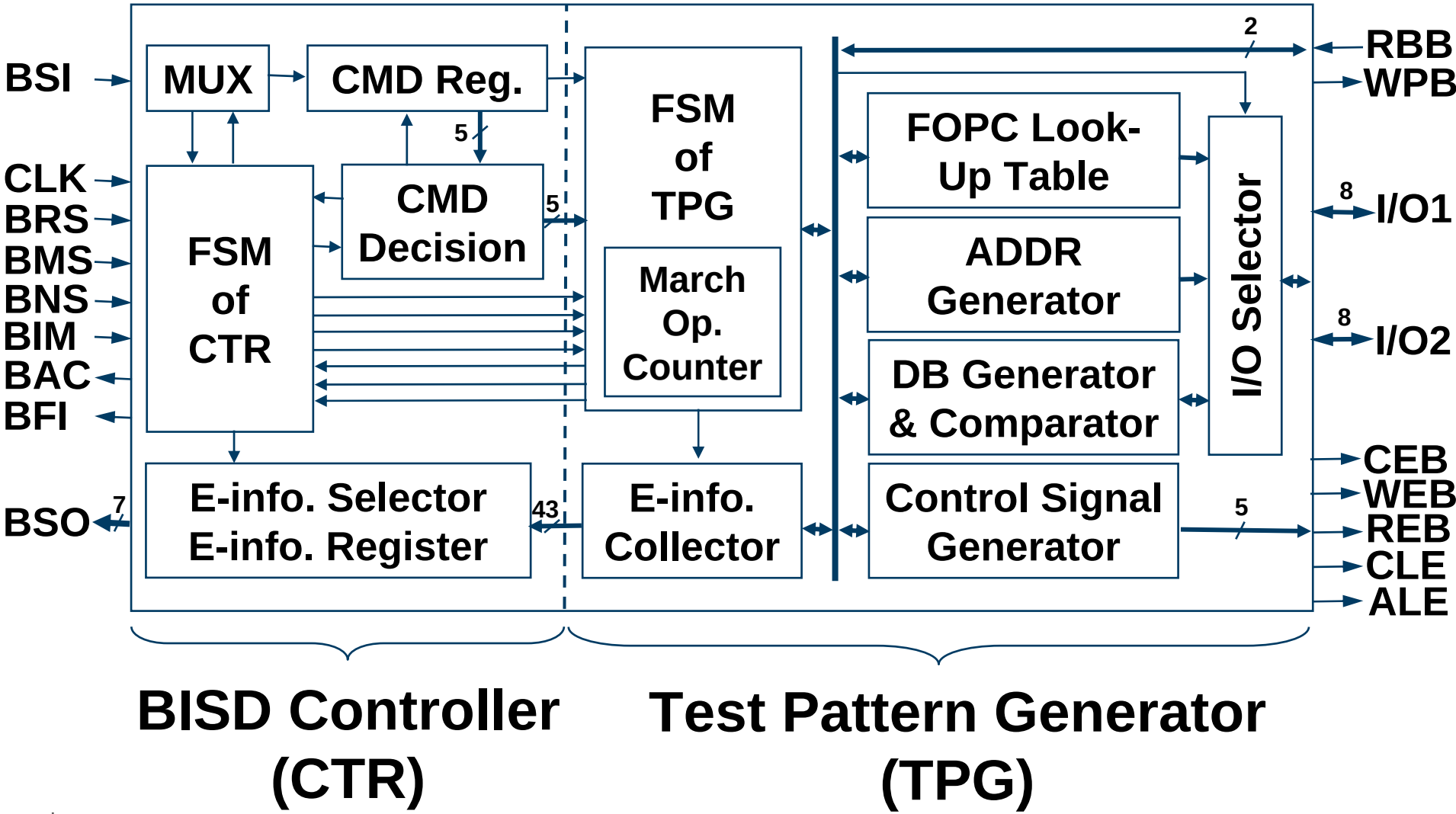
- Built-in March-FT algorithm
- Programmable diagnosis algorithms
- Flexible output format for test and/or diagnosis
- Supports dynamic burn-in (BI) test
- Engineering test mode can be accessed by BISD
  - Overall test time is reduced
- Provides various types of access commands, e.g., Reset Wait

High Voltage (HI-V) Tests

- HI-V tests usually employed to reduce the test time in the engineering test mode
- $T_{Execution}$(HI-V Erase) < $T_{Execution}$(Erase)

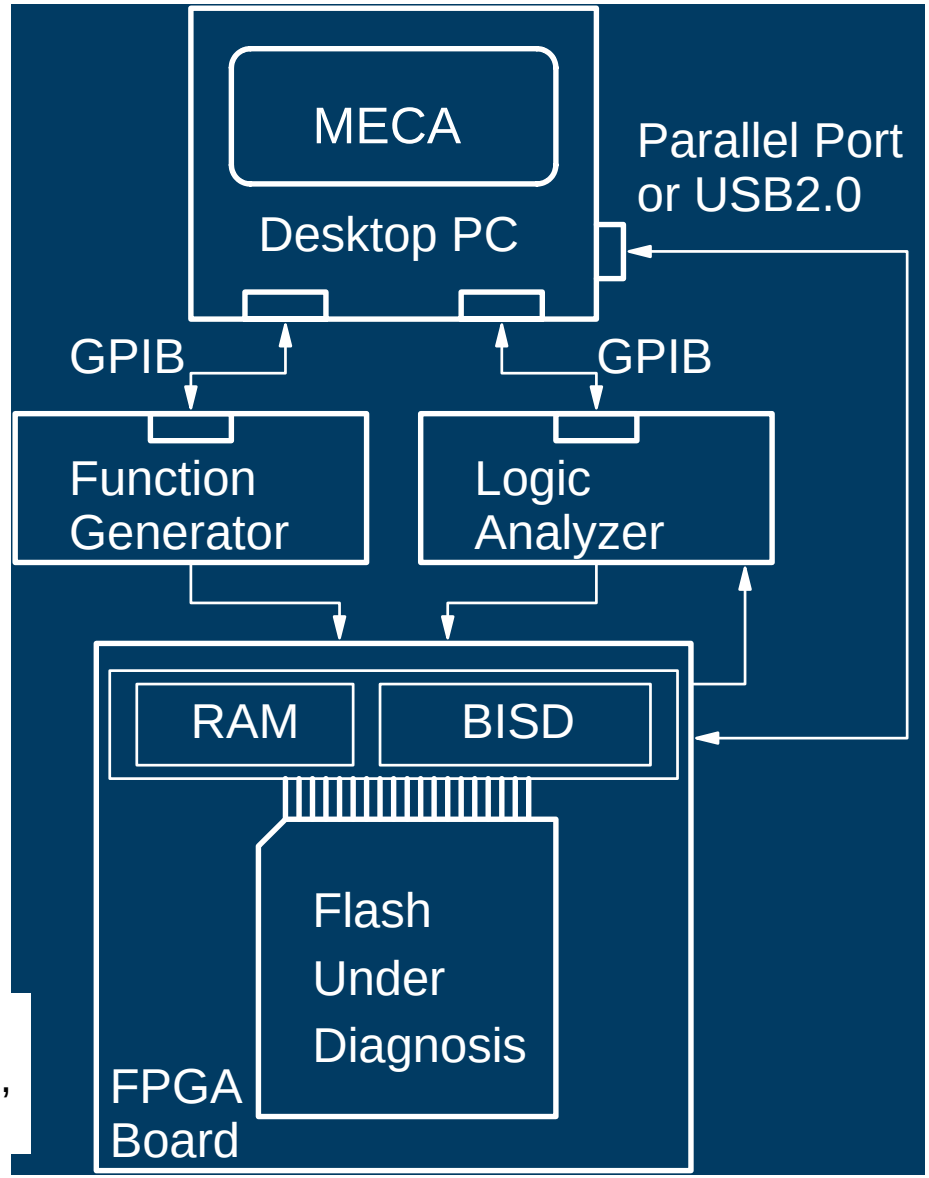


BISD Architecture



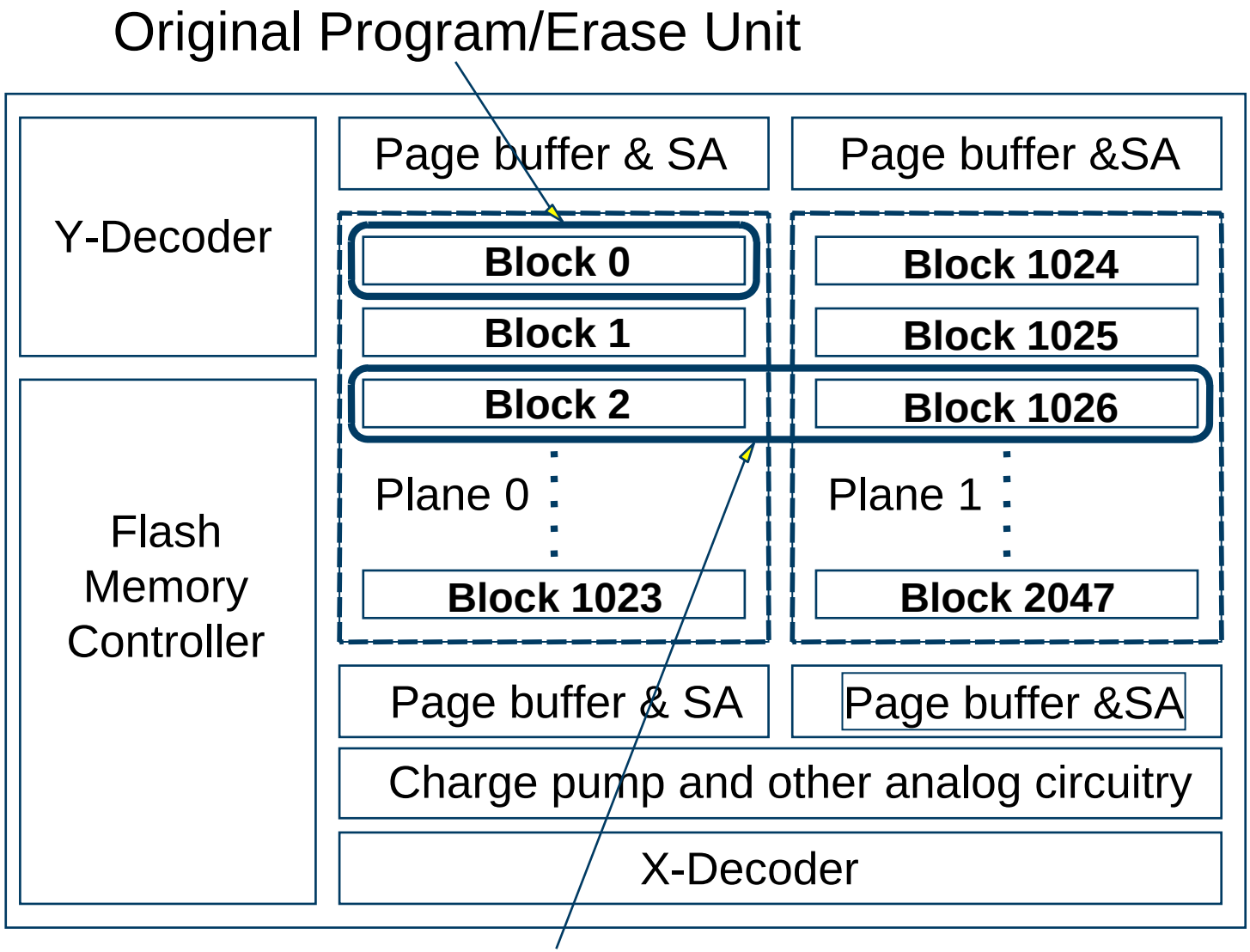
A Configurable Flash Tester

- PC-based low-cost test and diagnosis solution, called CONFLUENCE
- Memory Error Catch and Analysis (MECA*)
- GPIB: General-Purpose Interface Bus



* Ref: “Error catch and analysis for semiconductor memories using March tests”, ICCAD 2000

Parallel Test Methods



Experimental Results

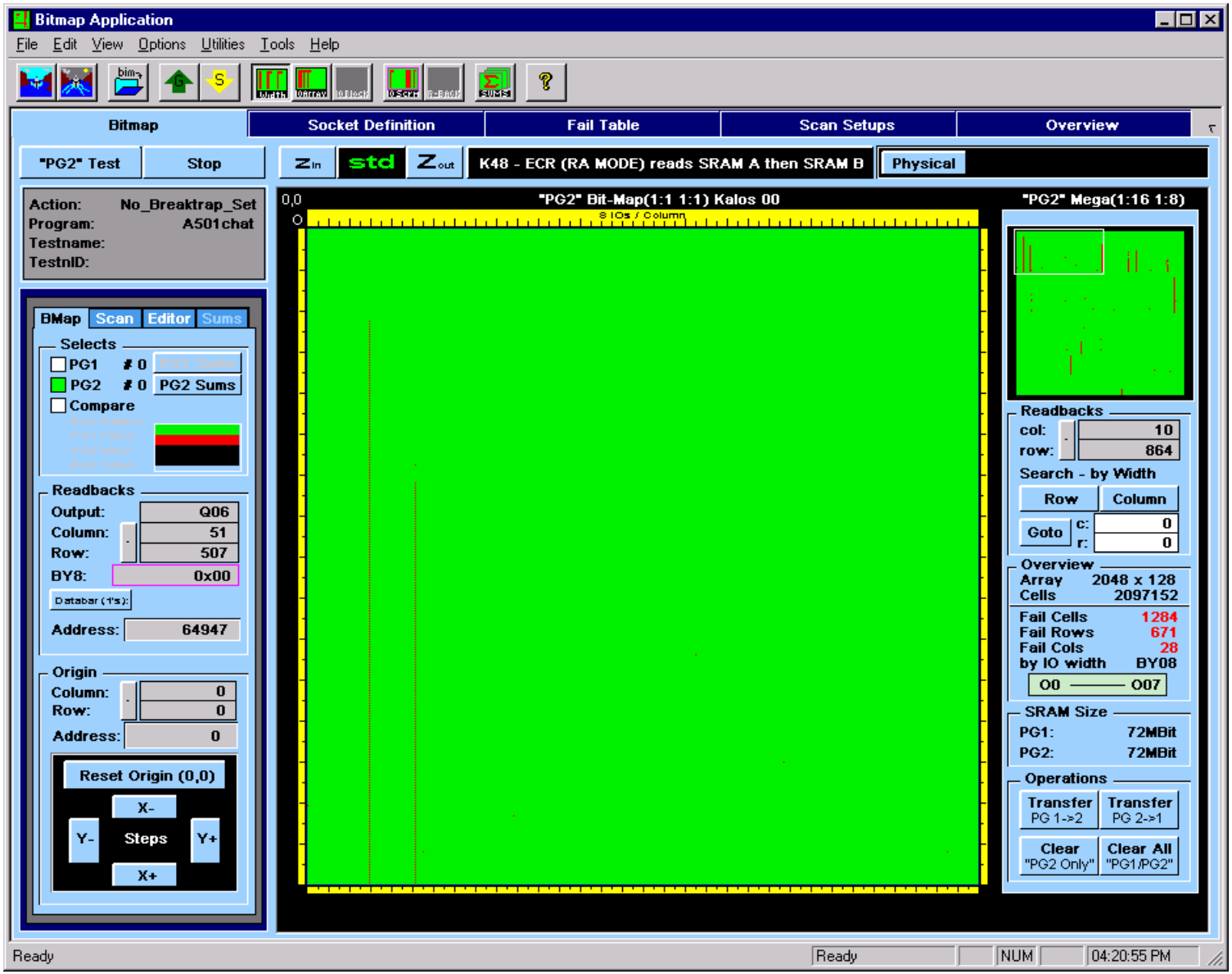
	Case I	Case II
Flash memory area	7.6mm^2	60mm^2
Flash memory capacity	2Mb	256Mb
BISD area	0.05mm^2	0.3mm^2
Area overhead	0.67%	0.5%
BISD frequency	10MHz	40MHz

- BISD circuit implemented on FPGA
- BISD test results compared with those of ATE

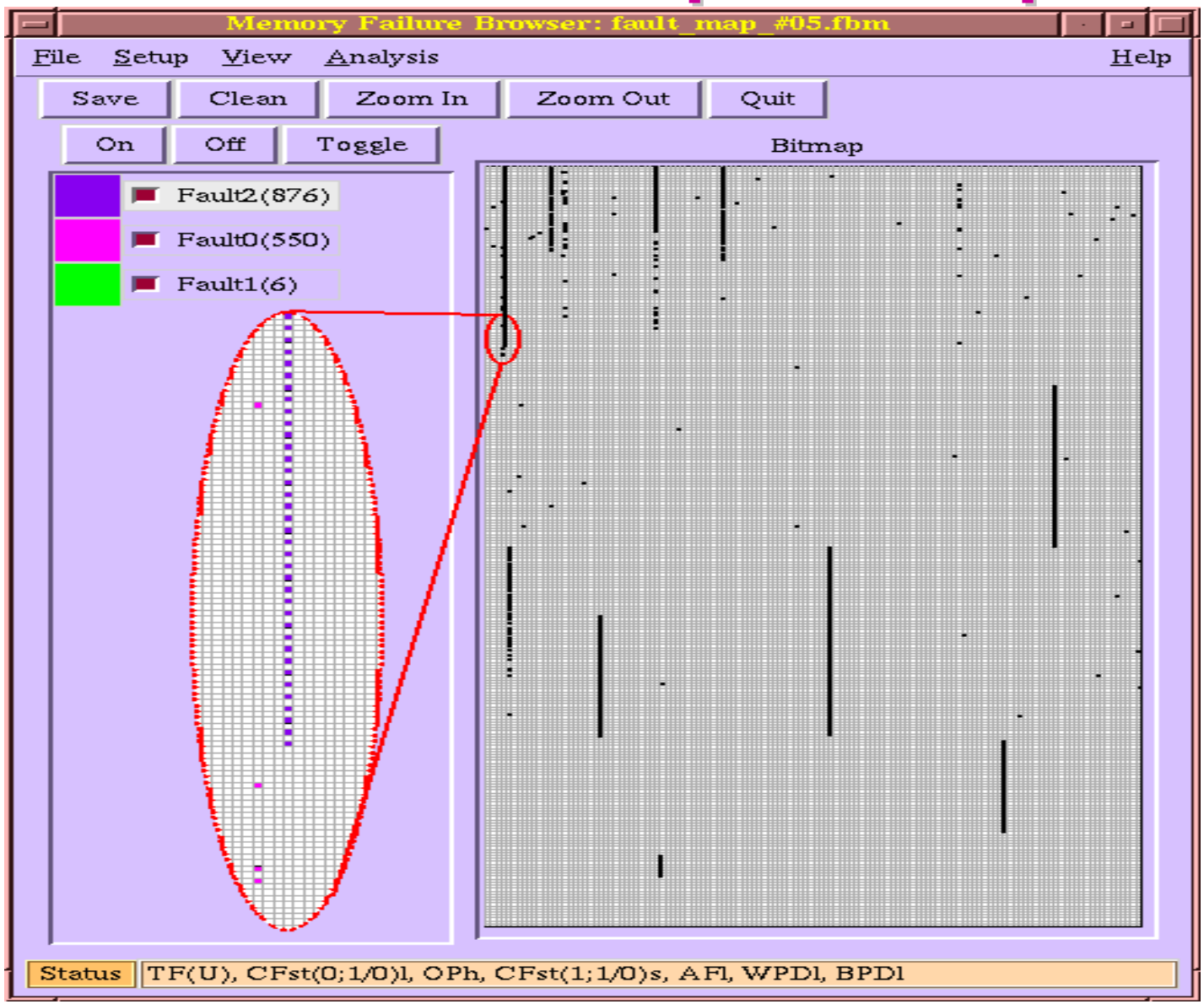
Diagnosis Result for 2Mb Flash

	Chip1	Chip2	Chip3	Chip4	Chip5	Chip6	Chip7	Chip8
MSCAN	Pass	Fail	Pass	Fail	Partial	Fail	Pass	Pass
March-FT	Fail	Fail	Fail	Fail	Fail	Fail	Fail	Pass
Unmodeled Faults	0	10	0	---	0	---	0	0
Fault Groups	A: 1 C:182 D: 81	B: 19 C: 1 E: 2 F: 1 G: 1 J: 30 K: 54	A: 4 C:113 D: 16		A: 6 C:876 D:550	A: 5 C:940 D:496 J:105	C: 4 D: 1	

The Error Bitmap for Chip 5



The Fault Bitmap for Chip 5



Results for 256Mb Flash Memory

- Three chips are tested in this case
- ATE test result: one passed and two failed
- FPGA (BISD prototype) test results: two passed and one failed
  - The difference between ATE and FPGA is clock rate
  - Real BISD can perform at-speed test
- Diagnosis result for the failed chip: one block cannot be erased (SA0)
  - Same for ATE & FPGA

Conclusions

- Flash memory fault models and test algorithms are proposed
  - Both march-based and diagonal tests are effective
- A flash memory simulator has been developed to facilitate the analysis and generation of the test algorithms
- Flash memory BIST/BISD is feasible
- Future work:
  - To support more flash memory types and other realistic fault models
  - Diagnosis methodology for flash memories
  - BISR