DATA SHEET

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SPFD54124B

396-channel 6-bit Source Driver with System-on-chip for Color Amorphous TFT-LCDs

Preliminary

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396-CHANNEL DRIVER WITH SYSTEM-ON-CHIP (SOC) FOR COLOR AMORPHOUS TFT LCD

1. GENERAL DESCRIPTION

The SPFD54124B, a 262144-color System-on-Chip (SoC) driver LSI designed for small and medium sizes of TFT LCD display, is capable of supporting up to 132xRGBx162 in resolution which can be achieved by the designated RAM for graphic data. The 396-channel source driver has true 6-bit resolution, which generates 64 Gamma-corrected values by an internal D/A converter.

The SPFD54124B is able to operate with low IO interface power supply up to 1.6V and incorporate with several charge pumps to generate various voltage levels that form an on-chip power management system for gate driver and source driver.

The built-in timing controller in SPFD54124B can support several interfaces for the diverse request of medium or small size portable display. SPFD54124B provides system interfaces, which include 8-/9-/16-/18-bit parallel interfaces and serial interface (SPI), to configure system. Not only can the system interfaces be used to configure system, they can also access RAM at high speed for still picture display. In addition, the SPFD54124B incorporates 6, 16, and 18-bit RGB interfaces for picture movement display. The SPFD54124B also supports a function to display eight colors and a standby mode for power control consideration.

2. FEATURES

- One-chip solution for amorphous TFT-LCD.
- Supports resolution up to 132xRGBx162, incorporating a 396-channel source driver and a 162-channel gate driver
- Outputs 64 γ -corrected values using an internal true 6-bit resolution D/A converter to achieve 262K colors
- Built-in 48114 bytes internal RAM
- Line Inversion AC drive / frame inversion AC drive
- System interfaces
  - High-speed interfaces to 8-, 9-, 16-, and 18-bit parallel ports
  - 3-pin 9 bits or 4-pin 8 bits Serial Peripheral Interface (SPI)
- Interfaces for moving picture display
  - 6-, 16-, and 18-bit RGB interfaces
- Diverse RAM accessing for functional display
  - Window address function to display at any area on the screen via a moving picture display interface
  - Window address function to limit the data rewriting area and reduce data transfer
  - Moving and still picture can display at the same time
  - Vertical scrolling function
  - Partial screen display
- Power supply
  - Logic power supply voltage (VDD): 2.6 ~ 3.6 V
  - I/O interface supply voltage (VDDIO): 1.6 ~ 3.6 V
  - Analog power supply voltage (VDD): 2.6 ~ 3.6V
- On-chip power management system
  - Power saving mode (standby / 8-color mode, etc)
  - Low power consumption structure for source driver.
- Built-in Charge Pump circuits
  - Source driver voltage level : 2 times (x2) of Vci1
  - Gate driver voltage level (VGH, VGL) up to 6 times (x6) and minus 5 times (x-5) Vci1
- Built-in internal oscillator and hardware reset
- Built–in One-Time-Programming (OTP) function for VCOM amplitude and VcomH voltage adjustment.

3. ORDERING INFORMATION

Product Number	Package Type
SPFD54124B-C	Chip Form With Gold Bump

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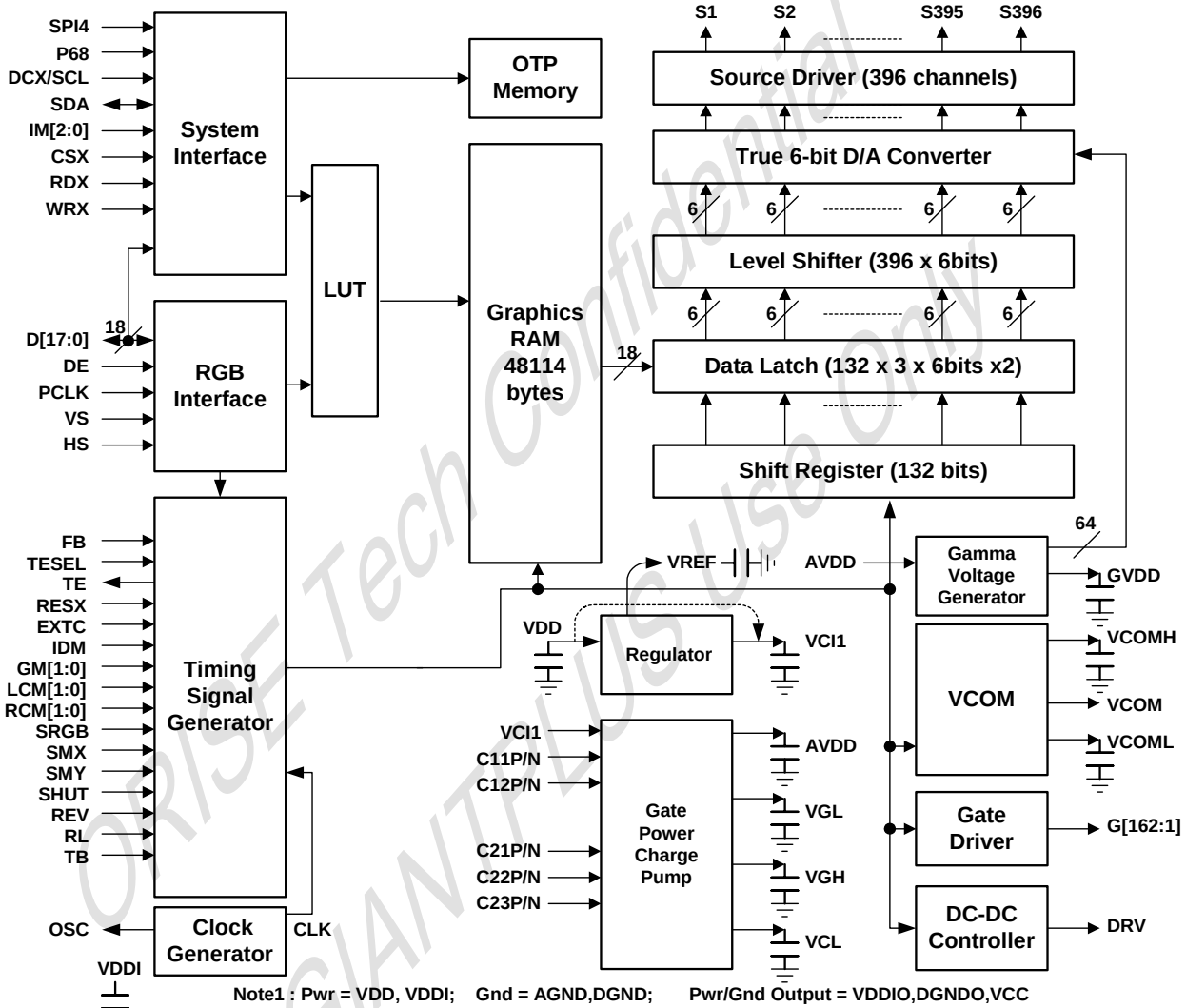
4. BLOCK DIAGRAM

4.1. Block Function



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4.1.1. System Interface

The SPFD54124B supports three high-speed system interfaces:

1. 80-system high-speed interfaces with 8-, 9-, 16-, 18-bit parallel ports.
2. 68-system high-speed interfaces with 8-, 9-, 16-, 18-bit parallel ports.
3. 3-pin 9-bits or 4-pin 8 bits Serial Peripheral Interface (SPI).

The SPFD54124B has a 16-bit index register (IR) and two 18-bit data registers, a write-data register (WDR) and a read-data register (RDR). The IR register is used to store index information from control registers. The WDR register is used to temporarily store data to be written for register control and internal GRAM. The RDR register is used to temporarily store data read from the GRAM. When graphic data is written to the internal GRAM from MCU/graphic engine, the data is first written to the WDR and then automatically written to the internal GRAM in internal operation. When graphic data read operation is executed, graphic data is read via the RDR from the internal GRAM. Therefore, invalid data is first read out to the data bus when the SPFD54124B executes the 1st read operation. Thus, valid data can be read out after the SPFD54124B executes the 2nd read operation.

4.1.2. External Display Interface

The SPFD54124B supports external RGB interface for picture movement display.

The SPFD54124B allows switching between one of the external display interfaces and the system interface via pin configuration so that the optimum interface is selected for still / moving picture displayed on the screen.

When the RGB interface is chosen, display operations are synchronized with external supplied signals, VSYNC, HSYNC, and DOTCLK. Moreover, valid display data (DB17-0) is written to GRAM, which synchronized with signal (DE) enabling.

4.1.3. Address Counter (AC)

SPFD54124B features an Address Counter (AC) giving an address to the internal GRAM. The address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

4.1.4. Graphics RAM (GRAM)

SPFD54124B features a 48114-byte (132 x 162x 18 / 8) Graphic RAM (GRAM).

4.1.5. Grayscale Voltage Generating Circuit

SPFD54124B has true 6-bit resolution D/A converter, which generates 64 Gamma-corrected values and cooperates with OP-AMP structure to enhance display quality. The grayscale voltage can be adjusted by grayscale data set in the γ-correction register.

4.1.6. Timing Controller

SPFD54124B has a timing controller which can generate a timing signal for internal circuit operation such as gate output timing, RAM accessing timing, etc.

4.1.7. Oscillator (OSC)

The SPFD54124B also features an internal oscillator to generate RC oscillation with an internal resistor. In standby mode, RC oscillation is halted to reduce power consumption.

4.1.8. Source Driver Circuit

SPFD54124B consists of a 396-output source driver circuit (S1 ~ S396). Data in the GRAM are latched when the 396th bit data is input. The latched data controls the source driver and generates a drive waveform.

4.1.9. Gate Driver Circuit

SPFD54124B consists of a 162-output gate driver circuit (G1~G162). The gate driver circuit outputs gate driver signals at either VGH or VGL level.

4.1.10. LCD Driving Power Supply Circuit

The LCD driving power supply circuit generates the voltage levels AVDD, VGH, VGL and VCOM for driving an LCD. All this voltages can be adjusted by register setting.

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5. SIGNAL DESCRIPTIONS

<table>
<tr><th>Signal</th><th>Pin No.</th><th>I/O</th><th>Connected with</th><th>Function</th></tr>
<tr><td colspan="5">System Configuration Input Signal</td></tr>
<tr><td>P68,
IM2~0,
SPI4</td><td>5</td><td>I</td><td>GND/ VDDIO</td><td>Select system interface mode.
<table>
<tr><th>SPI4</th><th>P68</th><th>IM2</th><th>IM1</th><th>IM0</th><th></th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>-</td><td>-</td><td>3-Pin Serial interface</td></tr>
<tr><td>-</td><td>0</td><td>1</td><td>0</td><td>0</td><td>8080 MCU 8-bits Parallel interface</td></tr>
<tr><td>-</td><td>0</td><td>1</td><td>0</td><td>1</td><td>8080 MCU 16-bits Parallel interface</td></tr>
<tr><td>-</td><td>0</td><td>1</td><td>1</td><td>0</td><td>8080 MCU 9-bits Parallel interface</td></tr>
<tr><td>-</td><td>0</td><td>1</td><td>1</td><td>1</td><td>8080 MCU 18-bits Parallel interface</td></tr>
<tr><td>-</td><td>1</td><td>0</td><td>-</td><td>-</td><td>3-Pin Serial interface</td></tr>
<tr><td>-</td><td>1</td><td>1</td><td>0</td><td>0</td><td>6800 MCU 8-bits Parallel interface</td></tr>
<tr><td>-</td><td>1</td><td>1</td><td>0</td><td>1</td><td>6800 MCU 16-bits Parallel interface</td></tr>
<tr><td>-</td><td>1</td><td>1</td><td>1</td><td>0</td><td>6800 MCU 9-bits Parallel interface</td></tr>
<tr><td>-</td><td>1</td><td>1</td><td>1</td><td>1</td><td>6800 MCU 18-bits Parallel interface</td></tr>
<tr><td>1</td><td>-</td><td>0</td><td>-</td><td>-</td><td>4-Pin Serial interface</td></tr>
</table></td></tr>
<tr><td>RESX</td><td>1</td><td>I</td><td>MPU or
external
RC circuit</td><td>Reset pin. This is an active low signal.</td></tr>
<tr><td>EXTC</td><td>1</td><td>1</td><td>GND/ VDDIO</td><td>Extend command set access
Low: Extend command set is not accessible.
High: Extend command set is accessible.
If this is not used. Open it (This pin is internally pull low).</td></tr>
<tr><td>GAMSEL</td><td>1</td><td>1</td><td>GND/ VDDIO</td><td>Gamma Setting selection:
(a) Low: GC0=1.0, GC1=2.5, GC2=2.2, GC3=1.8.
(b) High: GC0=2.2, GC1=1.8, GC2=2.5, GC3=1.0.</td></tr>
<tr><td>GM1~0</td><td>2</td><td>1</td><td>GND/ VDDIO</td><td>Resolution selection:
<table>
<tr><th>GM1</th><th>GM0</th><th>Resolution</th></tr>
<tr><td>0</td><td>0</td><td>128*RGB*160</td></tr>
<tr><td>0</td><td>1</td><td>120*RGB*160</td></tr>
<tr><td>1</td><td>0</td><td>128*RGB*128</td></tr>
<tr><td>1</td><td>1</td><td>132*RGB*162</td></tr>
</table></td></tr>
<tr><td>RCM1~0</td><td>2</td><td>1</td><td>GND/ VDDIO</td><td>Interface selection:
<table>
<tr><th>RCM1</th><th>RCM0</th><th>Interface</th></tr>
<tr><td>0</td><td>0</td><td>MCU Interface</td></tr>
<tr><td>0</td><td>1</td><td>MCU Interface</td></tr>
<tr><td>1</td><td>0</td><td>RGB Interface</td></tr>
<tr><td>1</td><td>1</td><td>RGB Interface</td></tr>
</table></td></tr>
<tr><td>IDM</td><td>1</td><td>1</td><td>MCU</td><td>In RGB interface mode:
(a) Low: Normal Display.
(b) High: Idle Mode (8-color mode).
This pin can be only used when RGB mode is selected.</td></tr>
<tr><td>LCM[1:0]</td><td>1</td><td>1</td><td>GND/ VDDIO</td><td>Liquid Crystal Type selection:</td></tr>
</table>

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<table>
<tr><th>Signal</th><th>Pin No.</th><th>I/O</th><th>Connected with</th><th>Function</th></tr>
<tr><td></td><td></td><td></td><td></td><td>
<table>
<tr><th>LCM1</th><th>LCM0</th><th>LC Type</th></tr>
<tr><td>0</td><td>0</td><td>TR</td></tr>
<tr><td>0</td><td>1</td><td>TM</td></tr>
<tr><td>1</td><td>0</td><td>LV</td></tr>
<tr><td>1</td><td>1</td><td>MVA</td></tr>
</table>
</td></tr>
<tr><td>SRGB</td><td>1</td><td>1</td><td>GND/ VDDIO</td><td>RGB arrangement selection:
(a) Low: S1, S2, S3 fit ‘R’, ‘G’, ‘B’.
(b) High: S1, S2, S3 fit ‘B’, ‘G’, ‘R’</td></tr>
<tr><td>SHUT</td><td>1</td><td>1</td><td>GND/ VDDIO</td><td>Display on/off selection when RGB mode is selected.
(a) Low: Display On.
(b) High: Display Off.
This pin can be only used when RGB mode is selected.</td></tr>
<tr><td>REV</td><td>1</td><td>1</td><td>GND/ VDDIO</td><td>Data reverse for source driver selection when RGB mode is selected.
(a) Low: Reverse Off.
(b) High: Reserve On.
This pin can be only used when RGB mode is selected.</td></tr>
<tr><td>SMX</td><td>1</td><td>1</td><td>GND/ VDDIO</td><td>Source driver output direction selection:
<table>
<tr><th>SMX</th><th>GM=”00” or “10”</th><th>GM=”01”</th><th>GM=”11”</th></tr>
<tr><td>0</td><td>S7 => S390</td><td>S7=>S366</td><td>S1=>S396</td></tr>
<tr><td>1</td><td>S390=>S7</td><td>S366=>S7</td><td>S396=>S1</td></tr>
</table>
</td></tr>
<tr><td>SMY</td><td>1</td><td>1</td><td>GND/ VDDIO</td><td>Gate driver output direction selection:
<table>
<tr><th>SMY</th><th>GM=”00” or “01”</th><th>GM=”10”</th><th>GM=”11”</th></tr>
<tr><td>0</td><td>G2 =>G161</td><td>G2=>G129</td><td>G1=>G162</td></tr>
<tr><td>1</td><td>G161=>G2</td><td>G129=>G2</td><td>G162=>G1</td></tr>
</table>
</td></tr>
<tr><td>RL</td><td>1</td><td>1</td><td>GND/ VDDIO</td><td>Source driver output direction selection:
<table>
<tr><th>RL</th><th>SMX</th><th>GM=”00” or “10”</th><th>GM=”01”</th><th>GM=”11”</th></tr>
<tr><td>0</td><td>0</td><td>S7 => S390</td><td>S7=>S366</td><td>S1=>S396</td></tr>
<tr><td>0</td><td>1</td><td>S390=>S7</td><td>S366=>S7</td><td>S396=>S1</td></tr>
<tr><td>1</td><td>0</td><td>S390=>S7</td><td>S366=>S7</td><td>S396=>S1</td></tr>
<tr><td>1</td><td>1</td><td>S7 => S390</td><td>S7=>S366</td><td>S1=>S396</td></tr>
</table>
This pin can be only used when RGB mode is selected.</td></tr>
<tr><td>TB</td><td>1</td><td>1</td><td>GND/ VDDIO</td><td>Gate driver output direction selection:
<table>
<tr><th>TB</th><th>SMY</th><th>GM=”00” or “01”</th><th>GM=”10”</th><th>GM=”11”</th></tr>
<tr><td>0</td><td>0</td><td>G2 =>G161</td><td>G2=>G129</td><td>G1=>G162</td></tr>
<tr><td>0</td><td>1</td><td>G161=>G2</td><td>G129=>G2</td><td>G162=>G1</td></tr>
<tr><td>1</td><td>0</td><td>G161=>G2</td><td>G129=>G2</td><td>G162=>G1</td></tr>
<tr><td>1</td><td>1</td><td>G2 =>G161</td><td>G2=>G129</td><td>G1=>G162</td></tr>
</table>
This pin can be only used when RGB mode is selected.</td></tr>
<tr><td>TESEL</td><td>1</td><td>I</td><td>GND/ VDDIO</td><td>
<table>
<tr><th>TESEL</th><th>TE period select</th></tr>
<tr><td>0</td><td>The period of TE is equal 162 line</td></tr>
<tr><td>0</td><td>The period of TE is equal 160 line</td></tr>
</table>
</td></tr>
</table>

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Signal	Pin No.	I/O	Connected with	Function
Interface input Signals				
CSX	1	I	MPU	Chip select signal. Low: the SPFD54124B is accessible High: the SPFD54124B is not accessible This pin has can be permanently fixed "Low" in MCU interface mode only.
D/CX (SCL)	1	I	MPU	Display data / Command selection pin in parallel interface Low: Command data High: Display data In SPI I/F, this is used as SCL pin. Must connect to the GND or VDDIO level when not used.
WRX (R/WX)	1	I	MPU	(A) In 80-system interface mode, a write strobe signal can be input via this pin and initializes a write operation when the signal is low. (B) In 68-system interface mode, a write or read control signal can be input via this pin and initializes a write or read operation. Must connect to the GND or VDDIO level when not used.
RDX (E)	1	I	MPU	In 80-system interface mode, a read strobe signal can be input via this pin and initializes a read operation when the signal is low. In 68system interface mode, a strobe signal can be input via this pin and initializes a write or read operation when the signal is low. Must connect to the GND or VDDIO level when not in use.
SDA	1	I/O	MPU	(A) When RCM = '1' (RGB I/F), Serial input/ output signal in serial I/F mode. The data is input on the rising edge of the SCL signal. The data is output on the falling edge of the SCL signal. (B) When RCM = '0' (MCU I/F), This pin is not used, and fix at VDDIO or DGND level. If not used, please fix this pin at VDDIO or DGND level.
DB0-DB17	1	I/O	MPU	(A) When RCM = '1' (RGB I/F), D[17:0] are used for RGB interface data bus (B) When RCM = '0' (MCU I/F), D[17:0] are used to MCU parallel interface data bus (C) In SPI I/F, D0 is used as Serial input/ output signal. In SPI I/F, D[17:1] not used, please fix this pin at VDDIO or DGND level.
VS	1	I	MPU	In external interface mode, served as a vertical synchronize signal input Must connect to the VDDIO or DGND level when not in use.
HS	1	I	MPU	In external interface mode, served as a horizontal synchronized signal input Must connect to the VDDIO or DGND level when not in use.
DE	1	I	MPU	In external interface mode, polarity of DE signal is synchronized with valid graphic data input. High: Valid data on DB17-DB0 Low: Invalid data on DB17-DB0 Must connect to the VDDIO or DGND level when not in use.
PCLK	1	I	MPU	In external interface mode, served as a dot clock signal. Must connect to the VDDIO or DGND level when not in use.
OSC	1	O	MPU	Oscillator frequency output pin for oscillator testing and turn ON/OFF by S/W command.
Charge Pump and Power Supply Signal				

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Signal	Pin No.	I/O	Connected with	Function
C11P/N, C12P/N C21P/N, C22P/N C23P/N	10	-	Step-up capacitor	Connect boost capacitors for the internal DC/DC converter circuit to these pins. Leave the pins open when DC/DC converter circuits are not used.
VCI1	1	O	Stabilizing capacitor	An internal reference voltage level, which is regulated from VDD. The amplitude of VCI1 is from VDD-GND. Place a stabilizing capacitor between GND.
AVDD	1	O	Stabilizing capacitor	Output 2x VCI1 voltage level from the step-up circuit 1. Place a stabilizing capacitor between GND. AVDD = 4.5 ~ 5.5V
VGH	1	O	Stabilizing capacitor	An output voltage from the step-up circuit 2x, 4x ~ 6x of the VCI1 level. Connect with a stabilizing capacitor.
VGL	1	O	Stabilizing capacitor	An output voltage from the step-up circuit –2x, -3x ~ -5x of the VCI1 level. Connect with a stabilizing capacitor.
VCL	1	O	Stabilizing capacitor	An output voltage from the step-up circuit 2, –1x of the VCI1 level. Connect with a stabilizing capacitor.
VDD_18V	1	O	Stabilizing capacitor	Reference voltage for Internal logic block Connect with a stabilizing capacitor
VREF	1	O	Stabilizing capacitor	Reference voltage for power block Connect with a stabilizing capacitor.
GVDD	1	I/O	Stabilizing capacitor	Output source driver grayscale reference voltage level.
FB	1	I	Backlight voltage enerator	The feedback voltage from DC-DC
DRV	1	O	DC-DC voltage generator	
Source/Gate Driver and VCOM Signals				
G1~G162	162	O	LCD	Output gate driver signals, which has the swing from VGH to VGL
S1~S396	396	O	LCD	Output source driver signals. The D/A converted 64-gray-scale analog voltage is output.
VCOM	1	O	TFT panel common electrode	Output a square wave signal with the swing from VcomH - VcomL to the common electrode of TFT panel. The alternating cycle can be set to frame inversion or 1-line inversion.
VcomH	1	O	Stabilizing capacitor	Output the high level of VCOM voltage. Connect with a capacitor to stabilize.
VcomL	1	O	Stabilizing capacitor or open	Output the low level of VCOM voltage. Connect with a capacitor to stabilize.
VDDIO	1	I	Stabilizing capacitor	VDDIO input voltage for control pins using
VDD	1	I	Stabilizing capacitor	Power supply Input
VSS				Digital ground pin.
VSSA				Analog ground pin.

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Signal	Pin No.	I/O	Connected with	Function
Misc. Signal				
TE	1	O	MPU	Tearing effect output pin to synchronies MCU to frame writing, activated by S/W command. When this pin is not activated (TE function OFF), this pin is DGND level.
PADA0	1	I		This pin is used for glass break detection
PADB0	1	O		This pin is used for glass break detection
PADA1/PADB1 PADA2/PADB2 PADA3/PADB3 PADA4/PADB4	8			This pin is used for chip attachment detection
TEST	1	T		Test pin. If not used, please open this pin.
TRIM0-9				Test pin. If not used, please open this pin.
Dummy		D		Dummy pin. If not used, please open this pin.

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6. INSTRUCTIONS

6.1. Outline

The SPFD54124B supports 18-bit data bus interface to configure system via accessing command register. When the command register is executed, sending the command information to specify which index register would be accessed and following the data to that control register. Moreover, register accessing operation should cooperate with DC/X, WRX, RDX signal for SPFD54124B to recognize the control instruction. And command instruction can be accomplished using all system interfaces (18-bit, 16-bit, 9-bit, 8-bit 80- or 68-system and SPI)..

6.1.1. System Function Command List and Description

Table 6.1.1 list all the system function command. After the H/W reset by RESX pin or S/W reset by SWRESET command, each internal register becomes default state (Refer "RESET TABLE" section). Commands 10h, 12h, 13h, 20h, 21h, 26h, 28h, 29h, 30h, 33h, 36h (ML parameter only), 37h, 38h and 39h are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09h), Read Display Power Mode (0Ah), Read Display MADCTR (0Bh), Read Display Pixel Format (0Ch), Read Display Image Mode (0Dh), Read Display Signal Mode (0Eh) and Read Display Self Diagnostic Result (0Fh) of these commands are updated immediately both in Sleep In mode and Sleep Out mode.

Table 6.1.1 System Function command List (1)

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)	No Operation
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)	Software reset
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)	Read Display ID
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		ID1 read
	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		ID2 read
	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		ID3 read
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)	Read Display Status
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24		-
	1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON		-
	1	1	↑	-	VSSON	ST14	INVON	ST12	ST11	DISON	TEON	GCS2		-
	1	1	↑	-	GCS1	GCS0	TELOM	HSON	VSON	PCKON	DEON	ST0		-
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)	Read Display Power Mode
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	D1	D0		-
RDD MADCTR	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)	Read Display MADCTR
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	MX	MY	MV	ML	RGB	MH	D1	D0		-
RDD COLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)	Read Display Pixel Format
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	D7	D6	D5	D4	D3	IFPF2	IFPF1	IFPF0		-
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)	Read Display Image Mode
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	VSSON	D6	INVON	D4	D3	GCS2	GCS1	GCS0		-
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)	Read Display Signal Mode
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	TEON	TELOM	HSON	VSON	PCKON	DEON	D1	D0		-
RDDSDR	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)	Read Display Self-diagnostic result
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	RELD	FUND	ATTD	BRD	D3	D2	D1	D0		-

"-": Don' t care, can be set to VDDIO or DGND level

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Table 6.1.1 System Function command List (2)

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)	Sleep in & booster off
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)	Sleep out & booster on
PTLON	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)	Partial mode on
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)	Partial off (Normal)
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)	Display inversion off (normal)
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)	Display inversion on
GAMSET	0	↑	1	-	0	0	1	0	0	1	1	0	(26h)	Gamma curve select
	1	↑	1	-	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0		-
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)	Display off
DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)	Display on
CASET	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)	Column address set
	1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8		X address start: 0 ≤ XS ≤ 0x83
	1	↑	1	-	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0		
	1	↑	1	-	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8		X address end: XS ≤ XE ≤ 0x83
	1	↑	1	-	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0		
RASET	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)	Row address set
	1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8		Y address start: 0 ≤ YS ≤ 0xA1
	1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0		
	1	↑	1	-	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8		Y address end: YS ≤ YE ≤ 0xA1
	1	↑	1	-	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0		
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)	Memory write
	1	↑	1	D17-8	D7	D6	D5	D4	D3	D2	D1	D0		Write data
RAMHD	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)	Memory read
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	D17-8	D7	D6	D5	D4	D3	D2	D1	D0		Read data
RGBSET	0	↑	1	-	0	0	1	0	1	1	0	1	(2Dh)	LUT for 4k,65k , 262K color display
	1	↑	1	-	R007	R006	R005	R004	R003	R002	R001	R000		Red tone 0
	1	↑	1	-	:	:	:	:	:	:	:	:		: -
	1	↑	1	-	Ra7	Ra6	Ra5	Ra4	Ra3	Ra2	Ra1	Ra0		Red tone “31”
	1	↑	1	-	G007	G006	G005	G004	G003	G002	G001	G000		Green tone 0
	1	↑	1	-	:	:	:	:	:	:	:	:		: -
	1	↑	1	-	Gb7	Gb6	Gb5	Gb4	Gb3	Gb2	Gb1	Gb0		Green tone “63”
	1	↑	1	-	B007	B006	B005	B004	B003	B002	B001	B000		Blue tone 0
	1	↑	1	-	:	:	:	:	:	:	:	:		: -
	1	↑	1	-	Bc7	Bc6	Bc5	Bc4	Bc3	Bc2	Bc1	Bc0		Blue tone “31”

“-“: Don’t care, can be set to VDDIO or DGND level

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Table 6.1.1 System Function command List (3)

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
PTLAR	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)	Partial start/end address set
	1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8		Partial start address (0,1,2, .., 161)
	1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0		
	1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8		Partial end address (0,1,2, .., 161)
	1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0		
SCRLAR	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)	Scroll area set
	1	↑	1	-	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8		Top fixed area (0,1,2, .., 161)
	1	↑	1	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0		
	1	↑	1	-	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8		Vertical scroll area (0,1,2, .., 161)
	1	↑	1	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0		
	1	↑	1	-	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8		Bottom fixed area (0,1,2, .., 161)
	1	↑	1	-	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0		
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)	Tearing effect line off
TEON	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)	Tearing effect mode set & on
	1	↑	1	-	0	0	0	0	0	0	0	TELOM		M="0": Mode1, M="1": Mode2
MADCTR	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)	Memory data access control
	1	↑	1	-	MY	MX	MV	ML	RGB	MH	0	0		-
VSCSAD	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)	Scroll start address of RAM
	1	↑	1	-	SSA15	SSA14	SSA13	SSA12	SSA11	SSA10	SSA9	SSA8		SSA = 0, 1, 2, …, 161
	1	↑	1	-	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0		
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)	Idle mode off
IDMON	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)	Idle mode on
COLMOD	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)	Interface pixel format
	1	↑	1	-	0	0	0	0	0	IFPF2	IFPF1	IFPF0		Interface format
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)	Read ID1
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		Read parameter
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)	Read ID2
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		Read parameter
RDID3	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)	Read ID3
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		Read parameter

"-": Don't care, can be set to VDDIO or DGND level

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6.1.2. Panel Function Command List and Description

Table 6.1.2 list all the panel function command. Panel function command is only accessible when EXTC is pulled high state (by VDDIO).

Table 6.1.2 Panel Function command List (1)

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
RGBCTR	0	↑	1	-	1	0	1	1	0	0	0	0	(B0h)	Set RGB signal control ICM: RGB data ascess select DW: RGB interface bus width set DP,HSP,VSP:PCLK,HS,VS polarity set
	1	↑	1	-	0	0	ICM	DW	DP	EP	HSP	VSP		
FRMCTR1	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)	In normal mode (Full colors) FP0: Front porch in normal mode BP0: Back porch in normal mode RTN0: Number of clock / one line
	1	↑	1	-	-	-	-	-	FP0 [3]	FP0 [2]	FP0 [1]	FP0 [0]		
	1	↑	1	-					BP0 [3]	BP0 [2]	BP0 [1]	BP0 [0]		
	1	↑	1	-					RTN0 [3]	RTN0 [2]	RTN0 [1]	RTN0 [0]		
FRMCTR2	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)	In Idle mode (8-colors) FP1: Front porch in idle mode BP1: Back porch in idle mode RTN1: Number of clock / one line
	1	↑	1	-					FP1 [3]	FP1 [2]	FP1 [1]	FP1 [0]		
	1	↑	1	-					BP1 [3]	BP1 [2]	BP1 [1]	BP1 [0]		
	1	↑	1	-					RTN1 [3]	RTN1 [2]	RTN1 [1]	RTN1 [0]		
FRMCTR3	0	↑	1	-	1	0	1	1	0	0	1	1	(B3h)	In partial mode + Full colors FP2: Front porch in partial mode BP2: Back porch in partial mode RTN2: Number of clock / one line
	1	↑	1	-					FP2 [3]	FP2 [2]	FP2 [1]	FP2 [0]		
	1	↑	1	-					BP2 [3]	BP2 [2]	BP2 [1]	BP2 [0]		
	1	↑	1	-					RTN2 [3]	RTN2 [2]	RTN2 [1]	RTN2 [0]		
INVCTR	0	↑	1	-	1	0	1	1	0	1	0	0	(B4h)	Display inversion control NLA, NLB, NLC: set inversion
	1	↑	1	-	0	0	0	0	0	NLA	NLB	NLC		
RGB PRCTR	0	↑	1	-	1	0	1	1	0	1	0	1	(B5h)	RGB I/F Blanking porch setting Vertical back porch in RGB mode
	1	↑	1	-	-	-	-	-	VBP [3]	VBP [2]	VBP [1]	VBP [0]		
DISSET5	0	↑	1	-	1	0	1	1	0	1	1	1	(B6h)	Display function setting NO: the amount of non-overlap SDT: set amount of source delay PT: No display area source/ VCOM/ Gate output control EQ: set EQ period
	1	↑	1	-	0	0	NO1	NO0	SDT1	STD0	EQ1	EQ0		
	1	↑	1	-	0	0	0	0	PTG1	PTG0	PT1	PT0		

"-": Don't care, can be set to VDDIO or DGND level

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Table 6.1.2 Panel Function Command List (2)

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
PWCTR1	0	↑	1	-	1	0	1	1	0	0	0	0	(C0h)	Power control setting VRH: Set the GVDD voltage VC : Set the VCI1 voltage Power control setting
	1	↑	1	-	0	0	0	VRH4	VRH3	VRH2	VRH1	VRH0		
	1	↑	1		0	0	0	0	0	VC2	VC1	VC0		
PWCTR2	0	↑	1	-	1	0	1	1	0	0	0	1	(C1h)	BT: set AVDD/VCL/ VGH/ VGL voltage
	1	↑	1	-	0	0	0	0	0	BT2	BT1	BT0		
PWCTR3	0	↑	1	-	1	0	1	1	0	0	1	0	(C2h)	n normal mode (Full colors) APA: adjust the operational amplifier DCA: adjust the booster circuit for Idle mode
	1	↑	1	-	0	0	0	0	0	APA2	APA1	APA0		
	1	↑	1	-	0	0	0	0	0	DCA2	DCA1	DCA0		
PWCTR4	0	↑	1	-	1	0	1	1	0	0	1	1	(C3h)	In Idle mode (8-colors) APB: adjust the operational amplifier DCB: adjust the booster circuit for Idle mode I
	1	↑	1	-	0	0	0	0	0	APB2	APB1	APB0		
	1	↑	1	-	0	0	0	0	0	DCB2	DCB1	DCB0		
PWCTR5	0	↑	1	-	1	0	1	1	0	1	0	0	(C4h)	In partial mode + Full colors APC: adjust the operational amplifier DCC: adjust the booster circuit for Idle mode
	1	↑	1	-	0	0	0	0	0	APC2	APC1	APC0		
	1	↑	1	-	0	0	0	0	0	DCC2	DCC1	DCC0		
VMCTR1	0	↑	1	-	1	0	1	1	0	1	0	1	(C5h)	VCOM control 1 nVM: VCOM input select VMH: VCOMH voltage control
	1	↑	1	-	nVM	VMH6	VMH 5	VMH4	VMH3	VMH2	VMH1	VMH0		
VMCTR2	0	↑	1	-	1	0	1	1	0	1	1	0	(C6h)	VCOM control 2 VMA: VCOMAC voltage control
	1	↑	1	-	0	0	VMA5	VMA4	VMA3	VMA2	VMA1	VMA0		
	1	↑	1	-	nVM	VMF6	VMF5	VMF4	VMF3	VMF2	VMF1	VMF0		
RVMOF CTR	0	**1**	↑	-	1	0	1	1	1	0	0	0	(C8h)	VCOM control 4 Read the VMOF value form NV memory
	1	**1**	↑	-	nVM	RVMF 6	RVMF 5	RVMF 4	RVMF 3	RVMF 2	RVMF 1	RVMF 0		

"-": Don't care, can be set to VDDIO or DGND level

Table 6.1.2 Panel Function Command List (3)

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
WRID1	0	↑	1	-	1	1	0	1	0	0	0	1	(D0h)	Panel ID code Write ID1 value to NV memory Set the LCM ID code at ID1
	1	↑	1	-	1	ID16	ID15	ID14	ID13	ID12	ID11	ID10		
WRID2	0	↑	1	-	1	1	0	1	0	0	0	1	(D1h)	Panel version code Write ID2 value to NV memory Set the LCM version code at ID2
	1	↑	1	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20		
WRID3	0	↑	1	-	1	1	0	1	0	0	1	0	(D2h)	Driver maker Project code Write ID3 value to NV memory Set the project code at ID3
	1	↑	1	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		
RDID4	0	↑	1	-	1	1	0	1	0	0	1	1	(D3h)	IC Vender Coder Dummy read ID41:IC Vender Coder ID42: IC Part Number Coder ID43 & ID44: Chip version coder
	1	1	↑	-	-	-	-	-	-	-	-	-		
	1	1	↑	-	ID417	ID416	ID415	ID414	ID413	ID412	ID411	ID410		
	1	1	↑	-	ID427	ID426	ID425	ID424	ID423	ID422	ID421	ID420		
	1	1	↑	-	ID437	ID436	ID435	ID434	ID43	ID432	ID431	ID430		
	1	1	↑	-	ID447	ID446	ID445	ID444	ID443	ID442	ID441	ID440		
NVCTR1	0	↑	1	-	1	1	0	1	1	0	0	1	(D9h)	NV memory function controller 1 Please refer to 'OTP programming procedure' for details.
				-										
NVCTR2	0	↑	1	-	1	1	0	1	1	1	1	0	(DEh)	NV memory function controller 2 Please refer to 'OTP programming procedure' for details.
	1	↑	1	-										
NVCTR3	0	↑	1	-	1	1	0	1	1	1	1	1	(DFh)	NV memory function controller 3 Please refer to 'OTP programming procedure' for details.
	1	↑	1	-										

"-": Don't care, can be set to VDDIO or DGND level

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Table 6.1.2 Panel Function Command List (4)

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
GAMCTRP1	0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)	Gamma adjustment
	1	↑	1	-	-	-	-	PVR1V0[4]	PVR1V0[3]	PVR1V0[2]	PVR1V0[1]	PVR1V0[0]		
	1	↑	1	-	-	-	PVR1V1[5]	PVR1V1[4]	PVR1V1[3]	PVR1V1[2]	PVR1V1[1]	PVR1V1[0]		
	1	↑	1	-	-	-	PVR1V2[5]	PVR1V2[4]	PVR1V2[3]	PVR1V2[2]	PVR1V2[1]	PVR1V2[0]		
	1	↑	1	-	-	-	PVR1V61[5]	PVR1V61[4]	PVR1V61[3]	PVR1V61[2]	PVR1V61[1]	PVR1V61[0]		
	1	↑	1	-	-	-	PVR1V62[5]	PVR1V62[4]	PVR1V62[3]	PVR1V62[2]	PVR1V62[1]	PVR1V62[0]		
	1	↑	1	-	-	-	-	PVR1V63[4]	PVR1V63[3]	PVR1V63[2]	PVR1V63[1]	PVR1V63[0]		
	1	↑	1	-	-	-	-	PVR2V13[4]	PVR2V13[3]	PVR2V13[2]	PVR2V13[1]	PVR2V13[0]		
	1	↑	1	-	-	-	-	PVR2V50[4]	PVR2V50[3]	PVR2V50[2]	PVR2V50[1]	PVR2V50[0]		
	1	↑	1	-	-	-	-	-	PVR3V4[3]	PVR3V4[2]	PVR3V4[1]	PVR3V4[0]		
	1	↑	1	-	-	-	-	-	PVR3V8[3]	PVR3V8[2]	PVR3V8[1]	PVR3V8[0]		
	1	↑	1	-	-	-	-	-	PVR3V20[3]	PVR3V20[2]	PVR3V20[1]	PVR3V20[0]		
	1	↑	1	-	-	-	-	-	PVR3V27[3]	PVR3V27[2]	PVR3V27[1]	PVR3V27[0]		
	1	↑	1	-	-	-	-	-	PVR3V36[3]	PVR3V36[2]	PVR3V36[1]	PVR3V36[0]		
	1	↑	1	-	-	-	-	-	PVR3V43[3]	PVR3V43[2]	PVR3V43[1]	PVR3V43[0]		
	1	↑	1	-	-	-	-	-	PVR3V55[3]	PVR3V55[2]	PVR3V55[1]	PVR3V55[0]		
	1	↑	1	-	-	-	-	-	PVR3V59[3]	PVR3V59[2]	PVR3V59[1]	PVR3V59[0]		

"-": Don't care, can be set to VDDIO or DGND level

Table 6.1.2 Panel Function Command List (5)

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
GAMCTRN1	0	↑	1	-	1	1	1	0	0	0	0	1	(E1h)	Gamma adjustment
	1	↑	1	-	-	-	-	NVR1V0[4]	NVR1V0[3]	NVR1V0[2]	NVR1V0[1]	NVR1V0[0]		
	1	↑	1	-	-	-	NVR1V1[5]	NVR1V1[4]	NVR1V1[3]	NVR1V1[2]	NVR1V1[1]	NVR1V1[0]		
	1	↑	1	-	-	-	NVR1V2[5]	NVR1V2[4]	NVR1V2[3]	NVR1V2[2]	NVR1V2[1]	NVR1V2[0]		
	1	↑	1	-	-	-	NVR1V61[5]	NVR1V61[4]	NVR1V61[3]	NVR1V61[2]	NVR1V61[1]	NVR1V61[0]		
	1	↑	1	-	-	-	NVR1V62[5]	NVR1V62[4]	NVR1V62[3]	NVR1V62[2]	NVR1V62[1]	NVR1V62[0]		
	1	↑	1	-	-	-	-	NVR1V63[4]	NVR1V63[3]	NVR1V63[2]	NVR1V63[1]	NVR1V63[0]		
	1	↑	1	-	-	-	-	NVR2V13[4]	NVR2V13[3]	NVR2V13[2]	NVR2V13[1]	NVR2V13[0]		
	1	↑	1	-	-	-	-	NVR2V50[4]	NVR2V50[3]	NVR2V50[2]	NVR2V50[1]	NVR2V50[0]		
	1	↑	1	-	-	-	-	-	NVR3V4[3]	NVR3V4[2]	NVR3V4[1]	NVR3V4[0]		
	1	↑	1	-	-	-	-	-	NVR3V8[3]	NVR3V8[2]	NVR3V8[1]	NVR3V8[0]		
	1	↑	1	-	-	-	-	-	NVR3V20[3]	NVR3V20[2]	NVR3V20[1]	NVR3V20[0]		
	1	↑	1	-	-	-	-	-	NVR3V27[3]	NVR3V27[2]	NVR3V27[1]	NVR3V27[0]		
	1	↑	1	-	-	-	-	-	NVR3V36[3]	NVR3V36[2]	NVR3V36[1]	NVR3V36[0]		
	1	↑	1	-	-	-	-	-	NVR3V43[3]	NVR3V43[2]	NVR3V43[1]	NVR3V43[0]		
	1	↑	1	-	-	-	-	-	NVR3V55[3]	NVR3V55[2]	NVR3V55[1]	NVR3V55[0]		
	1	↑	1	-	-	-	-	-	NVR3V59[3]	NVR3V59[2]	NVR3V59[1]	NVR3V59[0]		

"-": Don't care, can be set to VDDIO or DGND level

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6.2. System Command Description

6.2.1. NOP (00h)

00H	NOP (No Operation)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)
Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDIO or DGND level, can be set to VDDIO or DGND level

Description	-This command is empty command. It does not have effect on the display module. -However it can be used to terminate RAM data write or read as described in RAMWR (Memory Write), RAMHD (Memory Read) and parameter write commands.
Restriction	-
Register Availability	Status / Availability: Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status / Default Value: Power On Sequence: N/A S/W Reset: N/A H/W Reset: N/A
Flow Chart	-

6.2.2. SWRESET (01h): Software Reset

01H	SWRESET (Software Reset)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)
Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description	-When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values and all source outputs are set to DGND (display off). (See default tables in each command description) *Note: The Frame Memory contents are not affected by this command.*
Restriction	-It will be necessary to wait 5msec before sending new command following software reset. -The display module loads all display supplier's factory default values to the registers during 5msec. -If Software Reset is applied during Sleep Out mode, it will be necessary to wait *120msec* before sending Sleep Out command. -Software Reset command cannot be sent during Sleep Out sequence.
Register Availability	Status / Availability: Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes

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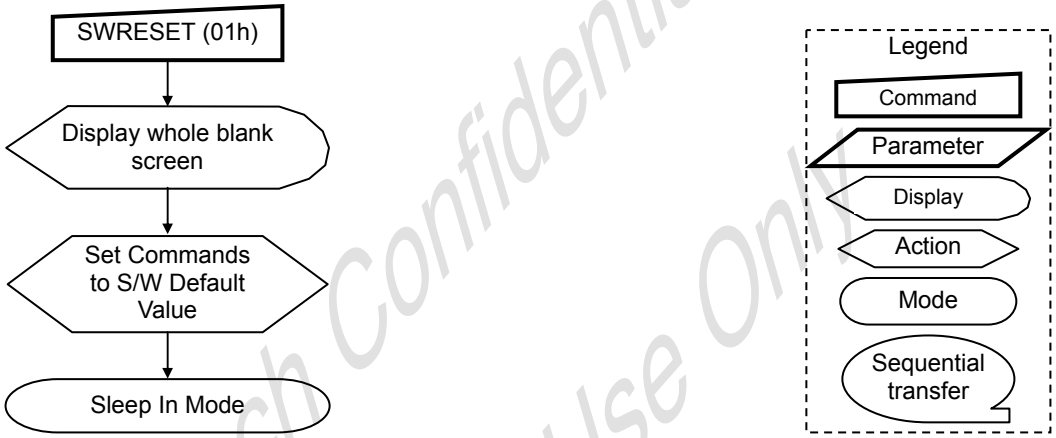
Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart



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6.2.3. RDDID (04h): Read Display ID

04H	RDDID (Read Display ID)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	
3rd Parameter	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
4th Parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

-This read byte returns 24-bits display identification information.

-The 1st parameter is dummy data

-The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID.

-The 3rd parameter (ID27 to ID20): LCD module/driver version ID

-The 4th parameter (ID37 to UD30): LCD module/driver ID.

NOTE: Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 2,3,4 of the command 04h, respectively.

Restriction

-

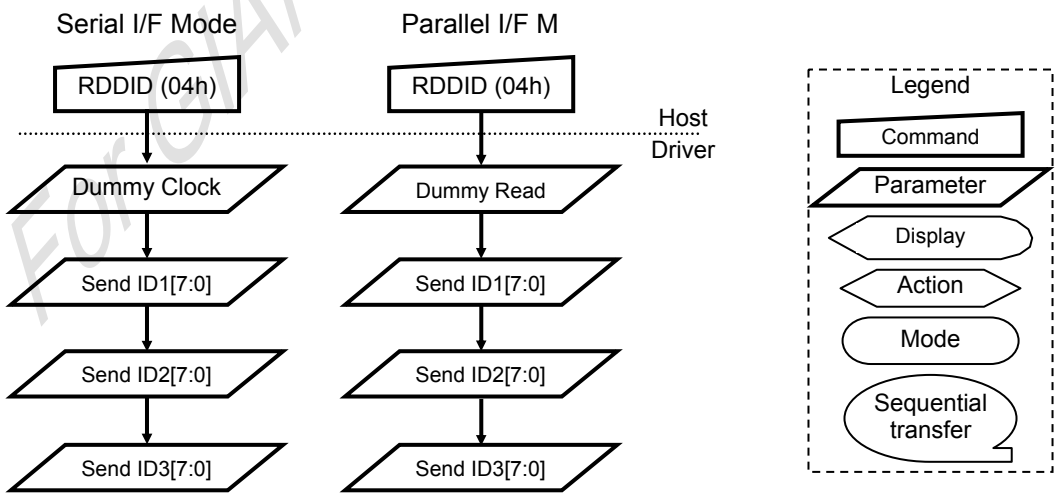
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	ID1	ID2	ID3
Power On Sequence	38h	8xh	4Fh
S/W Reset	38h	8xh	4Fh
H/W Reset	38h	8xh	4Fh

Flow Chart



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6.2.4. RDDST (09h): Read Display Status

09H	RDDST (Read Display Status)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24	
3rd Parameter	1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON	
4th Parameter	1	1	↑	-	VSSON	ST14	INVON	ST12	ST11	DISON	TEON	GCS2	
5th Parameter	1	1	↑		GCS1	GCS0	TELOM	HSON	VSON	PCKON	DEON	ST0	

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
BSTON	Booster Voltage Status	'1' =Booster on, '0' =Booster off
MY	Row Address Order (MY)	'1' =Decrement, (Bottom to Top, when MADCTL (36h) D7='1') '0' =Increment, (Top to Bottom, when MADCTL (36h) D7='0')
MX	Column Address Order (MX)	'1' =Decrement, (Right to Left, when MADCTL (36h) D6='1') '0' =Increment, (Left to Right, when MADCTL (36h) D6='0')
MV	Row/Column Exchange (MV)	'1' = Row/column exchange, (when MADCTL (36h) D5='1') '0' = Normal, (when MADCTL (36h) D5='0')
ML	Vertical Refresh Order (ML)	'1' =Decrement, (LCD refresh Bottom to Top, when MADCTL (36h) D4='1') "0"=Increment, (LCD refresh Top to Bottom, when MADCTL (36h) D4='0')
RGB	RGB/ BGR Order (RGB)	'1' =BGR, (When MADCTL (36h) D3='1') '0' =RGB, (When MADCTL (36h) D3='0')
MH	Horizontal Order (MH)	'1' =Decrement, (LCD refresh Right to Left, when MADCTL (36h) D2='1') '0' =Increment, (LCD refresh Left to Right, when MADCTL (36h) D2='0')
ST24	For Future Use	'0'
ST23	For Future Use	'0'
IFPF2 IFPF1 IFCPF0	Interface Color Pixel Format Definition	"011" = 12-bits / pixel, "101" = 16-bits / pixel, "110" = 18-bits / pixel,others are no define
IDMON	Idle Mode On/Off	'1' = On, "0" = Off
PTLON	Partial Mode On/Off	'1' = On, "0" = Off
SLPOUT	Sleep In/Out	'1' = Out, "0" = In
NORON	Display Normal Mode On/Off	'1' = Normal Display, '0' = Partial Display
VSSON	Vertical Scrolling Status	'1' = Scroll on,"0" = Scroll off
ST14	Horizontal Scroll Status	'0'
INVON	Inversion Status	'1' = On, "0" = Off
ST12	All Pixels On (Not Used)	'0'
ST11	All Pixels Off (Not Used)	'0'
DISON	Display On/Off	'1' = On, "0" = Off
TEON	Tearing effect line on/off	'1' = On, "0" = Off
GCSEL2 GCSEL1 GCSEL0	Gamma Curve Selection	"000" = GC0 "001" = GC1 "010" = GC2 "011" = GC3 "100" to "111" = Not defined
TELOM	Tearing effect line mode	'0' = mode1, '1' = mode2
HSON	Horizontal Sync. (HS)	'1' = On, '0' = Off
VSON	Vertical Sync, (VS, RGB I/F)	'1' = On, '0' = Off
PCLKON	Pixel Clock (PCLK, RGB I/F)	'1' = On, '0' = Off
DEON	Data Enable (DE, RGB I/F)	'1' = On, '0' = Off
ST0	For Future Use	'0'

Note: ST0, ST11-ST12, ST14, ST23, ST24 are set to '0'

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Restriction	-

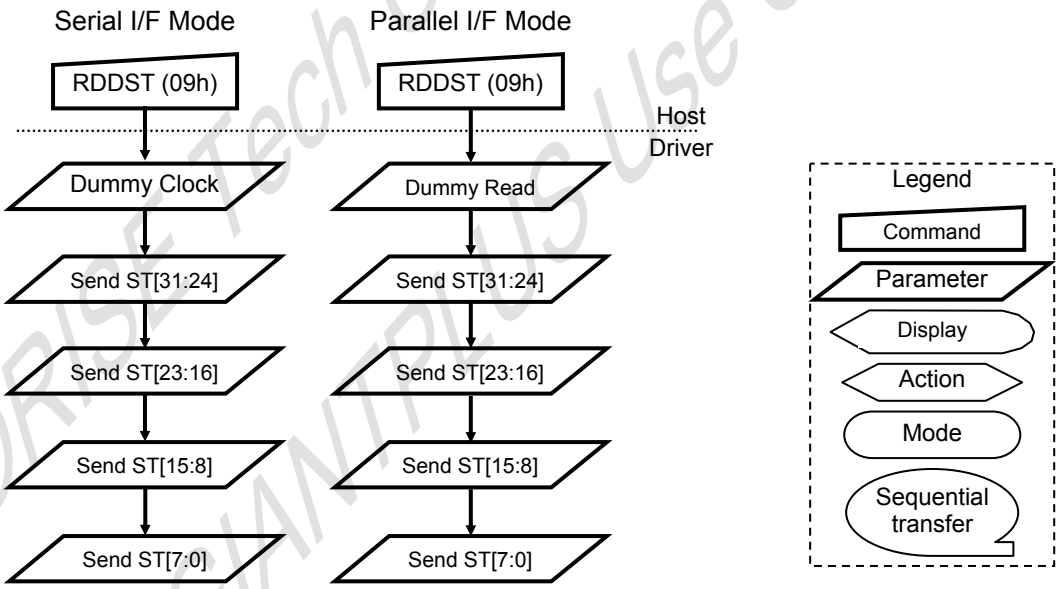
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (ST31 to ST0)			
	ST[31-24]	ST[23-16]	ST[15-8]	ST[7-0]
Power On Sequence	0000-0000	0110-0001	0000-0000	0000-0000
S/W Reset	0xxx-xx00	0xxx-0001	0000-0000	0000-0000
H/W Reset	0000-0000	0110-0001	0000-0000	0000-0000

Flow Chart



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6.2.5. RDDPM (0Ah): Read Display Power Mode

0AH	RDDPM (Read Display Power Mode)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑		BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	D1	D0	

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
BSTON	Booster Voltage Status	"1"=Booster on, "0"=Booster off
IDMON	Idle Mode On/Off	"1" = Idle Mode On, "0" = Idle Mode Off
PTLON	Partial Mode On/Off	"1" = Partial Mode On, "0" = Partial Mode Off
SLPON	Sleep In/Out	"1" = Sleep Out, "0" = Sleep In
NORON	Display Normal Mode On/Off	"1" = Normal Display, "0" = Partial Display
DISON	Display On/Off	"1" = Display On, "0" = Display Off
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

-

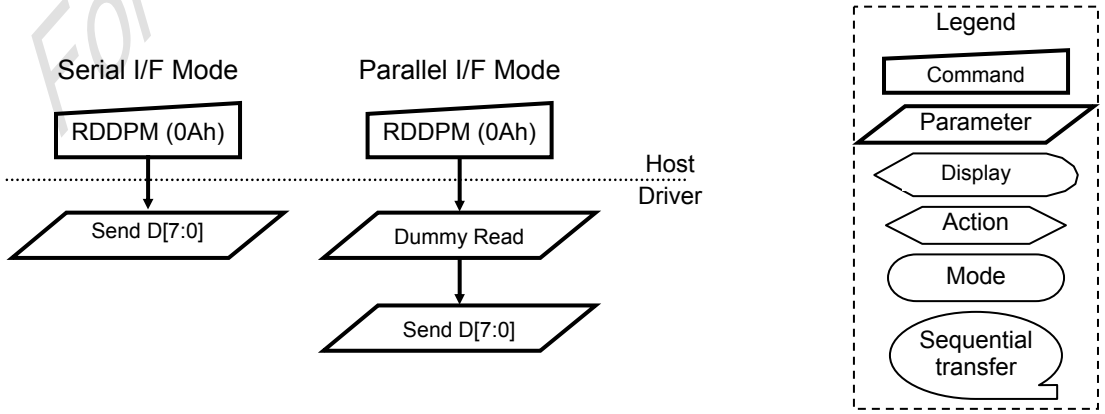
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_1000 (08h)
S/W Reset	0000_1000 (08h)
H/W Reset	0000_1000 (08h)

Flow Chart



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6.2.6. RDDMADCTR (0Bh): Read Display MADCTR

0BH	RDDMADCTR (Read Display MADCTR)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDMADCTR	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑		MX	MY	MV	ML	RGB	MH	D1	D0	

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
MX	Row Address Order	'1' = Bottom to Top (When MADCTL B7='1') '0' = Top to Bottom (When MADCTL B7='0')
MY	Column Address Order	'1' = Right to Left (When MADCTL B6='1') '0' = Left to Right (When MADCTL B6='0')
MV	Row/Column Order (MV)	'1' = Row/column exchange (MV=1) '0' = Normal (MV=0)
ML	Vertical Refresh Order	'1' =LCD Refresh Bottom to Top '0' =LCD Refresh Top to Bottom
RGB	RGB/BGR Order	'1' =BGR, "0"=RGB
MH	Horizontal order	'1' =LCD Refresh Right to Left '0' =LCD Refresh Left to Right
D1	Not Used	'0'
D0	Not Used	'0'

Restriction

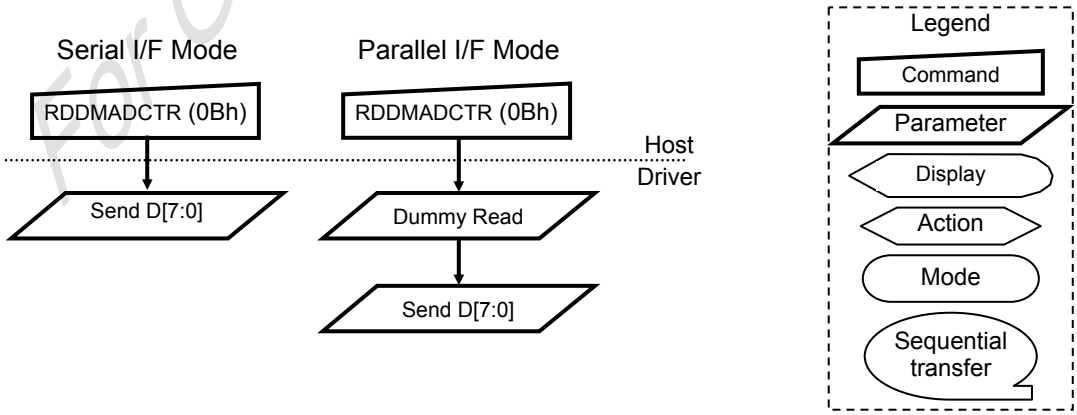
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	No change
H/W Reset	0000_0000 (00h)

Flow Chart



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6.2.7. RDDCOLMOD (0Ch): Read Display Pixel Format

0CH	RDDCOLMOD (Read Display Pixel Format)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDCOLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	VIPF3	VIPF2	VIPF1	VIPF0	D3	IFPF2	IFPF1	IFPF0	

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

-This command indicates the current status of the display as described in the table below:

IFPF[2:0]		MCU Interface Color Format
011	3	12-bits/pixel
101	5	16-bits/pixel
110	6	18-bits/pixel
111	7	No used

Others are no define and invalid

VIPF[3:0]		RGB Interface Color Format
0101	5	16-bits/pixel (1-times data transfer)
0110	6	18-bits/pixel (1-times data transfer)
0111	7	No used
1110	14	18-bits/pixel (3-times data transfer)

Others are no define and invalid

Restriction

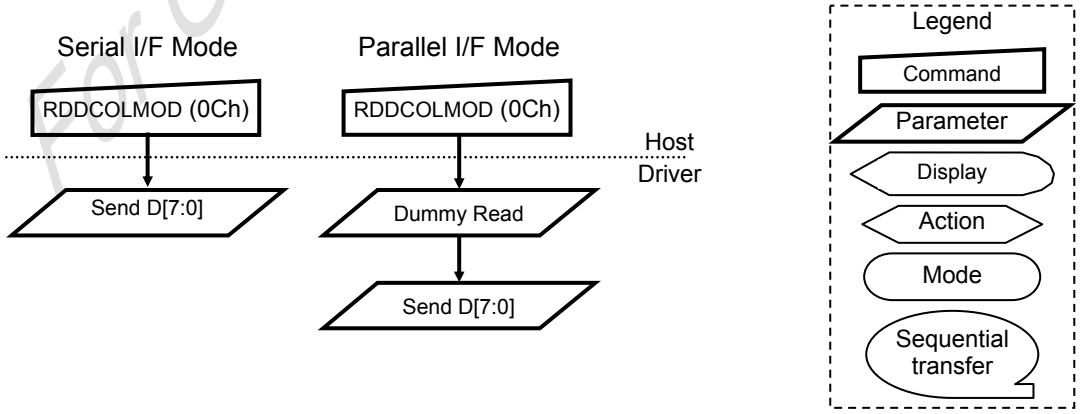
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	IFPF[2:0]	VIPF[3:0]
Power On Sequence	0110 (18-bits/pixel)	0110 (18-bits/pixel)
S/W Reset	No Change	No Change
H/W Reset	0110 (18-bits/pixel)	0110 (18-bits/pixel)

Flow Chart



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6.2.8. RDDIM (0Dh): Read Display Image Mode

0DH	RDDIM (0Dh): Read Display Image Mode												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	VSSON	D6	INVON	D4	D3	GCS2	GCS1	GCS0	

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
VSSON	Vertical Scrolling On/Off	"1" = Vertical scrolling is On, "0" = Vertical scrolling is Off
D6	Horizontal Scrolling On/Off	"0" (Not used)
INVON	Inversion On/Off	"1" = Inversion is On, "0" = Inversion is Off
D4	All Pixels On	"0" (Not used)
D3	All Pixels Off	"0" (Not used)
GCS2 GCS1 GCS0	Gamma Curve Selection	"000" = GC0, "001" = GC1, "010" = GC2, "011" = GC3, "100" to "111" = Not defined

Restriction

-

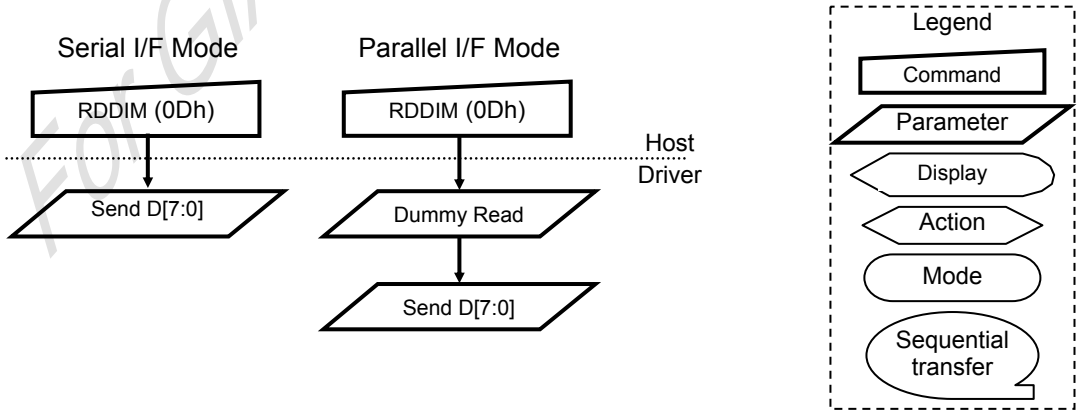
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)
H/W Reset	0000_0000 (00h)

Flow Chart



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6.2.9. RDDSM (0Eh): Read Display Signal Mode

0EH	RDDSM (0Eh): Read Display Signal Mode												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	TEON	TELOM	HSON	VSON	PCKON	DEON	D1	D0	

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
TEON	Tearing Effect Line On/Off	"1" = On, "0" = Off
TELOM	Tearing effect line mode	"0" = mode1, "1" = mode2
HSON	Horizontal Sync. (RGB I/F) On/Off	"1" = On, "0" = Off
VSON	Vertical Sync. (RGB I/F) On/Off	"1" = On, "0" = Off
PCKON	Pixel Clock (PCLK, RGB I/F) On/Off	"1" = On, "0" = Off
DEON	Data Enable (DE, RGB I/F) On/Off	"1" = On, "0" = Off
D1	Not Used	"1" = On, "0" = Off
D0	Not Used	"1" = On, "0" = Off

Restriction

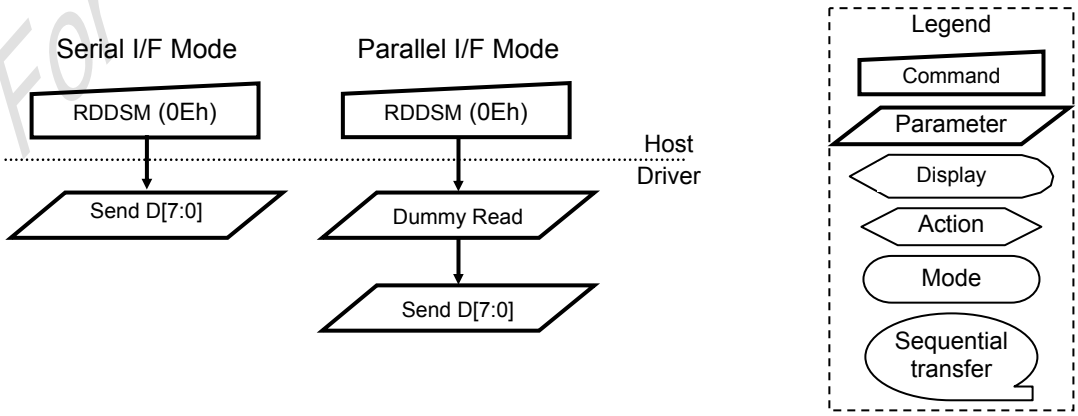
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)
H/W Reset	0000_0000 (00h)

Flow Chart



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6.2.10. RDDSDR (0Fh): Read Display Self-Diagnostic Result

0FH	RDDSDR (0Fh): Read Display Self-Diagnostic Result												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDSDR	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	RELD	FUND	ATTD	BRD	D3	D2	D1	D0	

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
RELD	Register Loading Detection	
FUND	Functionality Detection	
ATTD	Chip Attachment Detection	
BRD	Display Glass Break Detection	
D3	Not Used	"0"
D2	Not Used	"0"
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

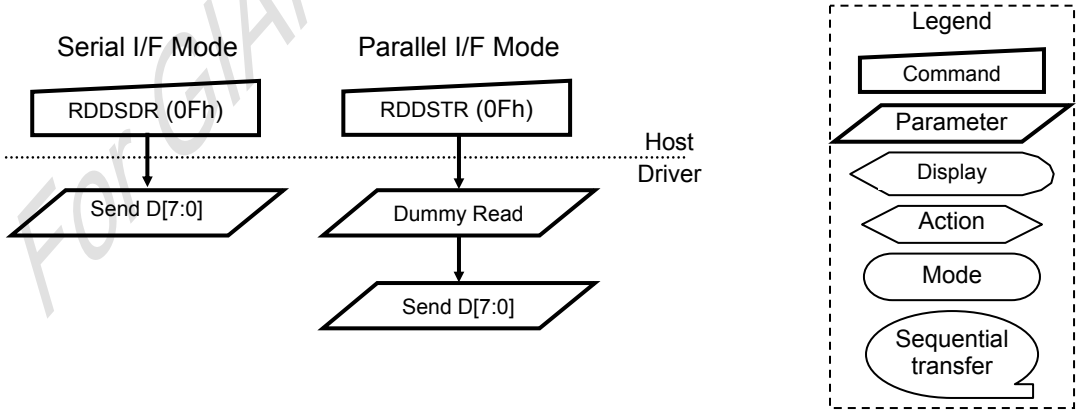
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)
H/W Reset	0000_0000 (00h)

Flow Chart



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6.2.11. SLPIN (10h): Sleep In

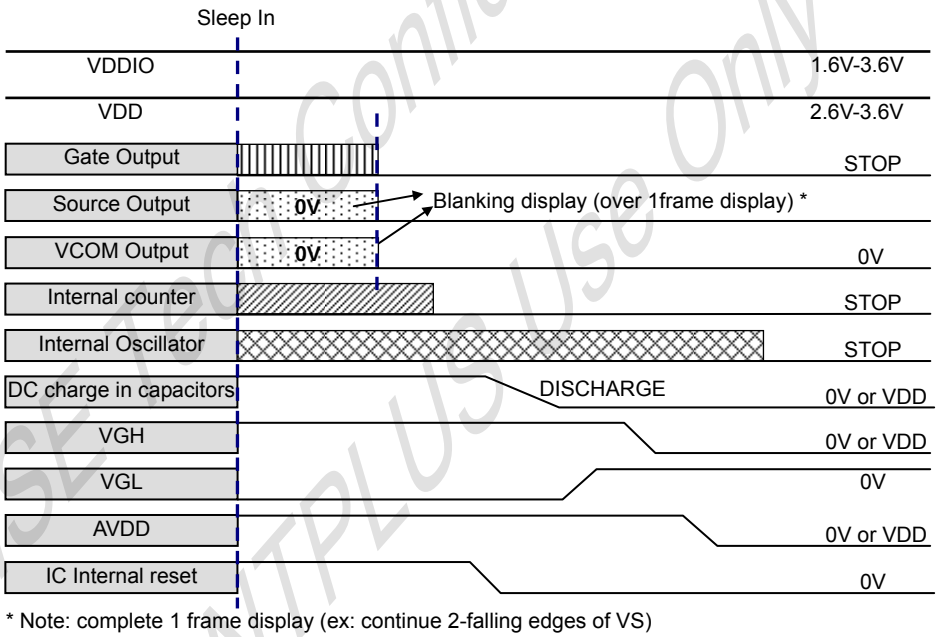
10H	SLPIN (Sleep In)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)
1st Parameter	No parameter												-

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

-This command causes the LCD module to enter the minimum power consumption mode.

-In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.



* Note: complete 1 frame display (ex: continue 2-falling edges of VS)

-MCU interface and memory are still working and the memory keeps its contents

Restriction

-This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11h).

-It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.

-It will be necessary to wait *120msec* after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

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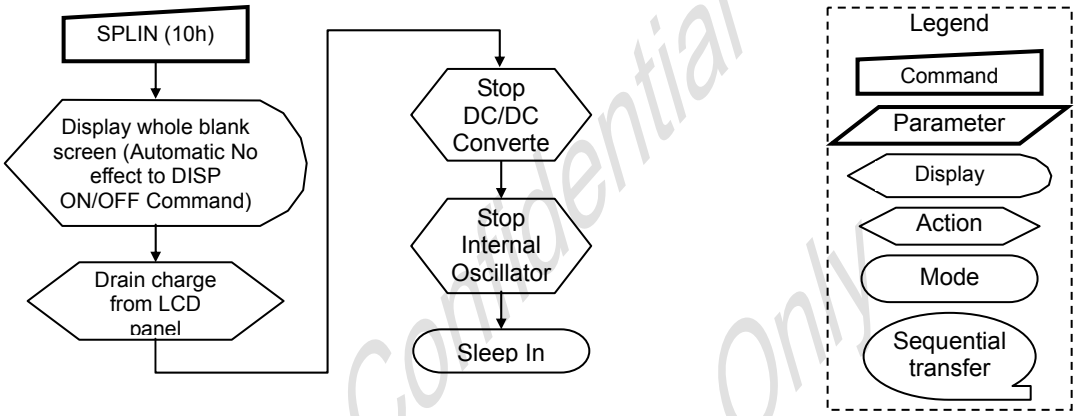
Flow Chart	-It takes about 120msec to get into Sleep In mode (booster off state) after SLPIN command issued. -The results of booster off can be check by RDDST (09h) command Bit31. 

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6.2.12. SLPOUT (11h): Sleep Out

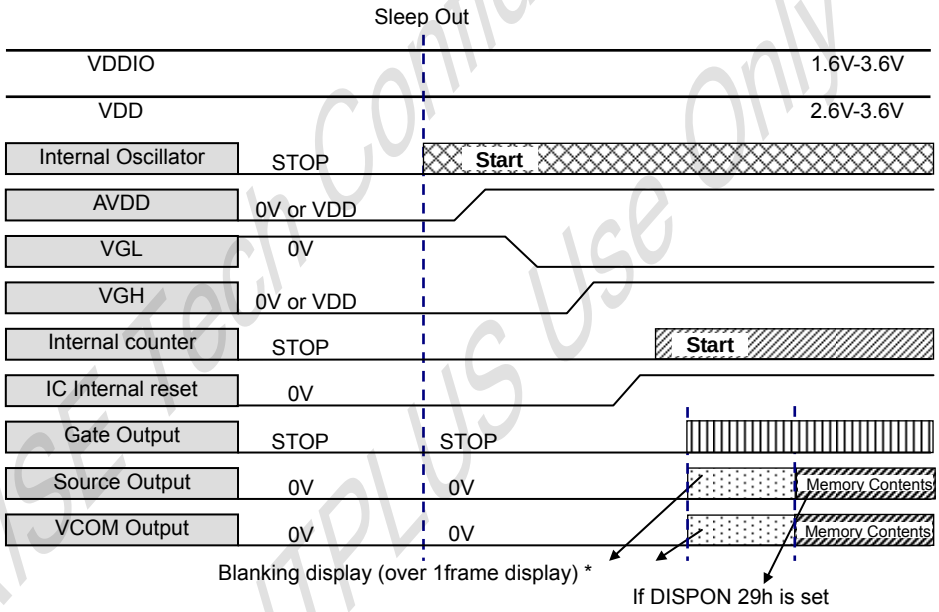
11H	SLPOUT (Sleep Out)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

-This command turns off sleep mode.

-In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.



* Note: complete 1 frame display (ex: continue 2-falling edges of VS)

Restriction

-This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10h).

-It will be necessary to wait *5msec* before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.

-DRIVER loads all default values of extended and test command to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if those default and register values are same when this load is done and when the DRIVER is already Sleep Out mode.

-DRIVER is doing self-diagnostic functions during this *5msec*.

-It will be necessary to wait *120msec* after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

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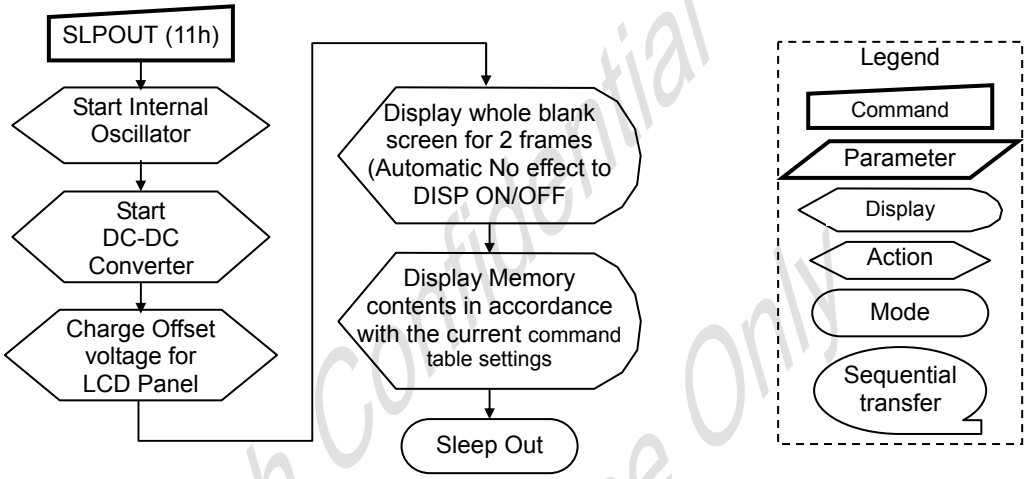
Flow Chart	-It takes 120msec to become Sleep Out mode (booster on mode) after SLPOUT command issued. -The results of booster on can be checked by RDDST (09h) command Bit31. 

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6.2.13. PTLON (12h): Partial Display Mode On

12H	PTLON (12h): Partial Display Mode On												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PTLON	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description	-This command turns on Partial mode. The partial mode window is described by the Partial Area command (30h) -To leave Partial mode, the Normal Display Mode On command (13H) should be written. -There is no abnormal visual effect during mode change between Normal mode On <-> Partial mode On.
Restriction	This command has no effect when Partial mode is active.
Register Availability	Status / Availability: Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status / Default Value: Power On Sequence: Normal Mode On S/W Reset: Normal Mode On H/W Reset: Normal Mode On
Flow Chart	See Partial Area (30h)

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6.2.14. NORON (13h): Normal Display Mode On

13H	NORON (Normal Display Mode On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description	-This command returns the display to normal mode. -Normal display mode on means Partial mode off, Scroll mode Off. -Exit from NORON by the Partial mode On command (12h) -There is no abnormal visual effect during mode change from Normal mode On to Partial mode On.
Restriction	-This command has no effect when Normal Display mode is active.
Register Availability	Status / Availability: Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status / Default Value: Power On Sequence: Normal Mode On S/W Reset: Normal Mode On H/W Reset: Normal Mode On
Flow Chart	-See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command

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6.2.15. INVOFF (20h): Display Inversion Off

20H	INVOFF (Display Inversion Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)
1st Parameter	No Parameter												-

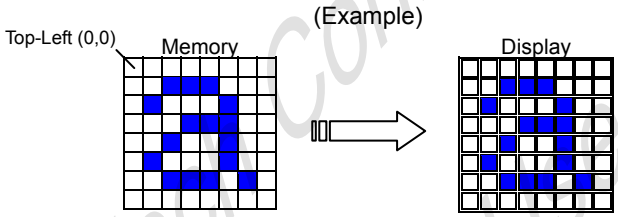
NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

-This command is used to recover from display inversion mode.

-This command makes no change of contents of frame memory.

-This command does not change any other status.



Restriction

-This command has no effect when module is already inversion off mode.

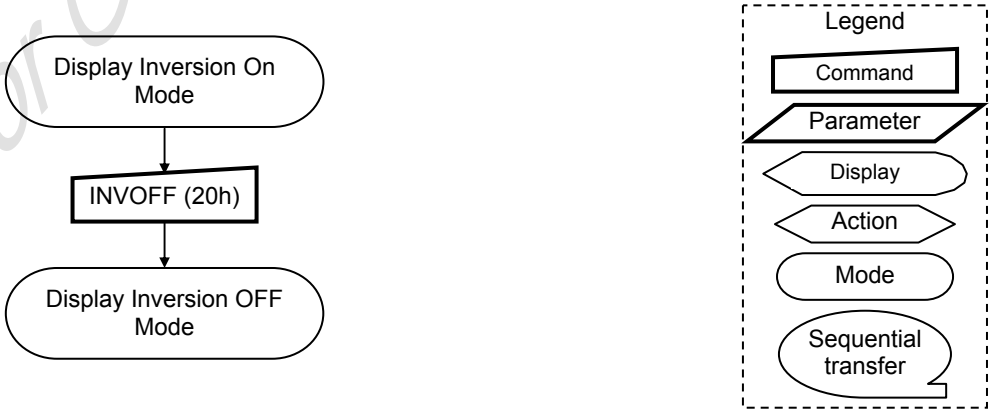
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

Flow Chart



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6.2.16. INVON (21h): Display Inversion On

21H	INVON (Display Inversion On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

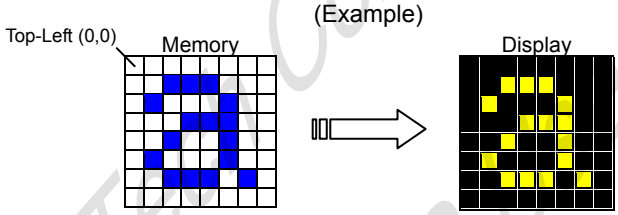
-This command is used to enter into display inversion mode

-This command makes no change of contents of frame memory.

-This command does not change any other status.

-To exit from Display Inversion On, the Display Inversion Off command (20h) should be written.

(Example)



Restriction

-This command has no effect when module is already Inversion On mode.

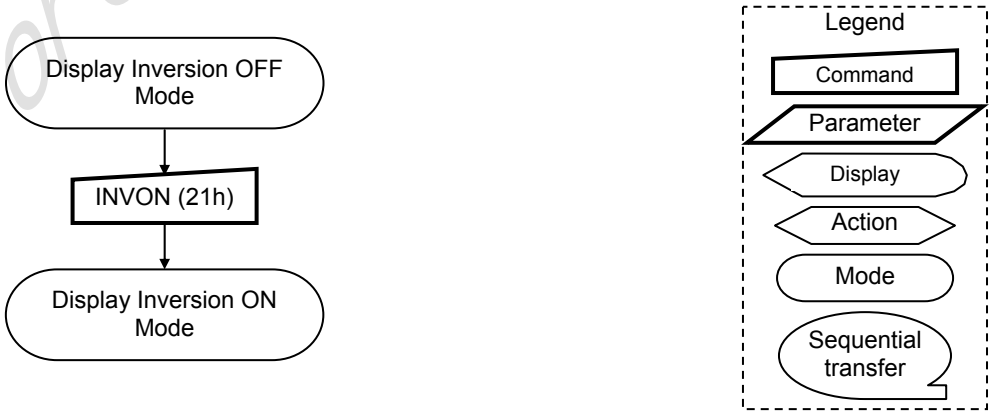
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

Flow Chart



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6.2.17. GAMSET (26h): Gamma Set

26H	GAMSET (Gamma Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GAMSET	0	↑	1	-	0	0	1	0	0	1	1	0	(26h)
1st Parameter	1	↑	1	-	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

-This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table.

GC [7:0]	Parameter	Curve Selected	
		GS=1	GS=0
01h	GC0	Gamma Curve 1 (G2.2)	Gamma Curve 1 (G1.0)
02h	GC1	Gamma Curve 2 (G1.8)	Gamma Curve 2 (G2.5)
04h	GC2	Gamma Curve 3 (G2.5)	Gamma Curve 3 (G2.2)
08h	GC3	Gamma Curve 4 (G1.0)	Gamma Curve 4 (G1.8)

Note: All other values are undefined.

Restriction

-Values of GC [7:0] not shown in table above are invalid and will not change the current selected Gamma curve until valid is received.

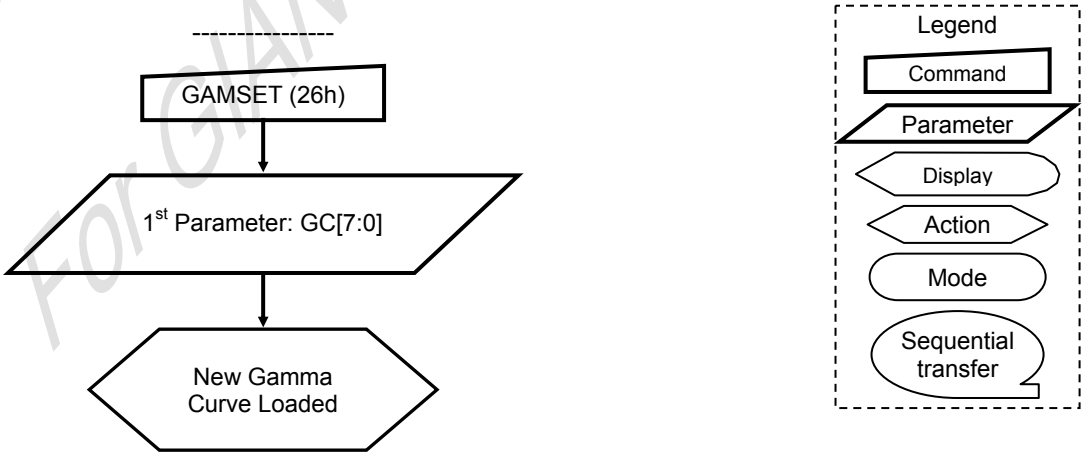
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

Flow Chart



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6.2.18. DISPOFF (28h): Display Off

28H	DISPOFF (Display Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

-This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disables and blank page inserted.

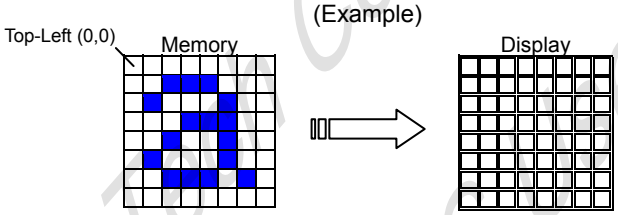
-This command makes no change of contents of frame memory.

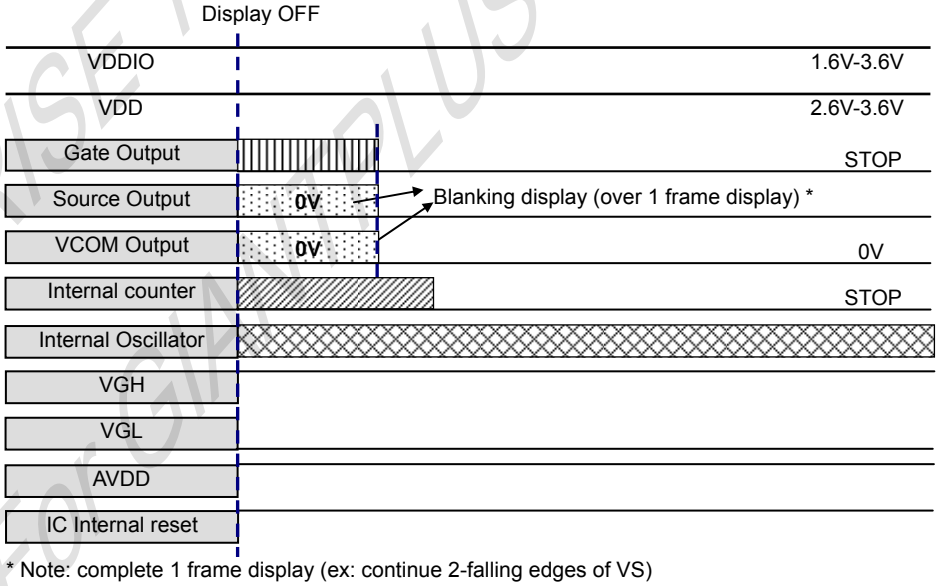
-This command does not change any other status.

-There will be no abnormal visible effect on the display.

-Exit from this command by Display On (29h)

(Example)





* Note: complete 1 frame display (ex: continue 2-falling edges of VS)

Restriction

-This command has no effect when module is already in Display Off mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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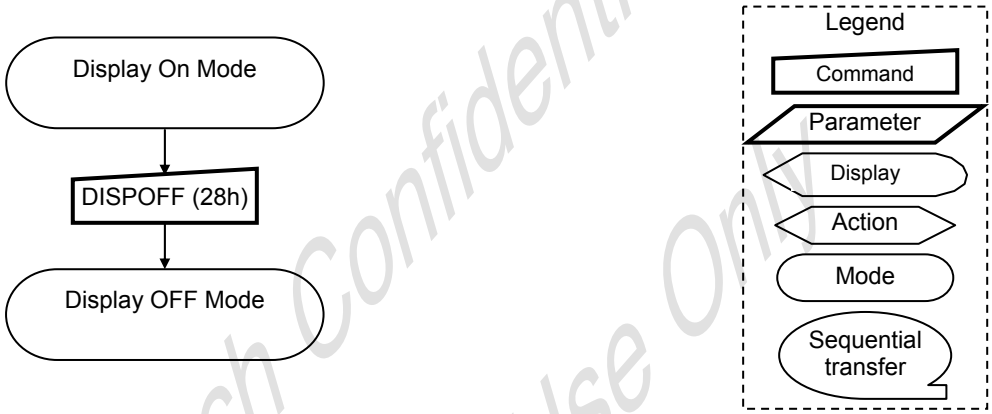
Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart



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6.2.19. DISPON (29h): Display On

29H	DISPON (Display On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)
1st Parameter	No Parameter												-

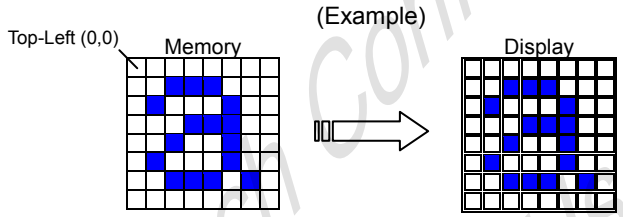
NOTE: "-" Don't care, can be set to VDDIO or DGND level

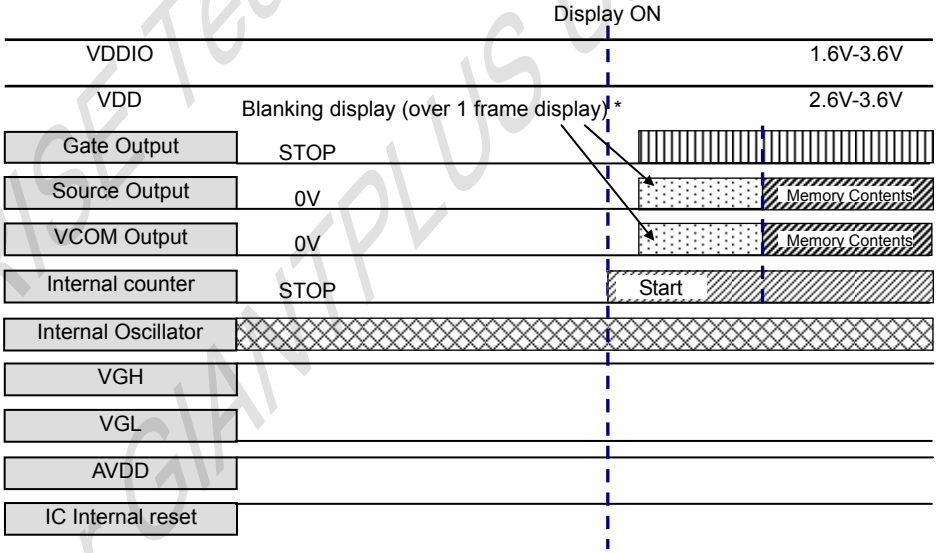
Description

-This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.

-This command makes no change of contents of frame memory.

-This command does not change any other status.





* Note: complete 1 frame display (ex: continue 2-falling edges of VS)

Restriction

-This command has no effect when module is already in Display On mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

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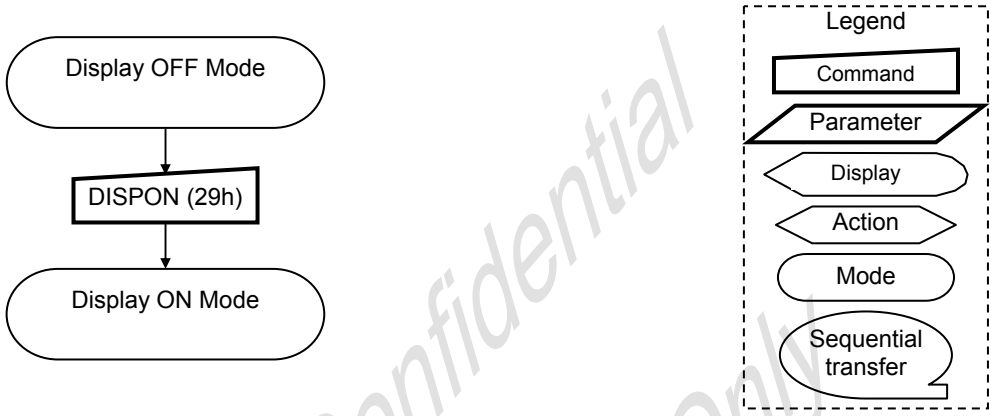
Flow Chart	

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6.2.20. CASET (2Ah): Column Address Set

2AH	CASET (Column Address Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
CASET	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)
1st Parameter	1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	
2nd Parameter	1	↑	1	-	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
3rd Parameter	1	↑	1	-	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	
4th Parameter	1	↑	1	-	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

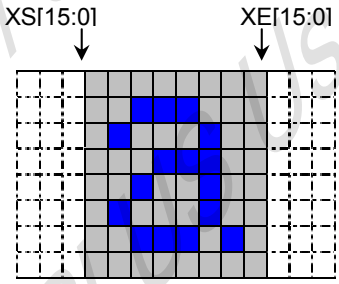
-This command is used to define area of frame memory where MCU can access.

-This command makes no change on the other driver status.

-The value of XS [15:0] and XE [15:0] are referred when RAMWR command comes.

-Each value represents one column line in the Frame Memory.

(Example)



Restriction

XS [15:0] always must be equal to or less than XE [15:0]

When XS [15:0] or XE [15:0] is greater than maximum address like below, data of out of range will be ignored.

1. 128X160 memory base (GM = '00')
   (Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 127 (007Fh)): MV="0"
   (Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 159 (009Fh)): MV="1"
2. 120x160 memory base (GM = '01')
   (Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 119 (0077h)): MV="0"
   (Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 159 (009Fh)): MV="1"
3. 128x128 memory base (GM = '10')
   (Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 127 (007Fh)): MV="0"
   (Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 127 (007Fh)): MV="1"
4. 132x162 memory base (GM = '11')
   (Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 131 (0083h)): MV="0"
   (Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 161 (00A1h)): MV="1"

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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Default

1. 128x160 memory base (GM = '00')

Status	Default Value		
	XS [15:0]	XE [15:0] (MV='**0**')	XE [15:0] (MV='**1**')
Power On Sequence	0000h	007Fh (127)	
S/W Reset	0000h	007Fh (127)	009Fh (159)
H/W Reset	0000h	007Fh (127)	

2. 120x160 memory base (GM = '01')

Status	Default Value		
	XS [15:0]	XE [15:0] (MV='**0**')	XE [15:0] (MV='**1**')
Power On Sequence	0000h	0077h (119)	
S/W Reset	0000h	0077h (119)	009Fh (159)
H/W Reset	0000h	0077h (119)	

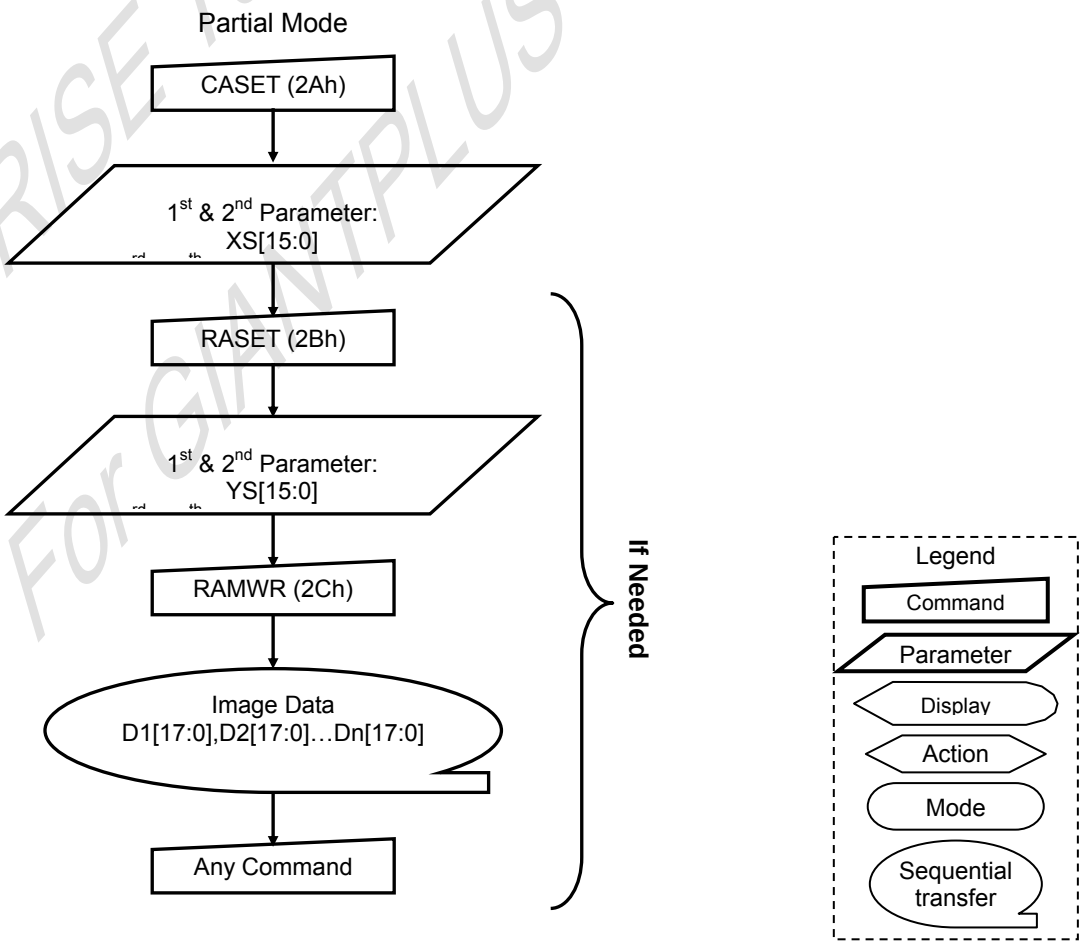
3. 128x128 memory base (GM = '10')

Status	Default Value		
	XS [15:0]	XE [15:0] (MV='**0**')	XE [15:0] (MV='**1**')
Power On Sequence	0000h	007Fh (127)	
S/W Reset	0000h	007Fh (127)	007Fh (127)
H/W Reset	0000h	007Fh (127)	

4. 132x162 memory base (GM = '11')

Status	Default Value		
	XS [15:0]	XE [15:0] (MV='**0**')	XE [15:0] (MV='**1**')
Power On Sequence	0000h	0083h (131)	
S/W Reset	0000h	0083h (131)	00A1h (161)
H/W Reset	0000h	0083h (131)	

Flow Chart



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6.2.21. RASET (2Bh): Row Address Set

2BH	RASET (Row Address Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RASET (2Bh)	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)
1st Parameter	1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	
2nd Parameter	1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
3rd Parameter	1	↑	1	-	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	
4th Parameter	1	↑	1	-	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

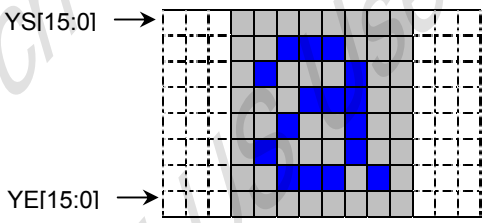
This command is used to define area of frame memory where MCU can access.

This command makes no change on the other driver status.

The value of YS [15:0] and YE [15:0] are referred when RAMWR command comes.

Each value represents one column line in the Frame Memory.

(Example)



Restriction

YS [15:0] always must be equal to or less than YE [15:0]

When YS [15:0] or YE [15:0] are greater than maximum row address like below, data of out of range will be ignored.

1. 128X160 memory base (GM = '00')
   (Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 159 (009Fh)): MV="0"
   (Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 127 (007Fh)): MV="1"
2. 120x160 memory base (GM = '01')
   (Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 159 (009Fh)): MV="0"
   (Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 119 (0077h)): MV="1"
3. 128x128 memory base (GM = '10')
   (Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 127 (007Fh)): MV="0"
   (Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 127 (007Fh)): MV="1"
4. 132x162 memory base (GM = '11')
   (Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 161 (00A1h)): MV="0"
   (Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 131 (0083h)): MV="1"

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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Default

1. 128x160 memory base (GM = '00')

Status	Default Value		
	YS [15:0]	YE [15:0] (MV='**0**')	YE [15:0] (MV='**1**')
Power On Sequence	0000h	009Fh (159)	
S/W Reset	0000h	009Fh (159)	007Fh (127)
H/W Reset	0000h	009Fh (159)	

2. 120x160 memory base (GM = '01')

Status	Default Value		
	YS [15:0]	YE [15:0] (MV='**0**')	YE [15:0] (MV='**1**')
Power On Sequence	0000h	009Fh (159)	
S/W Reset	0000h	007Fh (159)	0077h (119)
H/W Reset	0000h	009Fh (159)	

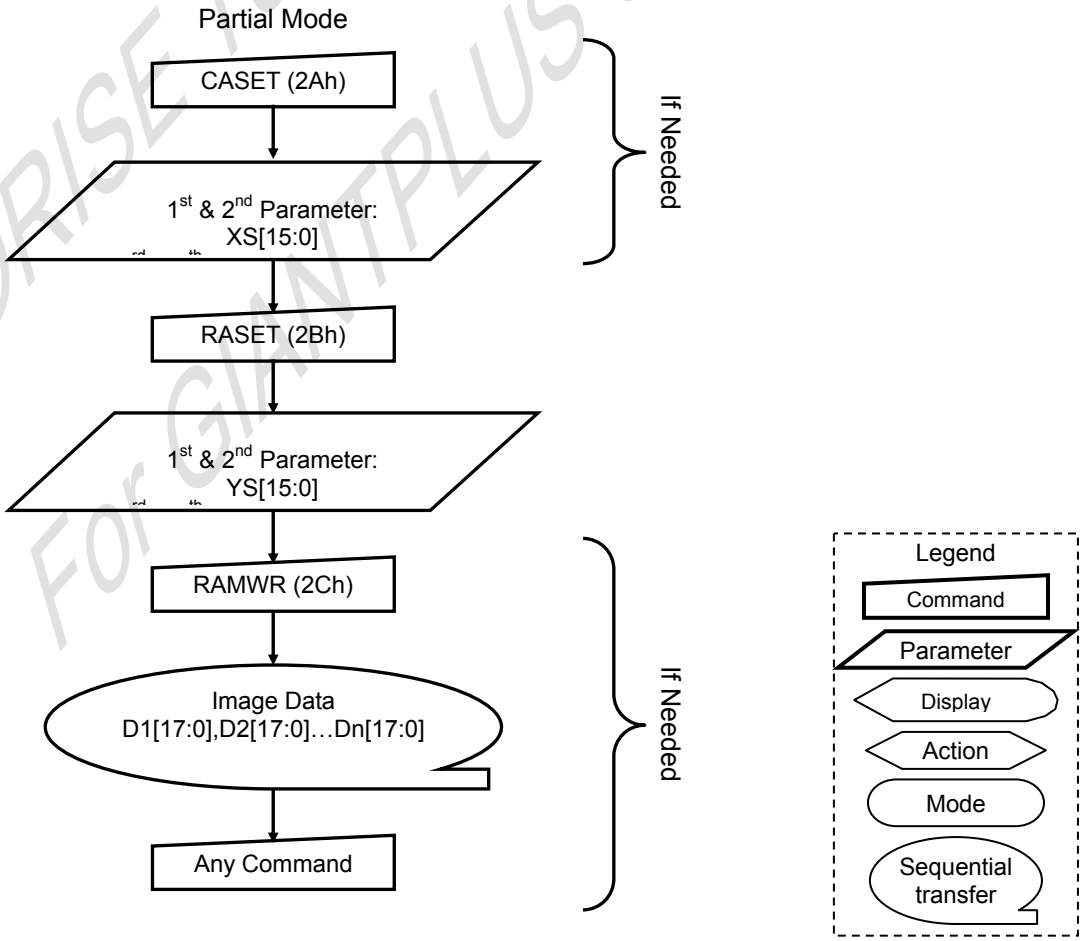
3. 128x128 memory base (GM = '10')

Status	Default Value		
	YS [15:0]	YE [15:0] (MV='**0**')	YE [15:0] (MV='**1**')
Power On Sequence	0000h	007Fh (127)	
S/W Reset	0000h	007Fh (127)	007Fh (127)
H/W Reset	0000h	007Fh (127)	

4. 132x162 memory base (GM = '11')

Status	Default Value		
	YS [15:0]	YE [15:0] (MV='**0**')	YE [15:0] (MV='**1**')
Power On Sequence	0000h	00A1h (161)	
S/W Reset	0000h	00A1h (161)	0083h (131)
H/W Reset	0000h	00A1h (161)	

Flow Chart



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6.2.22. RAMWR (2Ch): Memory Write

2CH	RAMWR (Memory Write)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)
1st Parameter	1	↑	1	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-
|	1	↑	1	|	|	|	|	|	|	|	|	|	|
Nth Parameter	1	↑	1	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description	-This command is used to transfer data from MCU to frame memory. -This command makes no change to the other driver status. -When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions. -The Start Column/Start Row positions are different in accordance with MADCTR setting. -Sending any other command can stop Frame Write.
Restriction	In all color modes, there is no restriction on length of parameters. -1. 128X160 memory base (GM = '00') 128x160x18-bit memory can be written by this command Memory range: (0000h,0000h) -> (007Fh, 09Fh) -2. 120x160 memory base (GM = '01') 120x160x18-bit memory can be written on this command. Memory range: (0000h,0000h) -> (0077h,09Fh) -3. 128x128 memory base (GM = '10') 128x128x18-bit memory can be written on this command. Memory range: (0000h,0000h) -> (007Fh,007Fh) -4. 132x162 memory base (GM = '11') 132x162x18-bit memory can be written on this command. Memory range: (0000h,0000h) -> (0083h,00A1h)
Register Availability	Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes
Default	Status: Power On Sequence — Default Value: Contents of memory is set randomly Status: S/W Reset — Default Value: Contents of memory is not cleared Status: H/W Reset — Default Value: Contents of memory is not cleared

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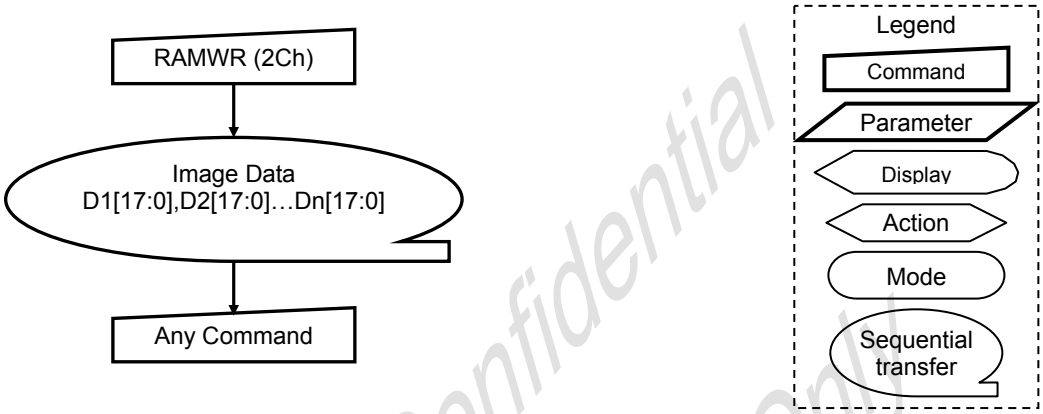
Flow Chart	

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6.2.23. RGBSET (2Dh): Colour Setting for 4K, 65K and 262K

2DH	RGBSET (Colour Set for 4K, 65K and 262K)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RGBSET	0	↑	1	-	0	0	1	0	1	1	0	1	(2Dh)
1st Parameter	1	↑	1	-	-	-	R005	R004	R003	R002	R001	R000	-
|	1	↑	1	-	-	-	Rnn5	Rnn4	Rnn3	Rnn2	Rnn1	Rnn0	-
|	1	↑	1	-	-	-	R315	R314	R313	R312	R311	R310	-
|	1	↑	1	-	-	-	G005	G004	G003	G002	G001	G000	-
|	1	↑	1	-	-	-	Gnn5	Gnn4	Gnn3	Gnn2	Gnn1	Gnn0	-
|	1	↑	1	-	-	-	G635	G634	G633	G632	G631	G630	-
|	1	↑	1	-	-	-	B005	B004	B003	B002	B001	B000	-
|	1	↑	1	-	-	-	Bnn5	Bnn4	Bnn3	Bnn2	Bnn1	Bnn0	-
128nd Parameter	1	↑	1	-	-	-	B315	B314	B313	B312	B311	B310	-

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

This command is used to define the LUT for 12bits-to-16bits / 16-bits-to-18bits color depth conversations.
128-Bytes must be written to the LUT regardless of the color mode..
In this condition, 4K-color (4-4-4) and 65K-color(5-6-5) data input are transferred 6(R)-6(G)-6(B) through RGB LUT table.
This command has no effect on other commands/parameters and Contents of frame memory.
Visible change takes effect next time the Frame Memory is written to.

Restriction

Do not send any command before the last data is sent or LUT is not defined correctly.

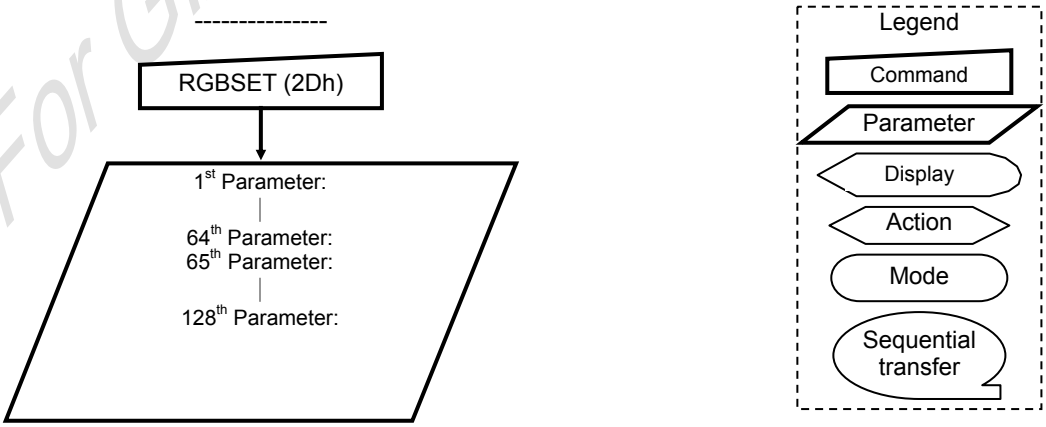
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Random
S/W Reset	Contents of the look-up table protected
H/W Reset	Random

Flow Chart



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6.2.24. RAMHD (2Eh): Memory Read

2EH	RAMHD (Memory Read)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RAMHD	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-
|	1	1	↑	|	|	|	|	|	|	|	|	|	|
(N+1)th Parameter	1	1	↑	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

-This command is used to transfer data from frame memory to MCU.

-This command makes no change to the other driver status.

-When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions.

-The Start Column/Start Row positions are different in accordance with MADCTR setting.

-Frame Read can be canceled by sending any other command.

Restriction

-In all color modes, the Frame Read is always 18-bits and there is no restriction on length of parameters.

-Memory read is only possible via the SPI and parallel interface.

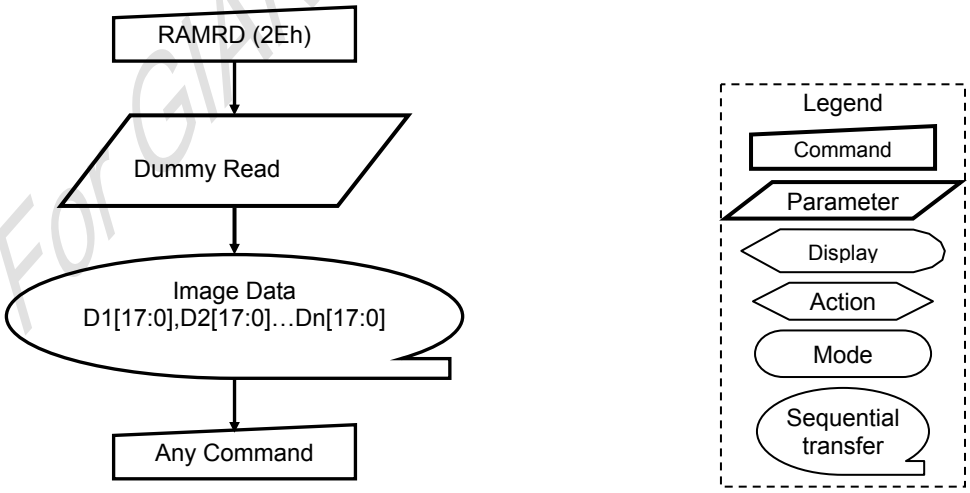
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart



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6.2.25. PTLAR (30h): Partial Area

30H	PTLAR (Partial Area)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PTLAR	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)
1st Parameter	1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	
2nd Parameter	1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	
3rd Parameter	1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	
4th Parameter	1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	

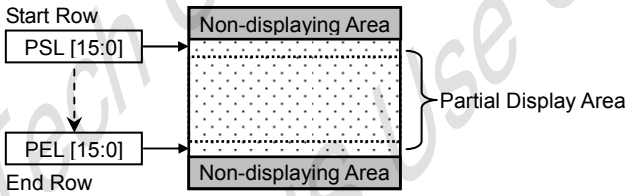
NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

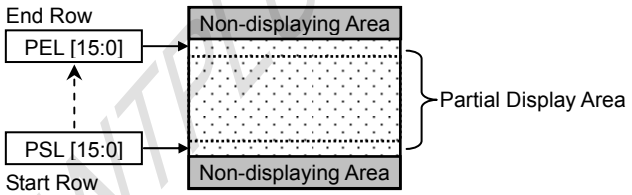
-This command defines the partial mode's display area.

-There are 4 parameters associated with this command, the first defines the Start Row (PSL) and the second the End Row (PEL), as illustrated in the figures below. PSL and PEL refer to the Frame Memory row address counter.

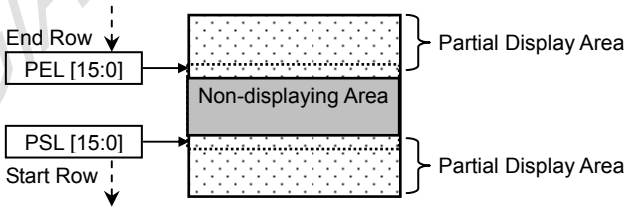
-If End Row > Start Row, when MADCTL ML='0'



-If End Row > Start Row, when MADCTL ML='1'



-If End Row < Start Row, when MADCTL ML='0'



-If End Row = Start Row then the Partial Area will be one row deep.

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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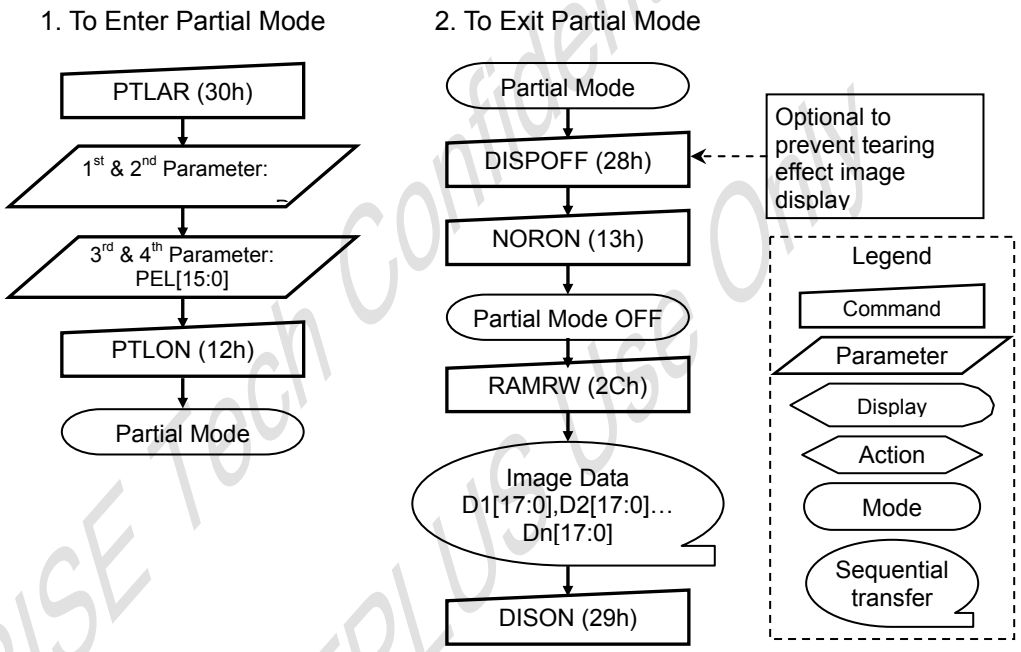
Default

Status	Default Value			
	PSL [15:0]	PEL [15:0]		
		GM="00" , "01"	GM="10"	GM="11"
Power On Sequence	0000h	009Fh	007Fh	00A1h
S/W Reset	0000h	009Fh	007Fh	00A1h
H/W Reset	0000h	009Fh	007Fh	00A1h

Flow Chart



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6.2.26. SCRLAR (33h): Scroll Area

33H	SCRLAR (Scroll Area)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SCRLAR	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)
1st Parameter	1	↑	1	-	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8	
2nd Parameter	1	↑	1	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	
3rd Parameter	1	↑	1	-	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8	
4th Parameter	1	↑	1	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	
5th Parameter	1	↑	1	-	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8	
6th Parameter	1	↑	1	-	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	

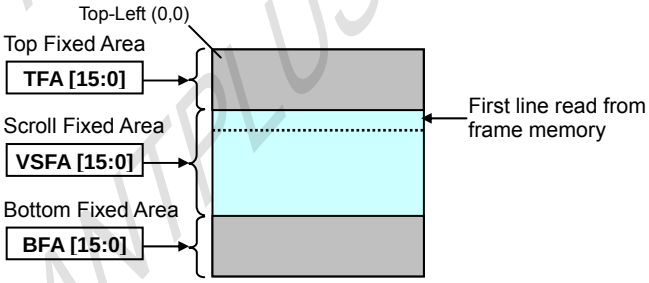
NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

This command defines the Vertical Scrolling Area of the display.

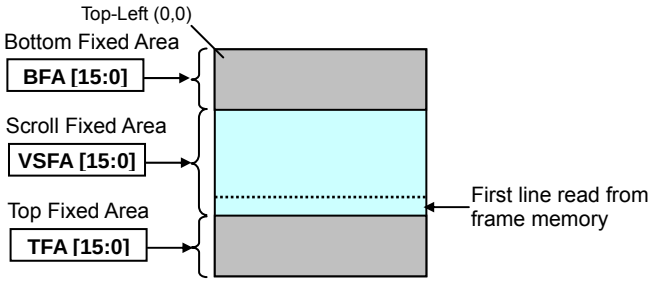
When MADCTR ML=0

- The 1st & 2nd parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).
- The 3rd & 4th parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address)
- The first line appears immediately after the bottom most line of the Top Fixed Area.
- The 5th & 6th parameter BFA [15:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).
- TFA, VSA and BFA refer to the Frame Memory row address.



When MADCTR ML=1

- The 1st & 2nd parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).
- The 3rd & 4th parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address)
- The first line appears immediately after the top most line of the Top Fixed Area.
- The 5th & 6th parameter BFA [15:0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).



Restriction

-The condition is 0 ≤ (TFA+VSA+BFA) ≤ 162, otherwise Scrolling mode is undefined.

-In Vertical Scroll Mode, MADCTR parameter MV should be set to '0'-this only affects the Frame Memory Write.

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Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

-

Status	Default Value				
	TFA [15:0]	VSA [15:0]			BFA [15:0]
		GM="00","01"	GM="10"	GM="11"	
Power On Sequence	0000h	00A0h	0080h	00A2h	0000h
S/W Reset	0000h	00A0h	0080h	00A2h	0000h
H/W Reset	0000h	00A0h	0080h	00A2h	0000h

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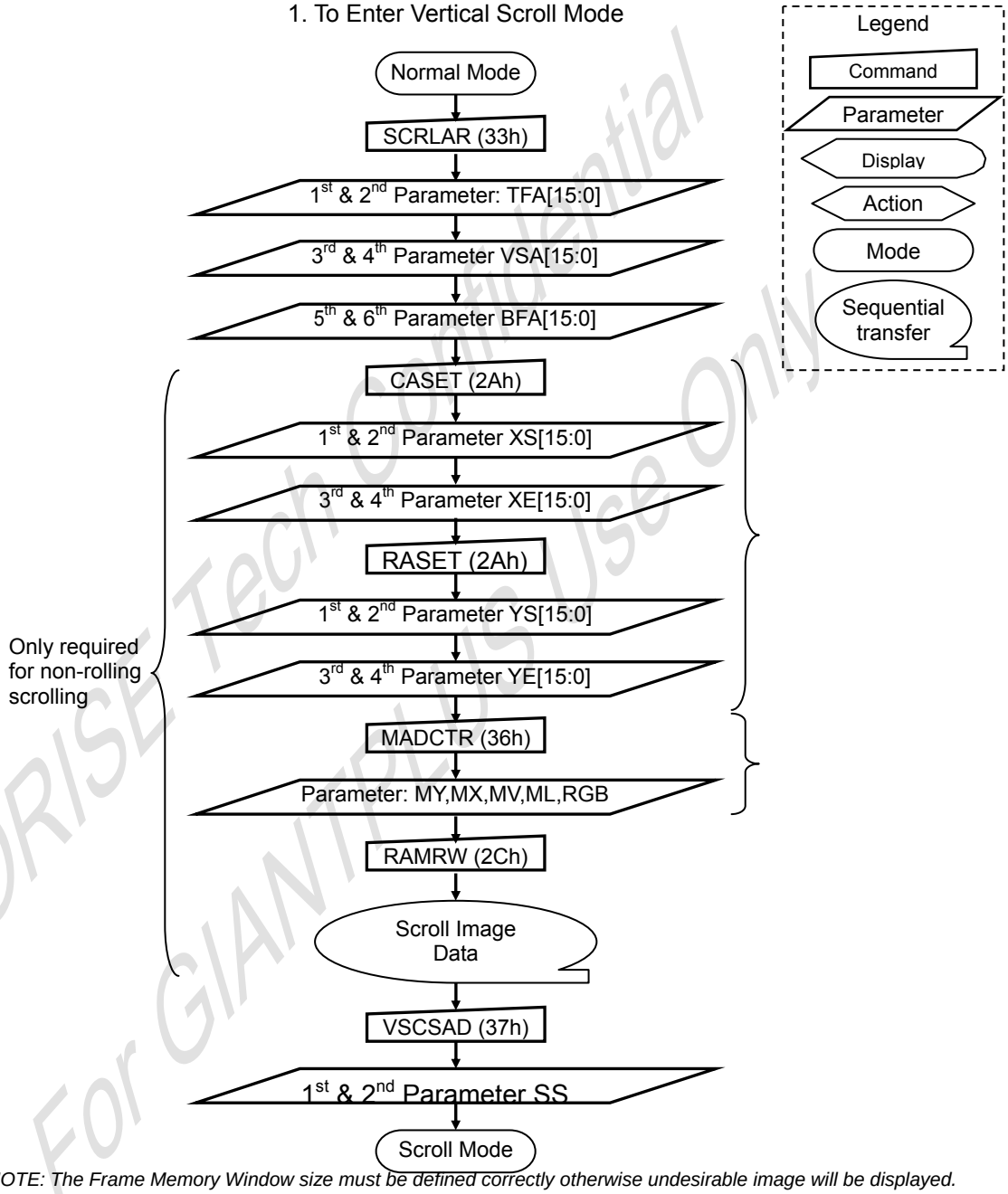
Flow Chart

1. To Enter Vertical Scroll Mode



NOTE: The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.

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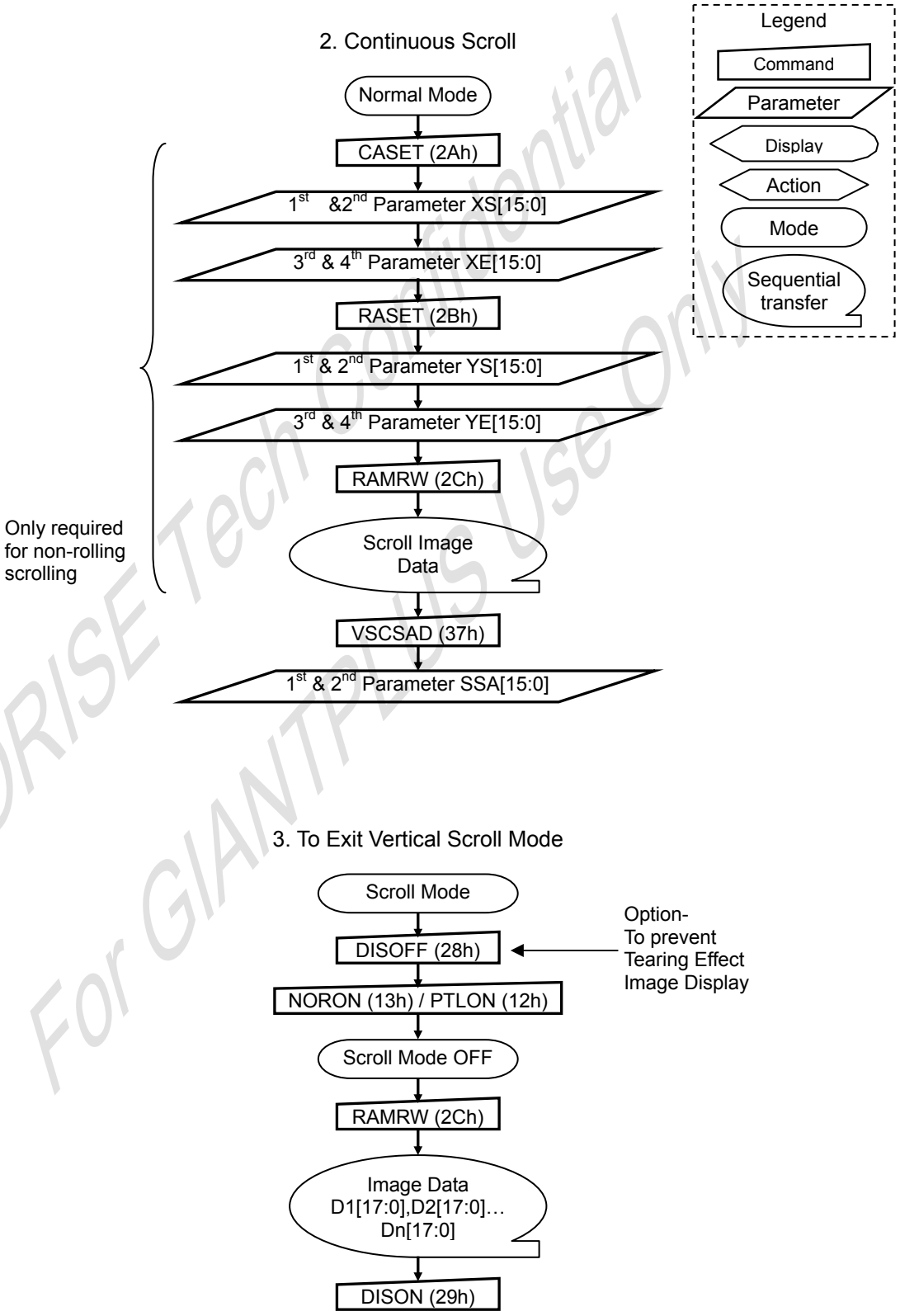
Flow Chart



NOTE: Scroll Mode can be exit by both the Normal Display Mode On (13h) and Partial Mode On (12h) commands.

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6.2.27. TEOFF (34h): Tearing Effect Line OFF

34H	TEOFF (Tearing Effect Line OFF)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description	-This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.
Restriction	-This command has no effect when Tearing Effect output is already OFF.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
S/W Reset	OFF
H/W Reset	OFF

Flow Chart

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6.2.28. TEON (35h): Tearing Effect Line ON

35H	TEON (Tearing Effect Line ON)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEON	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)
1st Parameter	1	↑	1	-	0	0	0	0	0	0	0	TELOM	

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

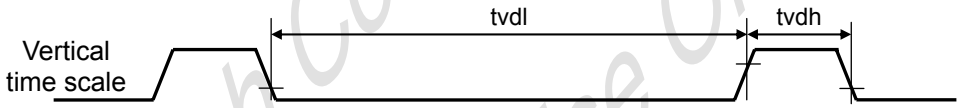
-This command is used to turn ON the Tearing Effect output signal from the TE signal line.

-This output is not affected by changing MADCTR bit ML.

-The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. ("-"=Don't Care).

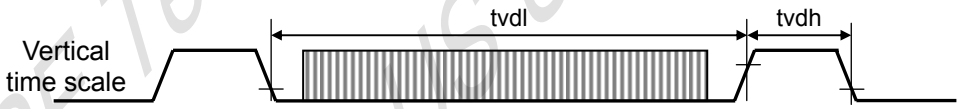
—When M='0':

The Tearing Effect Output line consists of V-Blanking information only.



—When M='1':

The Tearing Effect Output line consists of both V-Blanking and H-Blinking information.



Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

-This command has no effect when Tearing Effect output is already OFF.

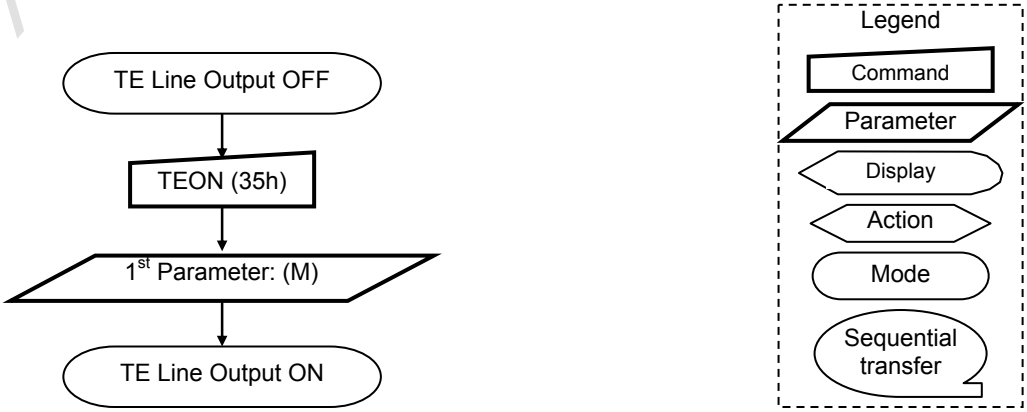
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Tearing effect off & TELOM=0
S/W Reset	Tearing effect off & TELOM=0
H/W Reset	Tearing effect off & TELOM=0

Flow Chart



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6.2.29. MADCTR (36h): Memory Data Access Control

36H	MADCTR (Memory Data Access Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
MADCTR	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)
1st Parameter	1	↑	1	-	MY	MX	MV	ML	RGB	0	0	0	

NOTE: "-" Don't care, can be set to VDDIO or DGND level

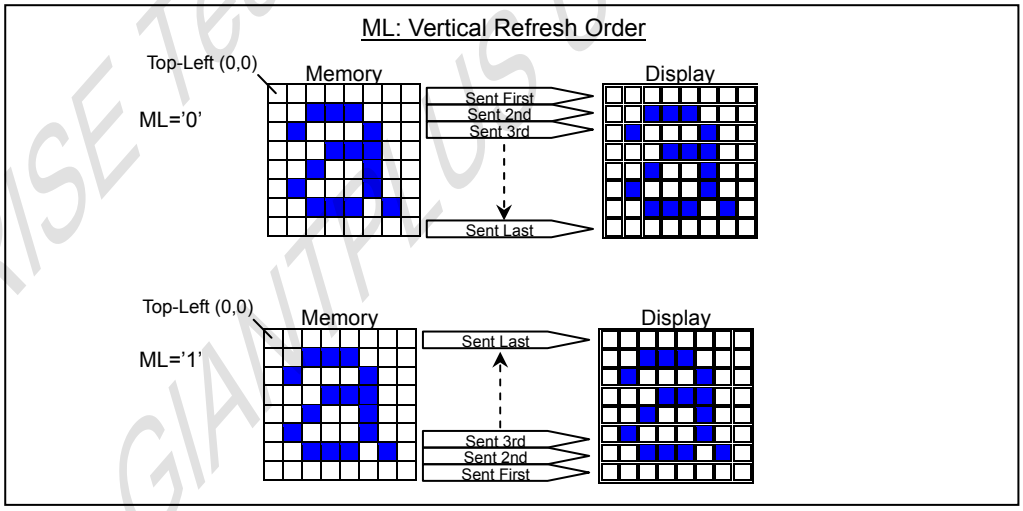
Description

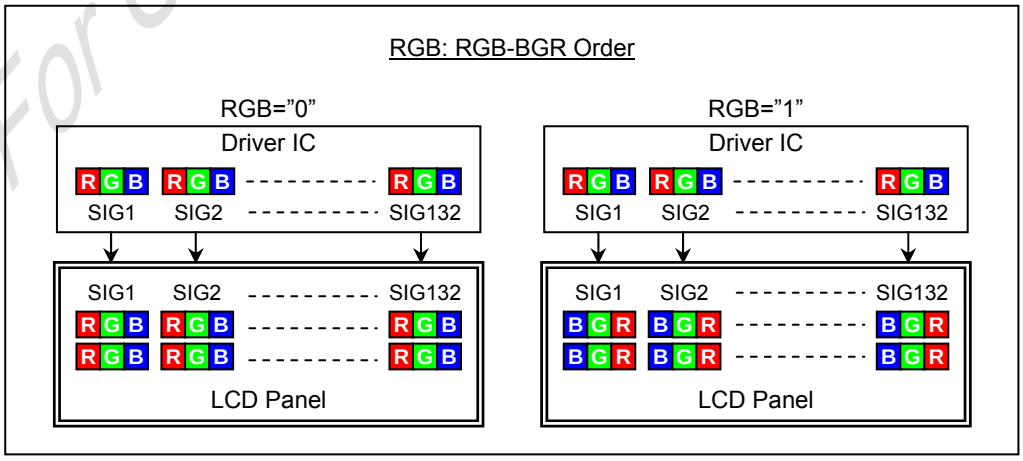
-This command defines read/ write scanning direction of frame memory.

-This command makes no change on the other driver status.

-Bit Assignment

Bit	NAME	DESCRIPTION
MY	Row Address Order	These 3bits controls MCU to memory write/read direction.
MX	Column Address Order	
MV	Row/Column Exchange	
ML	Vertical Refresh Order	LCD vertical refresh direction control '0' = LCD vertical refresh Top to Bottom '1' = LCD vertical refresh Bottom to Top
RGB	RGB-BGR ORDER	Color selector switch control '0' =RGB color filter panel, '1' =BGR color filter panel)





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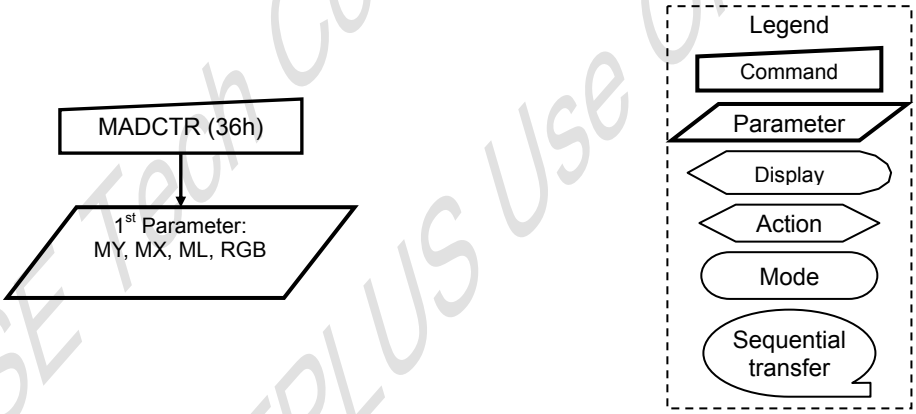
Restriction	D1 and D0 of the 1st parameter are set to “00” internally.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	MY=0,MX=0,MV=0,ML=0,RGB=0
S/W Reset	No Change
H/W Reset	MY=0,MX=0,MV=0,ML=0,RGB=0

Flow Chart



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6.2.30. VSCSAD (37h): Vertical Scroll Start Address of RAM

37H	VSCSAD (Vertical Scroll Start Address of RAM)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VSCSAD	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)
1st Parameter	1	↑	1	-	SSA15	SSA14	SSA13	SSA12	SSA11	SSA10	SSA9	SSA8	
2nd Parameter	1	↑	1	-	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

-This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode.

-The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:

-This command Start the scrolling.

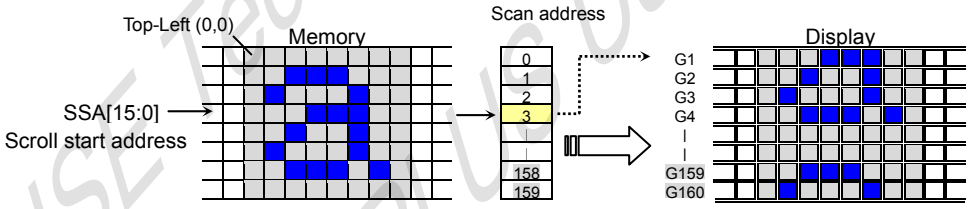
-Exit from V-scrolling mode by commands Partial mode On (12h) or Normal mode On (13h).

When MADCTR ML= '0'

Example:

—When Top Fixed Area=Bottom Fixed Area=00, Vertical Scrolling Area=160 and Vertical Scrolling Pointer SSA= '3'.

(Example)

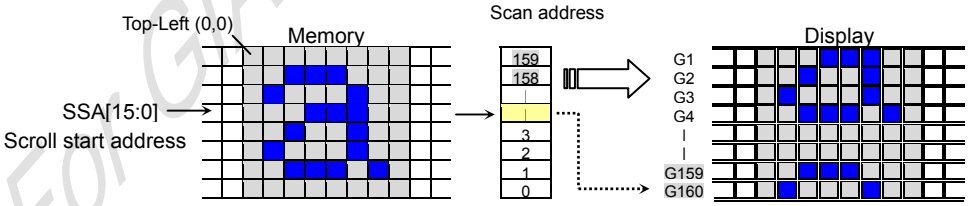


When MADCTR ML = '1'

Example:

—When Top Fixed Area= Bottom Fixed Area=00, Vertical Scrolling Area=160 and SSA= '3'

(Example)



NOTE: -When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.
-SSA refers to the Frame Memory scan address.

Restriction

-Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h)-otherwise undesirable image will be displayed on the Panel.

SSA[15:0] is based on 1-line unit.

-SSA[15:0] = 0000h, 0001h, 0002h, 0003h, … , 00A1h

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<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>0000h</td></tr>
<tr><td>S/W Reset</td><td>0000h</td></tr>
<tr><td>H/W Reset</td><td>0000h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

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6.2.31. IDMOFF (38h): Idle Mode Off

38H	IDMOFF (Idle Mode Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

-This command is used to recover from Idle mode on.

-There will be no abnormal visible effect on the display mode change transition.

-In the idle off mode,

1. LCD can display 4096, 65k or 262k colors.
2. Normal frame frequency is applied.

Restriction

-This command has no effect when module is already in idle off mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

Flow Chart

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6.2.32. IDMON (39h): Idle Mode On

39H	IDMON (Idle Mode On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
IDMON	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)
1st Parameter	No Parameter												-

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

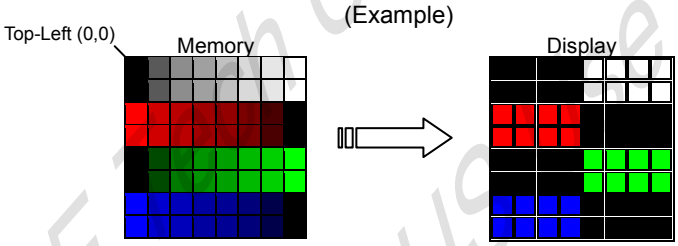
-This command is used to enter into Idle mode on.

-There will be no abnormal visible effect on the display mode change transition.

-In the idle on mode,

1. Color expression is reduced. The primary and the secondary colors using MSB of each R,G and B in the Frame Memory, 8 color depth data is displayed.
2. 8-Color mode frame frequency is applied.
3. Exit from IDMON by Idle Mode Off (38h) command

(Example)



Color	$R_5 R_4 R_3 R_2 R_1 R_0$	$G_5 G_4 G_3 G_2 G_1 G_0$	$B_5 B_4 B_3 B_4 B_1 B_0$
Black	0xxxxx	0xxxxx	0xxxxx
Blue	0xxxxx	0xxxxx	1xxxxx
Red	1xxxxx	0xxxxx	0xxxxx
Magenta	1xxxxx	0xxxxx	1xxxxx
Green	0xxxxx	1xxxxx	0xxxxx
Cyan	0xxxxx	1xxxxx	1xxxxx
Yellow	1xxxxx	1xxxxx	0xxxxx
White	1xxxxx	1xxxxx	1xxxxx

Restriction

This command has no effect when module is already in idle on mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

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Flow Chart	

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6.2.33. COLMOD (3Ah): Interface Pixel Format

3AH	COLMOD (3Ah): Interface Pixel Format												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
COLMOD	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)
1st Parameter	1	↑	1	-	VIPF3	VIPF2	VIPF1	VIPF0	D3	IFPF2	IFPF1	IFPF0	

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

This command is used to define the format of RGB picture data, which is to be transferred via the MCU interface and RGB interface. The formats are shown in the table:

IFPF[2:0]		MCU Interface Color Format
011	3	12-bits/pixel
101	5	16-bits/pixel
110	6	18-bits/pixel
111	7	No used

Others are no define and invalid

VIPF[3:0]		RGB Interface Color Format
0101	5	16-bits/pixel (1-times data transfer)
0110	6	18-bits/pixel (1-times data transfer)
0111	7	No used
1110	14	18-bits/pixel (3-times data transfer)

Others are no define and invalid

Note1: In 12-bits/Pixel, 16-bits/Pixel or 18-bits/Pixel mode, the LUT is applied to transfer data into the Frame Memory.
Note2: When RGB I/F the 12-bit/pixel don't care
Note 3: When VIPF[3:0]="1110",6-bits data width of 3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Restriction

There is no visible effect until the Frame Memory is written to.

Register Availability

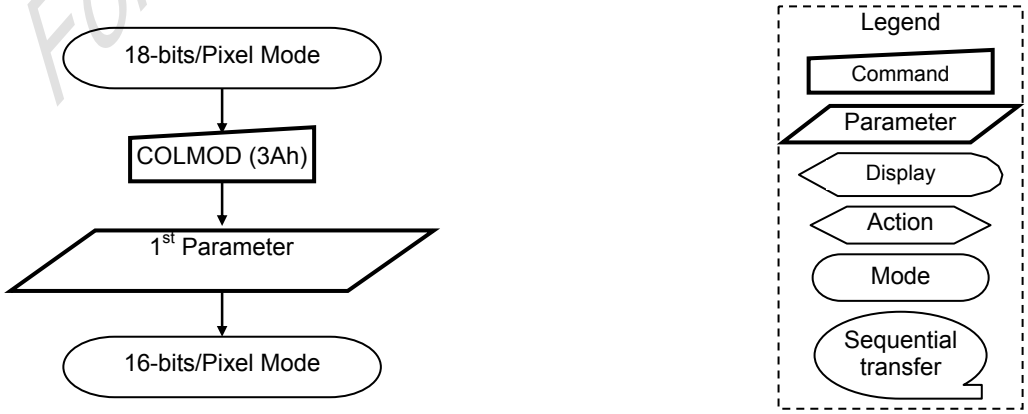
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	IFPF[2:0]	VIPF[3:0]
Power On Sequence	0110 (18-bits/pixel)	0110 (18-bits/pixel)
S/W Reset	No Change	No Change
H/W Reset	0110 (18-bits/pixel)	0110 (18-bits/pixel)

Flow Chart

Example:



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6.2.34. RDID1 (DAh): Read ID1 Value

DAH	RDID1 (Read ID1 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

-This read byte returns 8-bits LCD module's manufacturer ID

-The 1st parameter is dummy data

-The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID.

NOTE: See command RDDID (04h), 2nd parameter.

Restriction

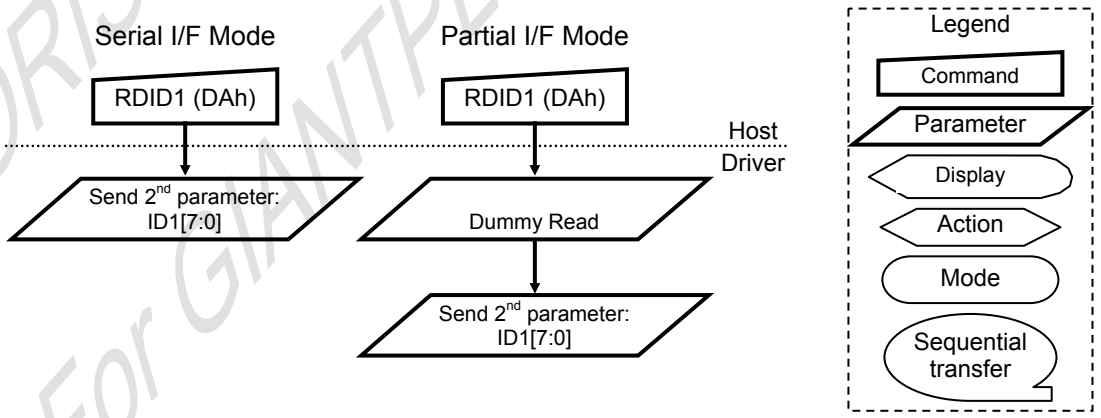
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	38h
S/W Reset	38h
H/W Reset	38h

Flow Chart



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6.2.35. RDID2 (DBh): Read ID2 Value

DBH	RDID2 (Read ID2 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

-This read byte returns 8-bits LCD module/driver version ID

-The 1st parameter is dummy data

-The 2nd parameter (ID26 to ID20): LCD module/driver version ID

-Parameter Range: ID=80h to FFh

ID26 to ID20	Version	Changes
80h		
81h		
82h		
83h		
-		

NOTE: See command RDDID (04h), 3rd parameter.

Restriction

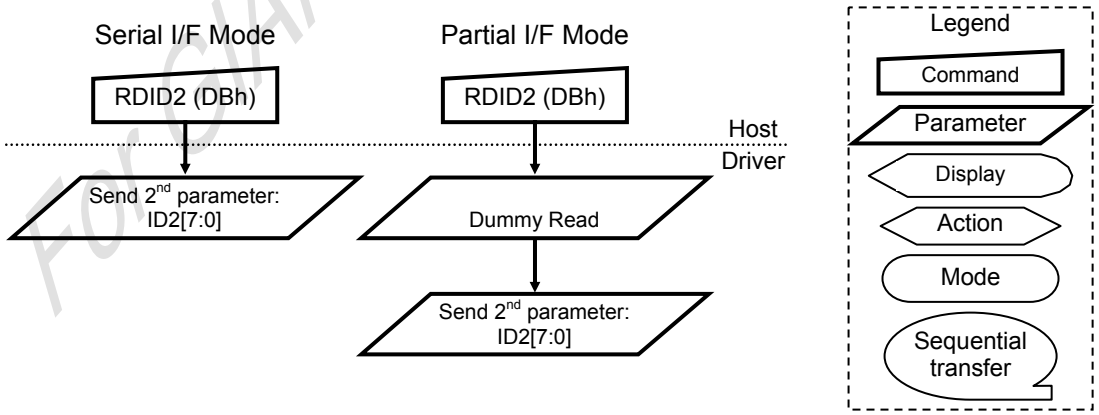
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	80h
S/W Reset	80h
H/W Reset	80h

Flow Chart



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6.2.36. RDID3 (DCh): Read ID3 Value

DCH	RDID3 (Read ID2 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID3	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

-This read byte returns 8-bits LCD module/driver ID.

-The 1st parameter is dummy data

-The 2nd parameter (ID37 to ID30): LCD module/driver ID.

NOTE: See command RDDID (04h), 4th parameter.

Restriction

-

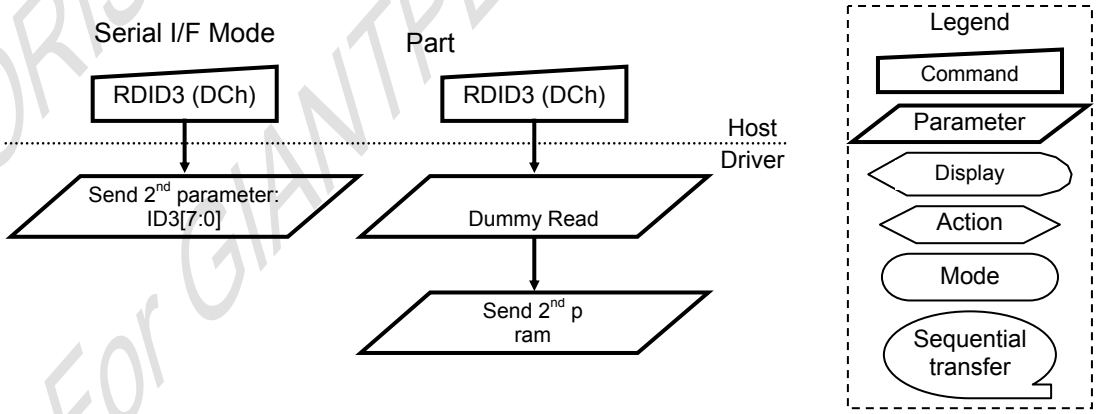
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	4Fh
S/W Reset	4Fh
H/W Reset	4Fh

Flow Chart



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6.3. Panel Command Description

6.3.1. RGBCTR (B0h): RGB signal control

B0H	RGBCTR (RGB signal control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RGBCTR	0	↑	1	-	1	0	1	1	0	0	0	0	(B0h)
1st Parameter	1	↑	1	-	0	0	0	ICM	DP	EP	HSP	VSP	

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

-Set the operation status on the RGB interface. The setting becomes effective as soon as the command is received.

-ICM: GRAM Write/Read frequency and data input select on the RGB interface

ICM	Write/ Read frequency and input data select		
	Write cycle	Read cycle	Data input
0	PCLK	PCLK	D[17:0]
1	SCL	Internal oscillator	SDA

Symbol	Name	Clock polarity set for RGB Interface
DP	PCLK polarity set	'1' = data fetched at the falling edge '0' = data fetched at the rising edge
EP	Enable polarity set	'1' = Low enable for RGB interface '0' = High enable for RGB interface
HSP	Hsync polarity set	'1' = High level sync clock '0' = Low level sync clock
VSP	Vsync polarity set	'1' = High level sync clock '0' = Low level sync clock

Restriction

-If this register not using the register need be reserved.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	ICM	DP/EP/HSP/VSP
Power On Sequence	0d	0d/0d/0d/0d
S/W Reset	0d	0d/0d/0d/0d
H/W Reset	0d	0d/0d/0d/0d

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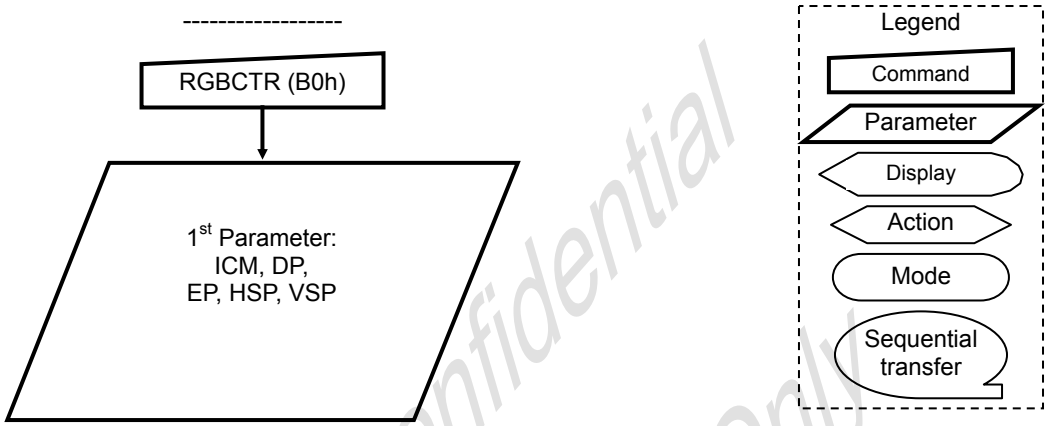
Flow Chart	

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6.3.2. FRMCTR1 (B1h): Frame Rate Control (In normal mode/ Full colors)

B1H	FRMCTR1 (Frame Rate Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
FRMCTR1	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)
1st Parameter	1	↑	1	-	0	0	0	0	FP0[3]	FP0[2]	FP0[1]	FP0[0]	-
2nd Parameter	1	↑	1	-	0	0	0	0	BP0[3]	BP0[2]	BP0[1]	BP0[0]	-
3rd Parameter	1	↑	1	-	0	0	0	0	RTN0 [3]	RTN0 [2]	RTN0 [1]	RTN0 [0]	-

NOTE: "-" Don't care

Description

-Set the frame frequency of the full colors normal mode in MPU interface.

--The default vaule of BP0, FP0, and RTN0 can fit the frame frequency to be 65Hz ±5%.

FP0[3:0]	Amount of Front Porch
0	0
1	1
2	2
3	3
4	4
…	…
D	13
E	14
F	15

BP0[3:0]	Amount of Back Porch
0	0
1	1
2	2
3	3
4	4
…	…
D	13
E	14
F	15

RTN0[3:0]	No. of clock in one line
0	16
1	17
2	18
3	19
4	20
…	…
D	29
E	30
F	31

Restriction

-If this register not using the register need be reserved.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	FP0	BP0	RTN0
Power On Sequence	2d	14d	0d
S/W Reset	2d	14d	0d
H/W Reset	2d	14d	0d

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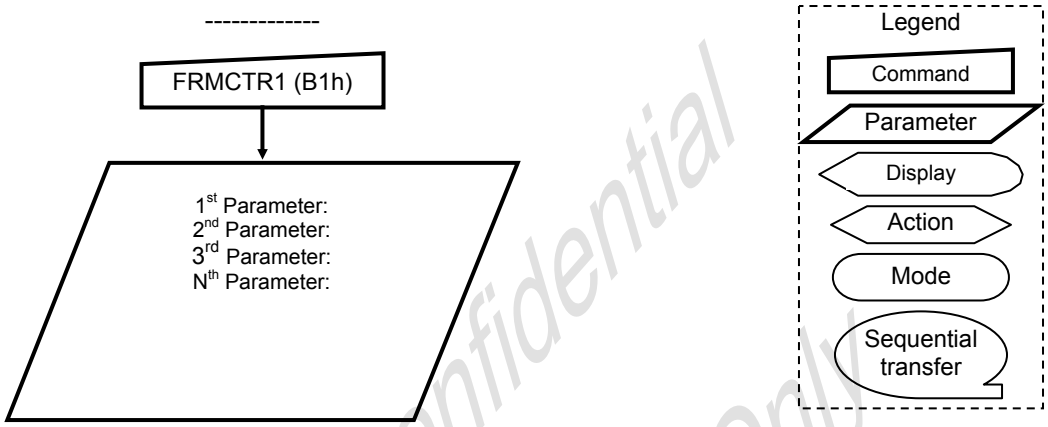
Flow Chart	

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6.3.3. FRMCTR2 (B2h): Frame Rate Control (In Idle mode/ 8-colors)

B2H	FRMCTR2 (Frame Rate Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
FRMCTR2	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)
1st Parameter	1	↑	1	-	0	0	0	0	FP1[3]	FP1[2]	FP1[1]	FP1[0]	-
2nd Parameter	1	↑	1	-	0	0	0	0	BP1[3]	BP1[2]	BP1[1]	BP1[0]	-
3rd Paramete	1	↑	1	-	0	0	0	0	RTN1 [3]	RTN1 [2]	RTN1 [1]	RTN1 [0]	-

NOTE: "-" Don't care

Description

-Set the frame frequency of the Idle mode in MPU interface.

-The default vaule of BP1, FP1, and RTN1 can fit the frame frequency to be 70Hz ±5%.

FP1[3:0]	Amount of Front Porch
0	0
1	1
2	2
3	3
4	4
…	…
D	13
E	14
F	15

BP1[3:0]	Amount of Back Porch
0	0
1	1
2	2
3	3
4	4
…	…
D	13
E	14
F	15

RTN1[3:0]	No. of clock in one line
0	16
1	17
2	18
3	19
4	20
…	…
D	29
E	30
F	31

Restriction

-If this register not using the register need be reserved.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	FP1	BP1	RTN1
Power On Sequence	2d	14d	0d
S/W Reset	2d	14d	0d
H/W Reset	2d	14d	0d

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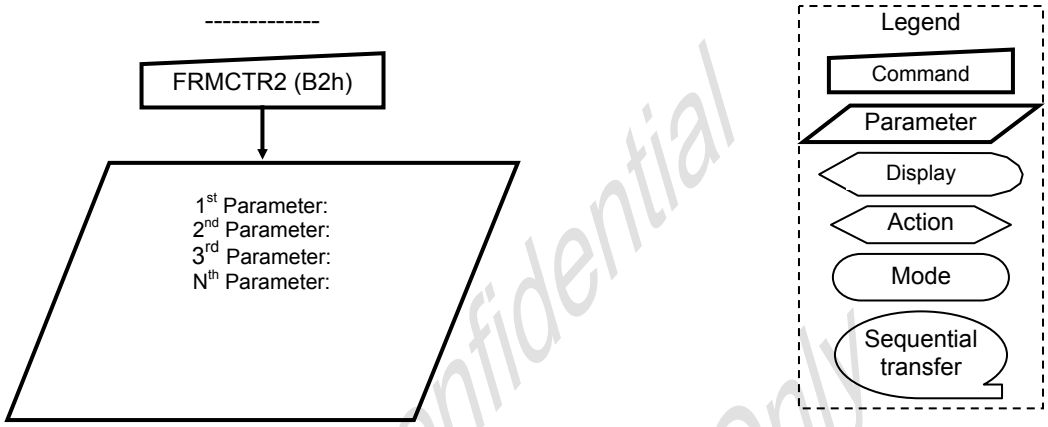
Flow Chart	

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6.3.4. FRMCTR3 (B3h): Frame Rate Control (In Partial mode/ full colors)

B3H	FRMCTR3 (Frame Rate Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
FRMCTR3	0	↑	1	-	1	0	1	1	0	0	1	1	(B3h)
1st Parameter	1	↑	1	-	0	0	0	0	FP2[3]	FP2[2]	FP2[1]	FP2[0]	-
2nd Parameter	1	↑	1	-	0	0	0	0	BP2[3]	BP2[2]	BP2[1]	BP2[0]	-
3rd Parameter	1	↑	1	-	0	0	0	0	RTN2 [3]	RTN2 [2]	RTN2 [1]	RTN2 [0]	-

NOTE: "-" Don't care

Description

-Set the frame frequency of the Partial mode/ full colors in MPU interface.

-The default vaule of BP2, FP2, and RTN2 can fit the frame frequency to be 70Hz ±5% with frame inversion and 65Hz ±5% with line inversion in this mode

FP2[3:0]	Amount of Front Porch
0	0
1	1
2	2
3	3
4	4
…	…
D	13
E	14
F	15

BP2[3:0]	Amount of Back Porch
0	0
1	1
2	2
3	3
4	4
…	…
D	13
E	14
F	15

RTN2[3:0]	No. of clock in one line
0	16
1	17
2	18
3	19
4	20
…	…
D	29
E	30
F	31

Restriction

-If this register not using the register need be reserved.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	FP2	BP2	RTN2
Power On Sequence	2d	14d	0d
S/W Reset	2d	14d	0d
H/W Reset	2d	14d	0d

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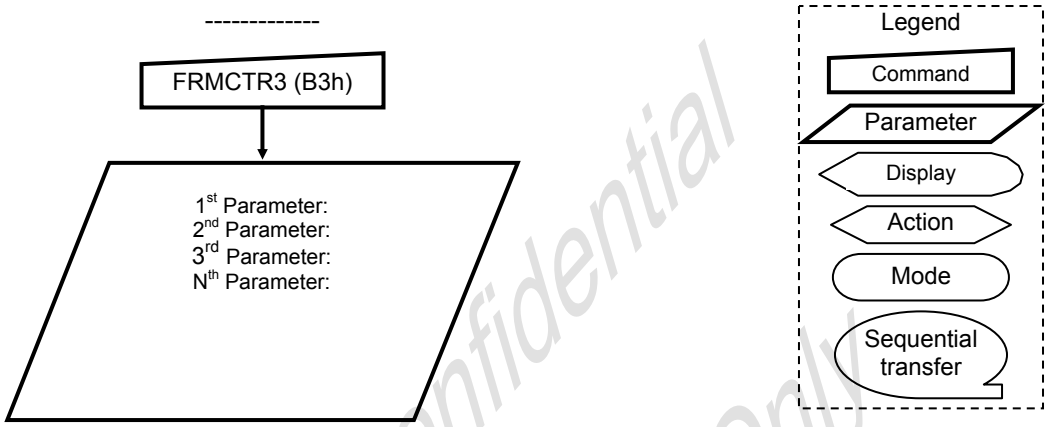
Flow Chart	

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6.3.5. INVCTR (B4h): Display Inversion Control

B4H	INVCTR (Display Inversion Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVCTR	0	↑	1	-	1	0	1	1	0	1	0	0	(B4h)
1st Parameter	1	↑	1	-	0	0	0	0	0	NLA	NLB	NLC	

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

-Display Inversion mode control

-NLA: Inversion setting in full colors normal mode (Normal mode on)

NLA	Inversion setting in full colours normal mode
0	**Line Inversion**
1	Frame Inversion

-NLB: Inversion setting in Idle mode (Idle mode on)

NLB	Inversion setting in Idle mode
0	Line Inversion
1	**Frame Inversion**

-NLC: Inversion setting in full colors partial mode (Partial mode on / Idle mode off)

NLC	Inversion setting in full colours partial mode
0	**Line Inversion**
1	Frame Inversion

Restriction

-If this register not using the register need be reserved.

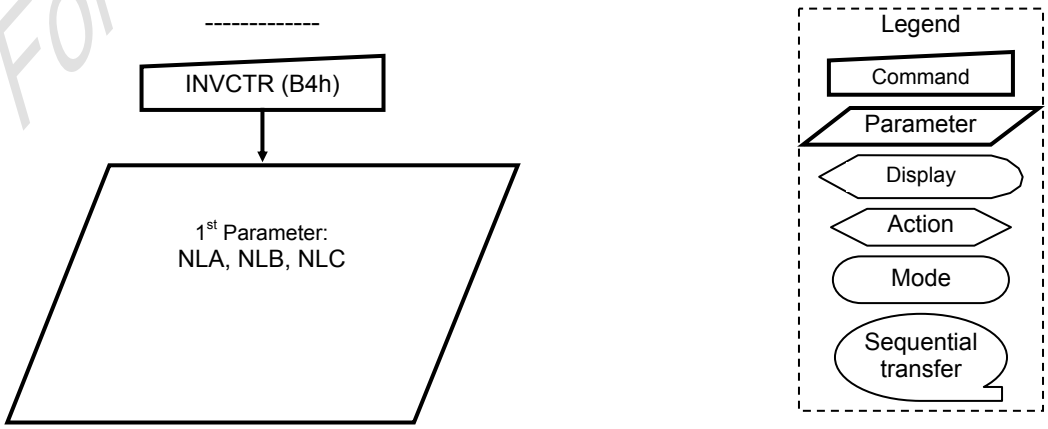
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	NLA	NLB	NLC	B4h
Power On Sequence	0d	1d	0d	02h
S/W Reset	0d	1d	0d	02h
H/W Reset	0d	1d	0d	02h

Flow Chart



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6.3.6. RGBBPCTR (B5h): RGB Interface Blanking Porch setting

B5H	RGBPSET (RGB Interface Blanking Porch setting)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RGBBPCTR	0	↑	1	-	1	0	1	1	0	1	0	1	(B5h)
1st Parameter	1	↑	1	-					VBP[3]	VBP[2]	VBP[1]	VBP[0]	-

NOTE: "-" Don't care

Description

-Set the blanking porch in the RGB interface

VBP[3:0]	Amount of Back Porch in RGB interface
0	0
1	1
2	2
3	3
4	4
…	…
D	13
E	14
F	15

Restriction

-If this register not using the register need be reserved.

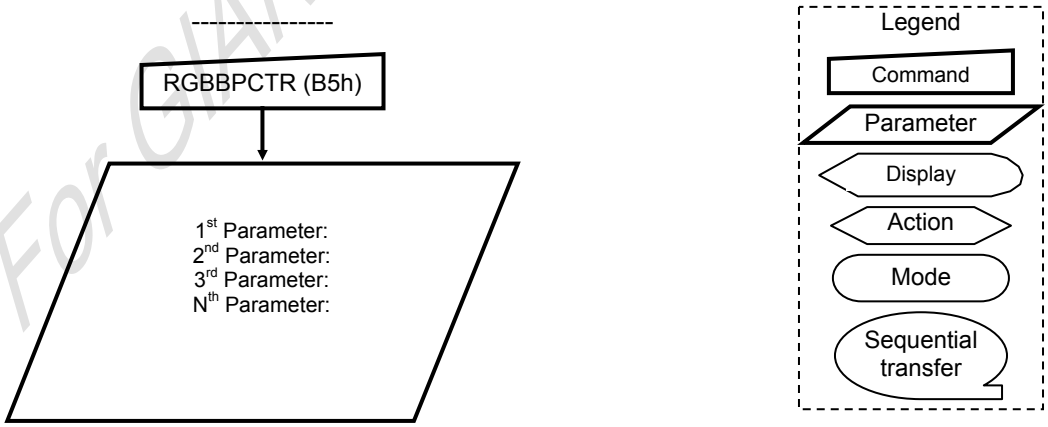
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	VBP
Power On Sequence	3d
S/W Reset	3d
H/W Reset	3d

Flow Chart



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6.3.7. DISSET5 (B6h): Display Function set 5

B6H	DISSET (Display Function set 5)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISSET5	0	↑	1	-	1	0	1	1	0	1	1	0	(B6h)
1st Parameter	1	↑	1	-	0	0	NO1	NO0	SDT1	STD0	EQ1	EQ0	
2nd Parameter	1	↑	1	-	0	0	0	0	PTG1	PTG0	PT1	PT0	

NOTE: "-" Don't care

Description

-1st parameter: Set output waveform relation.

-NO[1:0]: Set the amount of non-overlap of the gate output

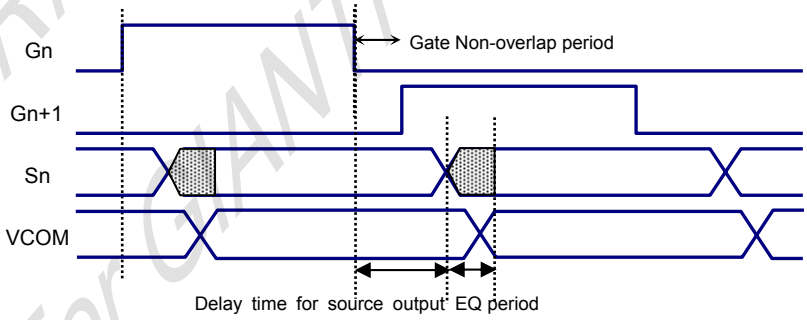
NO[1:0]		Amount of non-overlap of the gate output	
		Refer the Internal oscillator	Refer the PCLK
00	0	1 clock cycle	4 clock cycle
01	1	4 clock cycle	16 clock cycle
10	2	6 clock cycle	24 clock cycle
11	3	8 clock cycle	32 clock cycle

-SDT[1:0]: Set delay amount from gate signal falling edge of the source output.

SDT[1:0]		Amount of non-overlap of the source output	
		Refer the Internal oscillator	Refer the PCLK
00	0	1 clock cycle	4 clock cycle
01	1	2 clock cycle	8 clock cycle
10	2	3 clock cycle	12 clock cycle
11	3	4 clock cycle	16 clock cycle

-EQ[1:0]: Set the Equalizing period

EQ[1:0]		EQ period	
		Refer the Internal oscillator	Refer the PCLK
00	0	No EQ	No EQ
01	1	2 clock cycle	4 clock cycle
10	2	4 clock cycle	16 clock cycle
11	3	6 clock cycle	24 clock cycle



-2nd parameter: Set the output waveform in non-display area.

-PTG[1:0]: Determine gate output in a non-display area in the partial mode

PTG[1:0]		Gate output in a non-display area
00	0	Normal scan
01	1	Fix on VGL
10	2	Fix on VGL
11	3	Fix on VGL

-PT[1:0]: Determine Source /VCOM output in a non-display area in the partial mode

PT[1:0]		Source output on non-display area		VCOM output on non-display area	
		Positive	Negative	Positive	Negative
00	0	V63	V0	VCOML	VCOMH
01	1	V0	V63	VCOML	VCOMH
10	2	AGND	AGND	AGND	AGND
11	3	Hi-z	Hi-z	AGND	AGND

Restriction

-If this register not using the register need be reserved.

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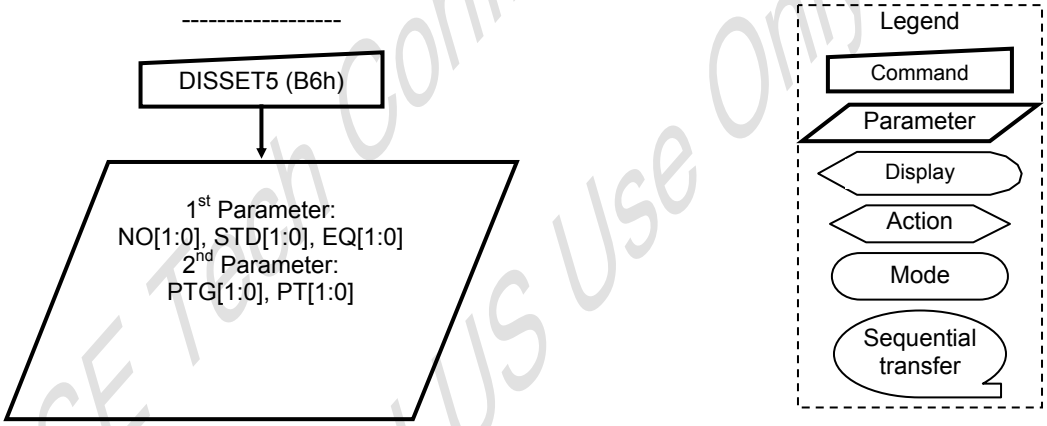
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value				
	NO[1:0]	STD[1:0]	EQ[1:0]	PTG[1:0]	PT[1:0]
Power On Sequence	1d	1d	2d	0d	2d
S/W Reset	1d	1d	2d	0d	2d
H/W Reset	1d	1d	2d	0d	2d

Flow Chart



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6.3.8. PWCTR1 (C0h): Power Control 1

C0H	PWCTR1 (Power Control 1)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR1	0	↑	1	-	1	1	0	0	0	0	0	0	(C0h)
1st Parameter	1	↑	1	-	0	0	0	VRH4	VRH3	VRH2	VRH1	VRH0	
2nd Parameter	1	↑	1	-	0	0	0	0	0	VCI2	VCI1	VCI0	

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

-Set the GVDD and VCI1 voltage

VRH[4:0]		GVDD
00000	0	5.00
00001	1	4.75
00010	2	4.70
00011	3	4.65
00100	4	4.60
00101	**5**	**4.55**
00110	6	4.50
00111	7	4.45
01000	8	4.40
01001	9	4.35
01010	10	4.30
01011	11	4.25
01100	12	4.20
01101	13	4.15
01110	14	4.10
01111	15	4.05
10000	**16**	**4.00**
10001	17	3.95
10010	18	3.90
10011	19	3.85
10100	20	3.80
10101	21	3.75
10110	22	3.70
10111	23	3.65
11000	24	3.60
11001	25	3.55
11010	26	3.50
11011	27	3.45
11100	28	3.40
11101	29	3.35
11110	30	3.25
11111	31	3.00

VC[2:0]		VCI1
000	0	2.75
001	1	2.70
010	2	2.65
011	3	2.60
100	4	2.55
101	**5**	**2.50**
110	6	x
111	7	x
000	8	

Restriction

-If this register not using the register need be reserved.

-The deviation value of GVDD between with Measurement and Specification: **Max <=50mV**

-The deviation value of VCI1 between with Measurement and Specification: **Max <=1% deviation**

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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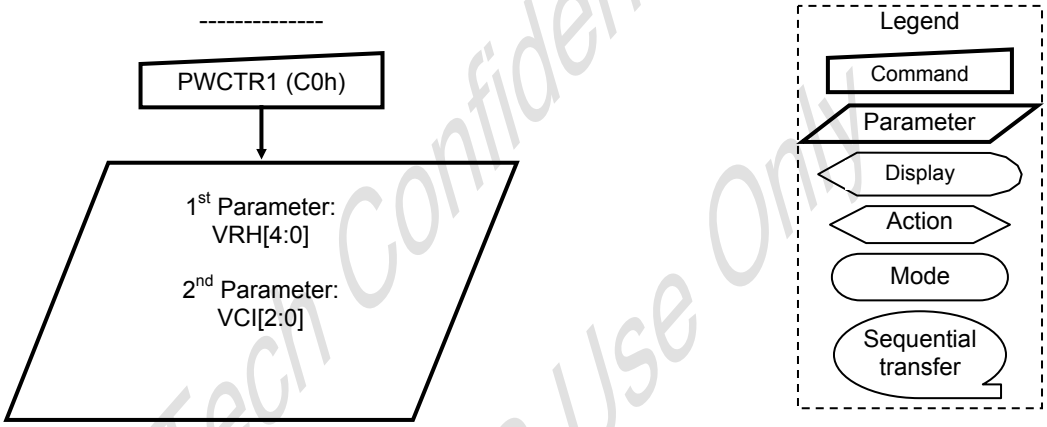
Default

Status	Default Value			
	LCM = '0' TR LC Type		LCM = '1' TM LC type	
	VRH[4:0]	VC[2:0]	VRH[4:0]	VC[2:0]
Power On Sequence	16d	5d	5d	5d
S/W Reset	16d	5d	5d	5d
H/W Reset	16d	5d	5d	5d

Flow Chart



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6.3.9. PWCTR2 (C1h): Power Control 2

C1H	PWCTR2 (Power Control 2)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR2	0	↑	1	-	1	1	0	0	0	0	0	1	(C1h)
1st Parameter	1	↑	1		0	0	0	0	0	BT2	BT1	BT0	

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

-Set the AVDD, VCL, VGH and VGL supply power level

BT[2:0]		AVDD		VCL		VGH		VGL	
000	0	2xVDDIO	4.75	-1xVDDIO	-2.45	4*VDDIO	9.80	-3*VDDIO	-7.35
001	1	2xVDDIO	4.75	-1xVDDIO	-2.45	4*VDDIO	9.80	-4*VDDIO	-9.80
010	2	2xVDDIO	4.75	-1xVDDIO	-2.45	5*VDDIO	12.25	-3*VDDIO	-7.35
011	3	2xVDDIO	4.75	-1xVDDIO	-2.45	5*VDDIO	12.25	-4*VDDIO	-9.80
100	4	2xVDDIO	4.75	-1xVDDIO	-2.45	5*VDDIO	12.25	-5*VDDIO	-12.25
101	5	2xVDDIO	4.75	-1xVDDIO	-2.45	6*VDDIO	14.70	-3*VDDIO	-7.35
110	6	2xVDDIO	4.75	-1xVDDIO	-2.45	6*VDDIO	14.70	-4*VDDIO	-9.80
111	**7**	**2xVDDIO**	**4.75**	**-1xVDDIO**	**-2.45**	**6*VDDIO**	**14.70**	**-5*VDDIO**	**-12.25**

Note: When VCI1=2.5V, Set-up cycle 1 effective=95%, Set-up cycle 2 effective=98%,

Restriction

-If this register not using the register need be reserved.

-The deviation value of VGH/ VGL between with Measurement and Specification: **Max: VGH-VGL<=1V**

-VGH-VGL <= 25V

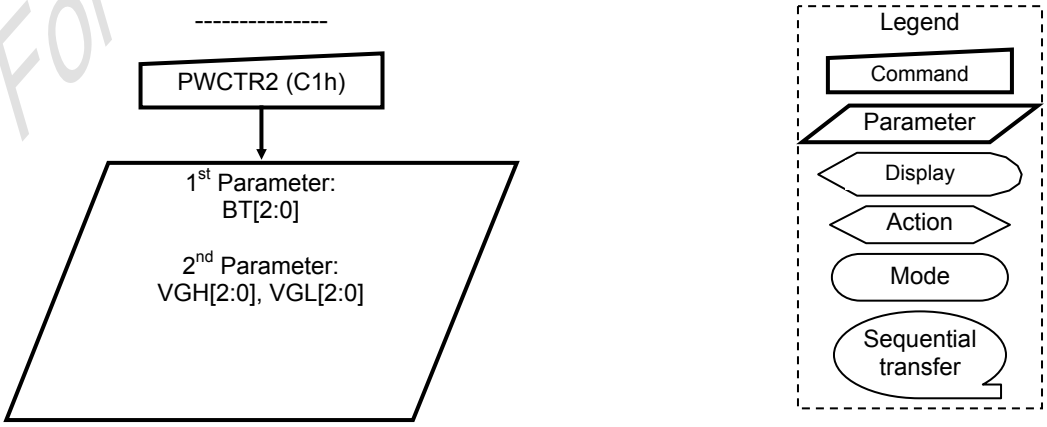
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	BT[2:0]
Power On Sequence	7d
S/W Reset	7d
H/W Reset	7d

Flow Chart



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6.3.10. PWCTR3 (C2h): Power Control 3 (in Normal mode/ Full colors)

C2H	PWCTR3 (Power Control 3)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR3	0	↑	1	-	1	1	0	0	0	0	1	0	(C2h)
1st Parameter	1	↑	1	-	0	0	0	0	0	APA2	APA1	APA0	
2nd Parameter	1	↑	1	-	0	0	0	0	0	DCA2	DCA1	DCA0	

NOTE: "-" Don't care

Description

-Set the amount of current in Operational amplifier in normal mode/full colors.

-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.

APA[2:0]		Amount of Current in Operational Amplifier
000	0	Operation of the operational amplifier stops
001	1	Small
010	2	Medium Low
011	3	Medium
100	**4**	Medium High
101	5	Large
110	6	Reserved
111	7	Reserved

-Set the Booster circuit Step-up cycle in Normal mode/ full colors.

DCA[2:0]		Step-up cycle in Booster circuit 1	Step-up cycle in Booster circuit 2,3
000	0	BCLK / 1	BCLK / 1
001	**1**	**BCLK / 1**	**BCLK / 2**
010	2	BCLK / 1	BCLK / 4
011	3	BCLK / 2	BCLK / 2
100	4	BCLK / 2	BCLK / 4
101	5	BCLK / 4	BCLK / 4
110	6	BCLK / 4	BCLK / 8
111	7	BCLK / 4	BCLK / 16

Note: BCLK is Clock frequency for Booster circuit

Restriction

-If some parameter of the register not use the register need to be reserved.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	AP[2:0]	DC[2:0]
Power On Sequence	4d	1d
S/W Reset	4d	1d
H/W Reset	4d	1d

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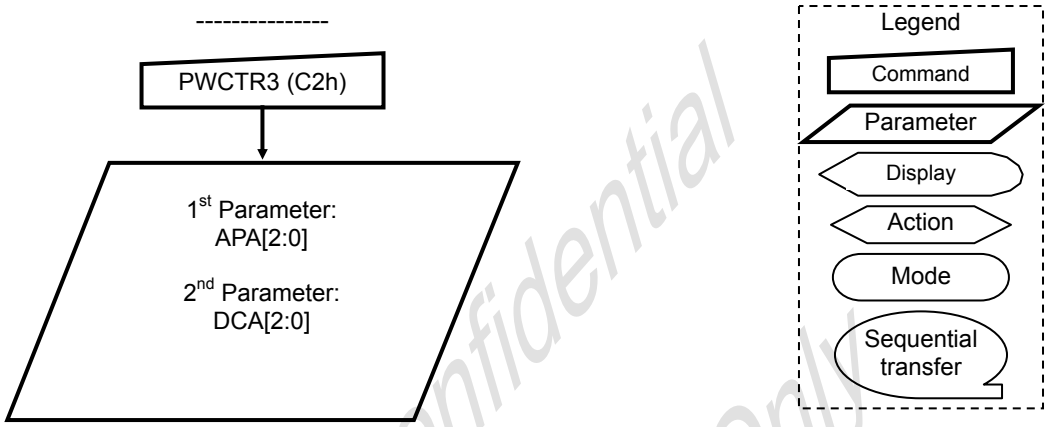
Flow Chart	

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6.3.11. PWCTR4 (C3h): Power Control 4 (in Idle mode/ 8-colors)

C3H	PWCTR4 (Power Control 4)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR4	0	↑	1	-	1	1	0	0	0	0	1	1	(C3h)
1st Parameter	1	↑	1	-	0	0	0	0	0	APB2	APB1	APB0	
2nd Parameter	1	↑	1	-	0	0	0	0	0	DCB2	DCB1	DCB0	

NOTE: "-" Don't care

Description

-Set the amount of current in Operational amplifier in Idle mode/ 8-colors.

-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.

APB[2:0]		Amount of Current in Operational Amplifier
000	0	Operation of the operational amplifier stops
001	1	Small
010	**2**	**Medium Low**
011	3	Medium
100	4	Medium High
101	5	Large
110	6	Reserved
111	7	Reserved

-Set the Booster circuit Step-up cycle in Idle mode/ 8-colors.

DCB[2:0]		Step-up cycle in Booster circuit 1	Step-up cycle in Booster circuit 2,3
000	0	BCLK / 1	BCLK / 1
001	1	BCLK / 1	BCLK / 2
010	2	BCLK / 1	BCLK / 4
011	3	BCLK / 2	BCLK / 2
100	**4**	**BCLK / 2**	**BCLK / 4**
101	5	BCLK / 4	BCLK / 4
110	6	BCLK / 4	BCLK / 8
111	7	BCLK / 4	BCLK / 16

Note: BCLK is Clock frequency for Booster circuit

Restriction

-If some parameters of the register not use the register need to be reserved.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	AP[2:0]	DC[2:0]
Power On Sequence	2d	4d
S/W Reset	2d	4d
H/W Reset	2d	4d

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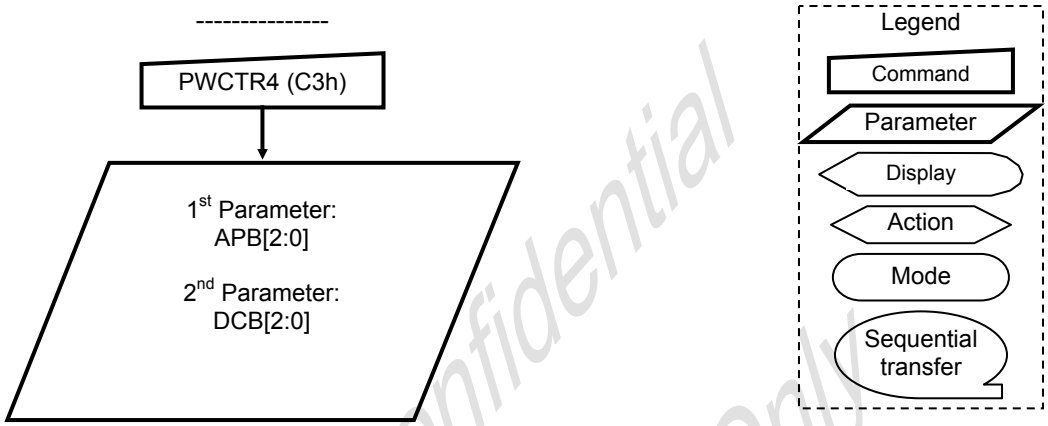
Flow Chart	

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6.3.12. PWCTR5 (C4h): Power Control 5 (in Partial mode/ full-colors)

C4H	PWCTR5 (Power Control 5)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWCTR5	0	↑	1	-	1	1	0	0	0	1	0	0	(C4h)
1st Parameter	1	↑	1	-	0	0	0	0	0	APC2	APC1	APC0	
2nd Parameter	1	↑	1	-	0	0	0	0	0	DCC2	DCC1	DCC0	

NOTE: "-" Don't care

Description

-Set the amount of current in Operational amplifier in Partial mode/ full-colors.

-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.

APC[2:0]		Amount of Current in Operational Amplifier
000	0	Operation of the operational amplifier stops
001	1	Small
010	2	Medium Low
011	**3**	**Medium**
100	4	Medium High
101	5	Large
110	6	Reserved
111	7	Reserved

-Set the Booster circuit Step-up cycle in Partial mode/ full-colors.

DCC[2:0]		Step-up cycle in Booster circuit 1	Step-up cycle in Booster circuit 2,3
000	0	BCLK / 1	BCLK / 1
001	1	BCLK / 1	BCLK / 2
010	**2**	**BCLK / 1**	**BCLK / 4**
011	3	BCLK / 2	BCLK / 2
100	4	BCLK / 2	BCLK / 4
101	5	BCLK / 4	BCLK / 4
110	6	BCLK / 4	BCLK / 8
111	7	BCLK / 4	BCLK / 16

Note: BCLK is Clock frequency for Booster circuit

Restriction

-If some parameters of the register not use the register need to be reserved.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	APC[2:0]	DCC[2:0]
Power On Sequence	3d	2d
S/W Reset	3d	2d
H/W Reset	3d	2d

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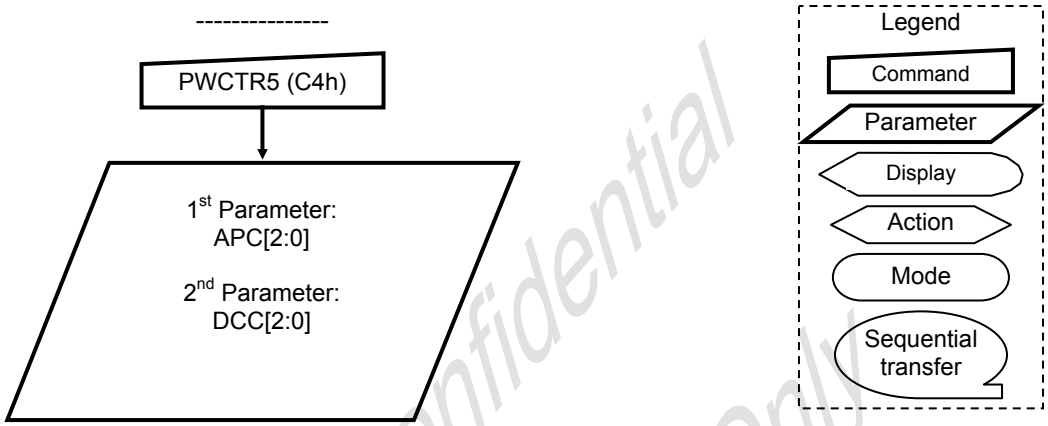
Flow Chart	

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6.3.13. VMCTR1 (C5h): VCOM Control 1

C5H	VMCTR1 (VCOM Control 1)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VMCTR1	0	↑	1	-	1	1	0	0	0	1	0	1	(C5h)
1st Parameter	1	↑	1	-	nVM *	VMH6	VMH5	VMH 4	VMH 3	VMH 2	VMH 1	VMH 0	

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

-Set **VCOMH** Voltage

VMH[6:0]		VCOMH	VMH[6:0]		VCOMH	VMH[6:0]		VCOMH	VMH[6:0]		VCOMH
0000000	0	2.500	0011011	27	3.175	0110110	54	3.850	1010001	81	4.525
0000001	1	2.525	0011100	28	3.200	0110111	55	3.875	1010010	82	4.550
0000010	2	2.550	0011101	29	3.225	0111000	56	3.900	1010011	83	4.575
0000011	3	2.575	0011110	30	3.250	0111001	57	3.925	1010100	84	4.600
0000100	4	2.600	0011111	31	3.275	0111010	58	3.950	1010101	85	4.625
0000101	5	2.625	0100000	32	3.300	0111011	59	3.975	1010110	86	4.650
0000110	6	2.650	0100001	33	3.325	0111100	60	4.000	1010111	87	4.675
0000111	7	2.675	0100010	34	3.350	0111101	61	4.025	1011000	88	4.700
0001000	8	2.700	0100011	35	3.375	0111110	62	4.050	1011001	89	4.725
0001001	9	2.725	0100100	36	3.400	0111111	63	4.075	1011010	90	4.750
0001010	10	2.750	0100101	37	3.425	1000000	64	4.100	1011011	91	4.775
0001011	11	2.775	0100110	38	3.450	1000001	65	4.125	1011100	92	4.800
0001100	12	2.800	0100111	39	3.475	1000010	66	4.150	1011101	93	4.825
0001101	13	2.825	**0101000**	**40**	**3.500**	1000011	67	4.175	1011110	94	4.850
0001110	14	2.850	0101001	41	3.525	1000100	68	4.200	1011111	95	4.875
0001111	15	2.875	0101010	42	3.550	1000101	69	4.225	1100000	96	4.900
0010000	16	2.900	0101011	43	3.575	1000110	70	4.250	1100001	97	4.925
0010001	17	2.925	0101100	44	3.600	1000111	71	4.275	1100010	98	4.950
0010010	18	2.950	0101101	45	3.625	1001000	72	4.300	1100011	99	4.975
0010011	19	2.975	0101110	46	3.650	1001001	73	4.325	1100100	100	5.000
0010100	20	3.000	0101111	47	3.675	1001010	74	4.350	1100101	101	Not Permitted
0010101	21	3.025	0110000	48	3.700	1001011	75	4.375		|	
0010110	22	3.050	0110001	49	3.725	1001100	76	4.400	1111111	127	
0010111	23	3.075	0110010	50	3.750	1001101	77	4.425			
0011000	24	3.100	0110011	51	3.775	1001110	78	4.450			
0011001	25	3.125	0110100	52	3.800	1001111	79	4.475			
0011010	**26**	**3.150**	0110101	53	3.825	1010000	80	4.500			

-Select the VCOMH value

nVM *	VCOMH value
0	**VCOMH value is from NV memory**
1	VCOMH value is from the VCOMH[6:0] setting

-The nVM need be used in 1st parameter of VMCTR1 (C5h)
- When nVM=0, the value of VMH[6:0] is from NV memory. So it must program the NV memory first.
- When nVM=1, the vaule of VMH[6:0] is from $C5 register. It can fine-tune the display performance to the best quality by setting this register, and program this optium value to NV memory.

Restriction

-If this register not using the register need be reserved.

-The deviation value of VCOMH between with Measurement and Specification: **Max <=25mV**

-The deviation value of VCOMAC between with Measurement and Specification: **Max <=50mV**

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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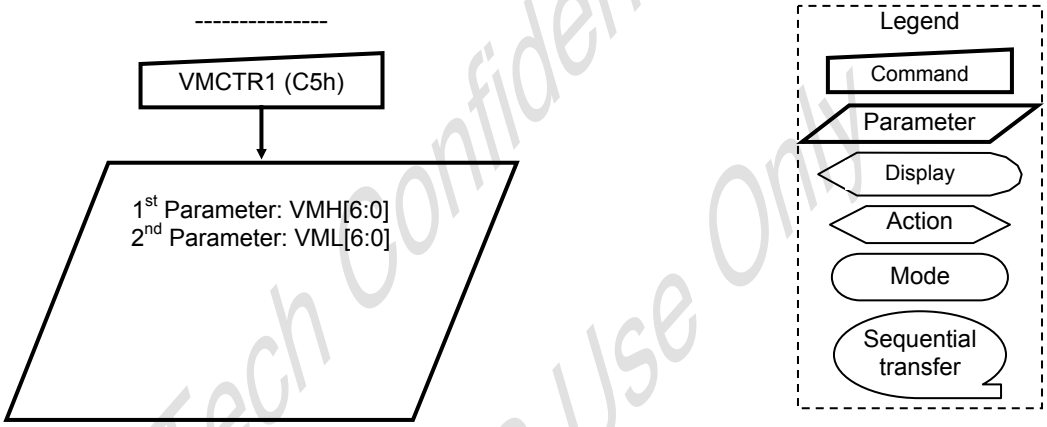
Default

Status	Default Value		
	nVM	LCM = '0' TR LC Type	LCM = '1' TM LC type
		VMH[6:0] / VML[6:0]	VMH[6:0] / VML[6:0]
Power On Sequence	0d	40d / 68d	26d / 24d
S/W Reset	0d	40d / 68d	26d / 24d
H/W Reset	0d	40d / 68d	26d / 24d

Flow Chart



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6.3.14. VMCTR2 (C6h): VCOM Control 2

C6H	VMCTR2 (VCOM Control 2)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VMCTR2	0	↑	1	-	1	1	0	0	0	1	1	0	(C6h)
1st Parameter	1	↑	1	-	0	0	VMA5	VMA4	VMA3	VMA2	VMA1	VMA0	

NOTE: "-" Don't care, can be set to VDDIO or DGND level

Description

-Set **VCOMAC** Voltage

VMA[5:0]		VCOMAC	VMA[5:0]		VCOMAC	VMA[5:0]		VCOMAC
000000	0	4.000	010000	16	4.800	100000	32	5.600
000001	1	4.050	010001	17	4.850	100001	33	5.650
000010	2	4.100	010010	18	4.900	100010	34	5.700
000011	3	4.150	010011	19	4.950	100011	35	5.750
000100	4	4.200	010100	20	5.000	100100	36	5.800
000101	5	4.250	**010101**	**21**	**5.050**	100101	37	5.850
000110	**6**	**4.300**	010110	22	5.100	100110	38	5.900
000111	7	4.350	010111	23	5.150	100111	39	5.950
001000	8	4.400	011000	24	5.200	101000	40	6.000
001001	9	4.450	011001	25	5.250	101001	41	Not Permitted
001010	10	4.500	011010	26	5.300		|	
001011	11	4.550	011011	27	5.350	111111	63	
001100	12	4.600	011100	28	5.400			
001101	13	4.650	011101	29	5.450			
001110	14	4.700	011110	30	5.500			
001111	15	4.750	011111	31	5.550			

Restriction

-If this register not use the register need be reserved.

-The deviation value of VCOMAC between with Measurement and Specification: **Max <=50mV**

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	LCM = '0' TR LC Type	LCM = '1' TM LC type
	VMA[5:0]	VMA[5:0]
Power On Sequence	6d	21d
S/W Reset	6d	21d
H/W Reset	6d	21d

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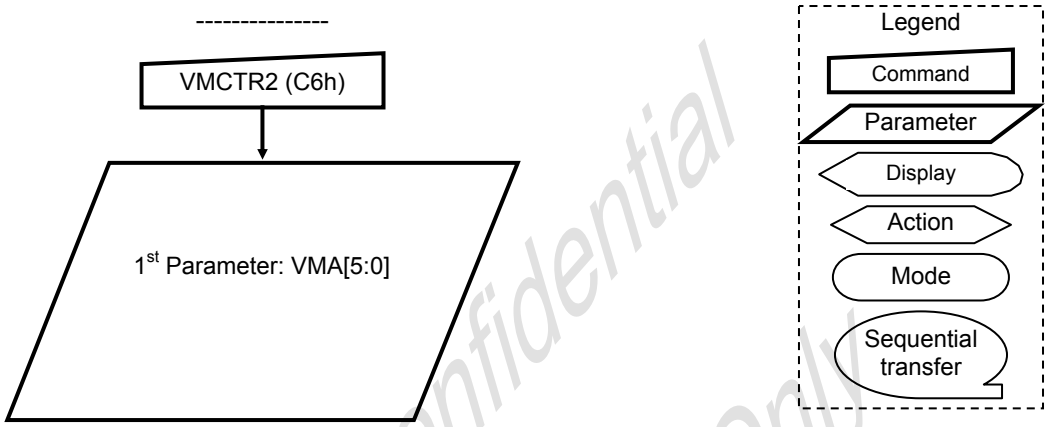
Flow Chart	

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6.3.15. RDVMH (C8h): Read the VCOMH Value NV memory

C8H	RDVMH (Read the VCOMH Value NV memory)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDVMOF	0	↑	1	-	1	1	0	0	1	0	0	0	(C8h)
1st Parameter	0	**1**	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	**1**	↑	-	nVM	RVMH6	RVMH5	RVMH4	RVMH3	RVMH2	RVMH1	RVMH0	-

NOTE: "-" Don't care

Description

-Read the VCOMH value from NV memory

-The 1st parameter is dummy data.

-The 2nd parameter is RVMH[6:0] value from NV memory or default value.

Restriction

-If this register not use the register need be reserved.

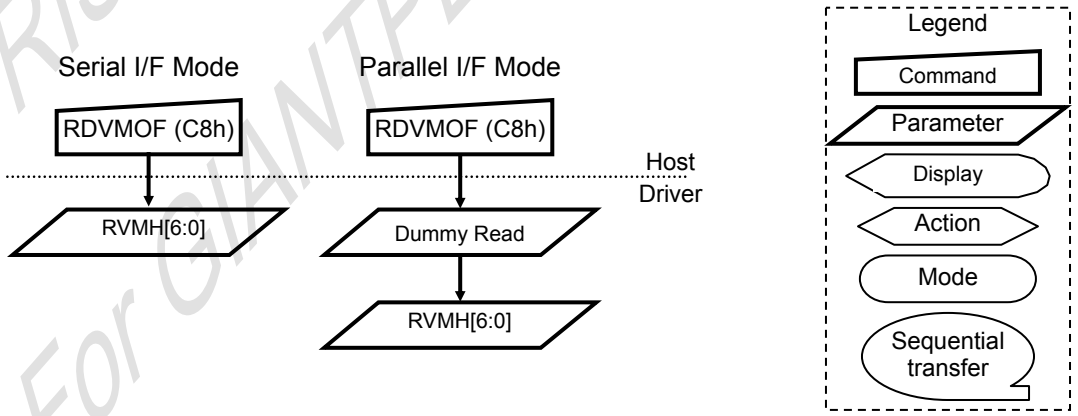
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value-
Power On Sequence	-
S/W Reset	-
H/W Reset	-

Flow Chart



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6.3.16. WRID1 (D0h): Write ID1 Value

D0H	WRID2 (Write ID2 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
WRID1	0	↑	1	-	1	1	0	1	0	0	0	0	(D0h)
1st Parameter	1	↑	1	-	1	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-

NOTE: "-" Don't care

Description

-Write 7-bits data of LCD panel maker ID code to save it to NV memory.

-The 1st parameter ID1[6:0] is LCD panel maker ID code.

Restriction

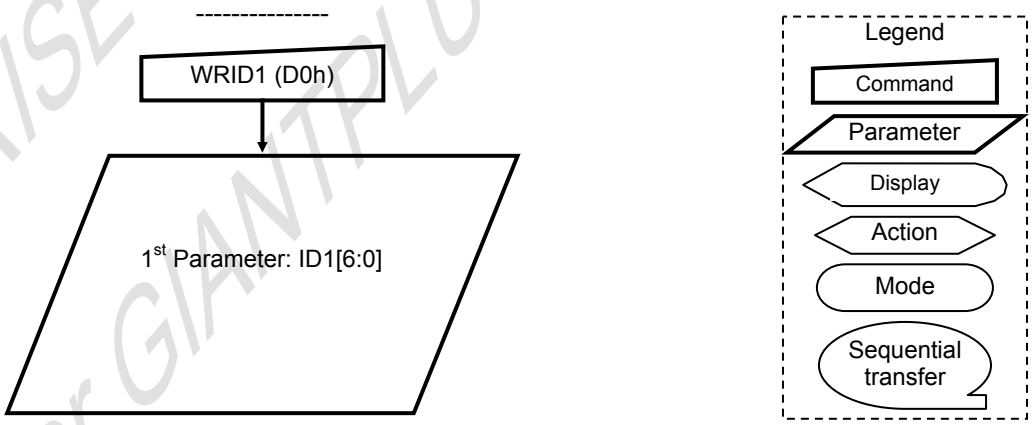
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Not Fixed
S/W Reset	Not Fixed
H/W Reset	Not Fixed

Flow Chart



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6.3.17. WRID2 (D1h): Write ID2 Value

D1H	WRID2 (Write ID2 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
WRID2	0	↑	1	-	1	1	0	1	0	0	0	1	(D1h)
1st Parameter	1	↑	1	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-

NOTE: "-" Don't care

Description

-Write 7-bits data of LCD module version to save it to NV memory.

-The 1st parameter ID2[6:0] is LCD Module version ID.

Restriction

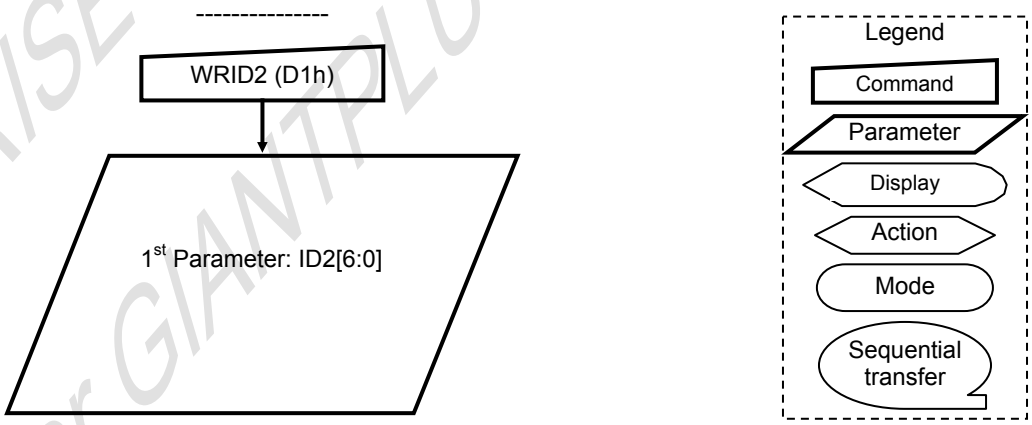
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Not Fixed
S/W Reset	Not Fixed
H/W Reset	Not Fixed

Flow Chart



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6.3.18. WRID3 (D2h): Write ID3 Value

D2H	WRID3 (Write ID3 Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
WRID3	0	↑	1	-	1	1	0	1	0	0	1	0	(D2h)
1st Parameter	1	↑	1	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	

NOTE: "-" Don't care

Description

-Write 8-bits data of project code module to save it to NV memory.

-The 1st parameter ID3[7:0] is product project ID.

Restriction

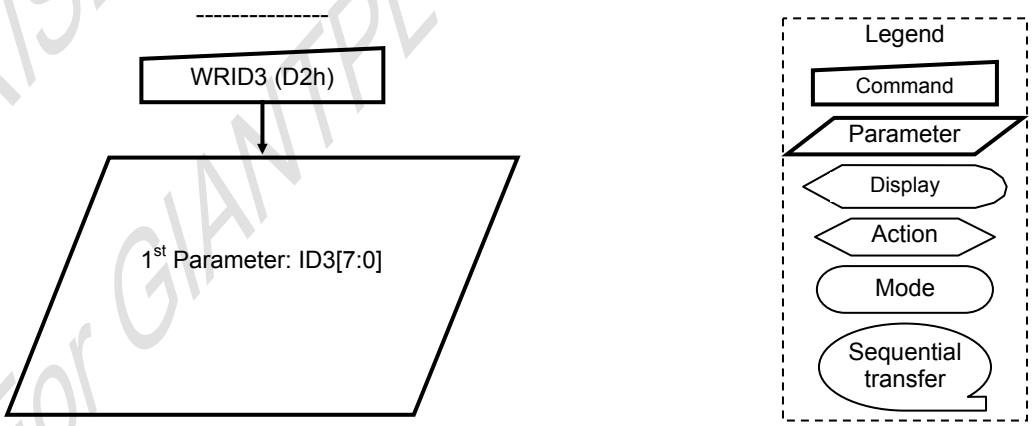
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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6.3.19. RDID4 (D3h): Read the ID4 value

D3H	RDID4 (Read the ID4 value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID4	0	↑	1	-	1	1	0	1	0	0	1	1	(D3h)
1st Parameter	1	**1**	↑	-	-	-	-	-	-	-	-	-	
2nd Parameter	1	**1**	↑	-	ID417	ID416	ID415	ID414	ID413	ID412	ID411	ID410	-
3rd Parameter	1	**1**	↑	-	ID427	ID426	ID425	ID424	ID423	ID422	ID421	ID420	-
4th Parameter	1	**1**	↑	-	ID437	ID436	ID435	ID434	ID433	ID432	ID431	ID430	-
5th Parameter	1	**1**	↑	-	ID447	ID446	ID445	ID444	ID443	ID442	ID441	ID440	-

NOTE: "-" Don't care

Description

-Read the Driver IC information from mask value.
-The 1st parameter is dummy data.
-The 2nd parameter ID41[7:0] is Driver IC ID code.
  -ID41[7:0] is 06H.
-The 3rd parameter ID42[7:0] is Driver IC Part number ID. It is 14H.
-The 4th & 5th parameter ID43[7:0] & ID44[7:0] are Driver IC version ID.

Restriction

-

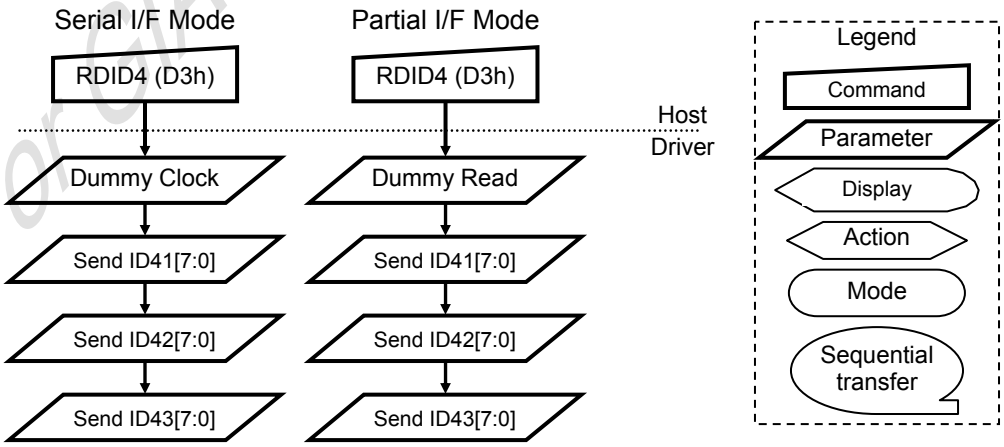
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value-			
	ID41[7:0]	ID42[7:0]	ID43[7:0]	ID44[7:0]
Power On Sequence	06H	14H	00H	01H
S/W Reset	06H	14H	00H	01H
H/W Reset	06H	14H	00H	01H

Flow Chart



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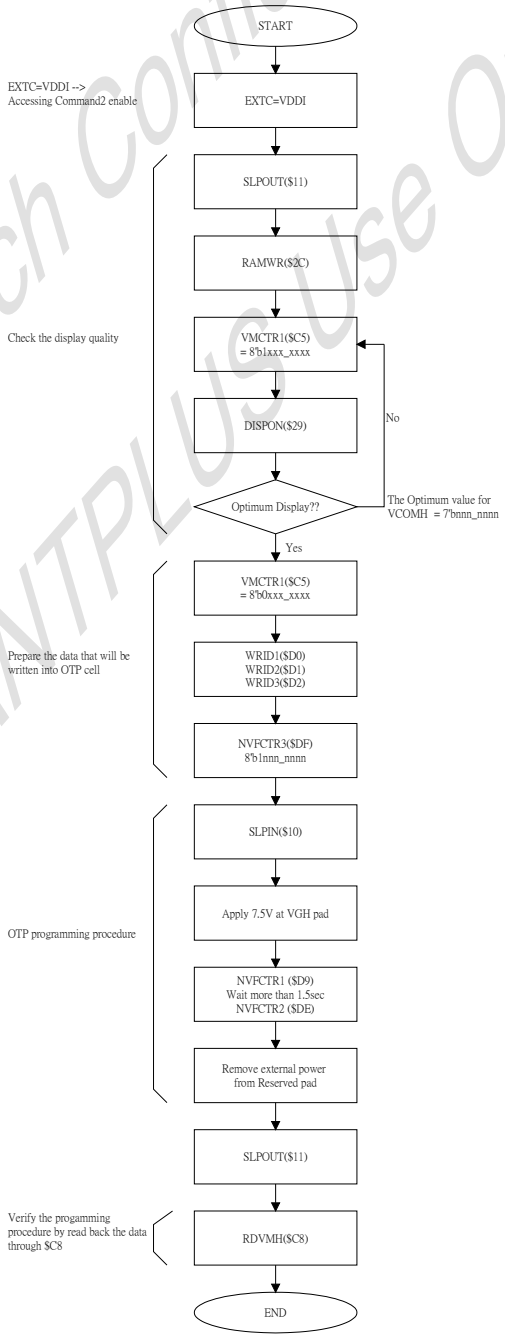
6.3.20. NVFCTR1 (D9h): NV Memory Function Controller 1

D9H	NVFCTR1 (NV Memory Function Controller 1)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NVFCTR1	0	↑	1	-	1	1	0	1	1	0	0	1	(D9h)
1st Parameter	1	↑	1	-	WVMH 7	WVMH 6	WVMH 5	WVMH 4	WVMH 3	WVMH 2	WVMH 1	WVMH 0	-

NOTE: "-" Don't care1

Description

- Write WVMH[6:0] for VCOMH voltage to $D9 when the value is considered as the optimum for display quality.
- The endurence for SPFD54124B NV memory is 4 times for ID1 ,ID2, ID3, and VCOMH.



Restriction

The endurence of ID1, ID2, ID3, and WVMH is 4 times.

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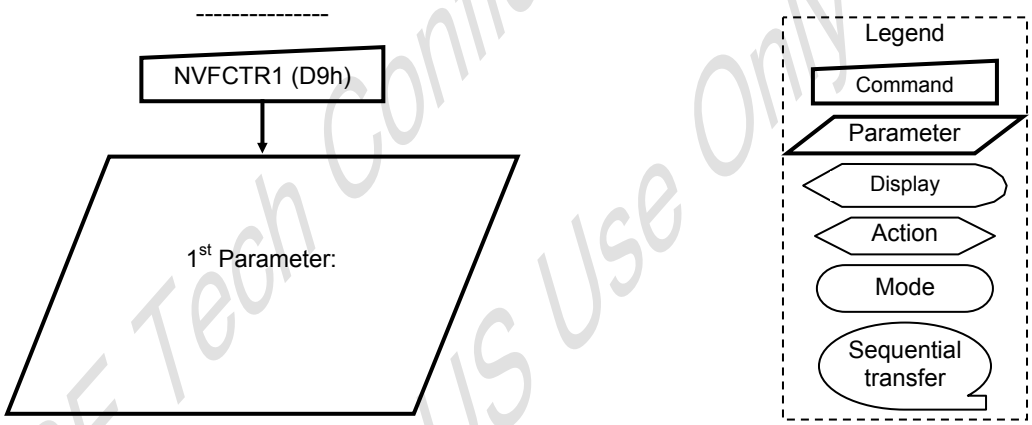
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Not Fixed
S/W Reset	Not Fixed
H/W Reset	Not Fixed

Flow Chart



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6.3.21. NVFCTR2 (DEh): NV Memory Function Controller 2

DEH	NVFCTR2 (NV Memory Function Controller 2)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NVFCTR2	0	↑	1	-	1	1	0	1	1	1	1	0	(DEh)
1st Parameter	1	↑	1	-	1								-

NOTE: "-" Don't care

Description

- Please refer to $D9 for details.

Restriction

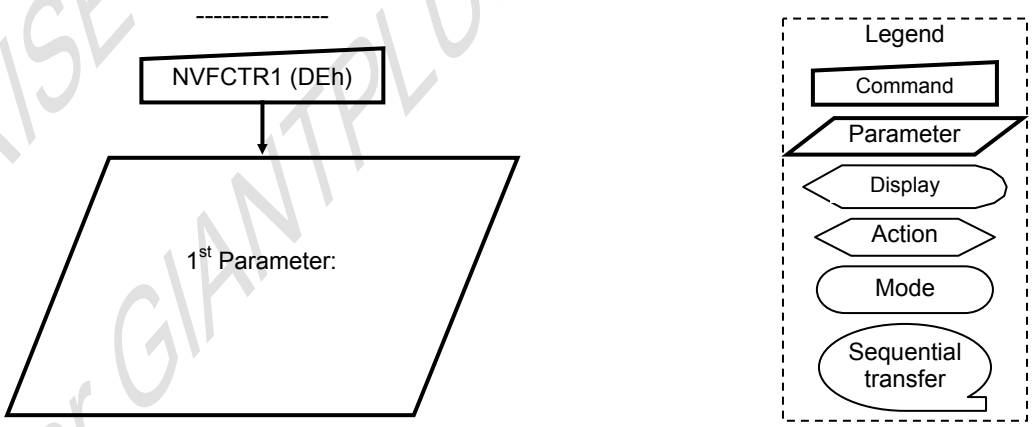
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Not Fixed
S/W Reset	Not Fixed
H/W Reset	Not Fixed

Flow Chart



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6.3.22. NVFCTR3 (DFh): NV Memory Function Controller 3

DEH	NVFCTR3 (NV Memory Function Controller 3)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NVFCTR3	0	↑	1	-	1	1	0	1	1	1	1	1	(DFh)
1st Parameter	1	↑	1	-	1								-

NOTE: "-" Don't care

Description

- Please refer to $D9 for details.

Restriction

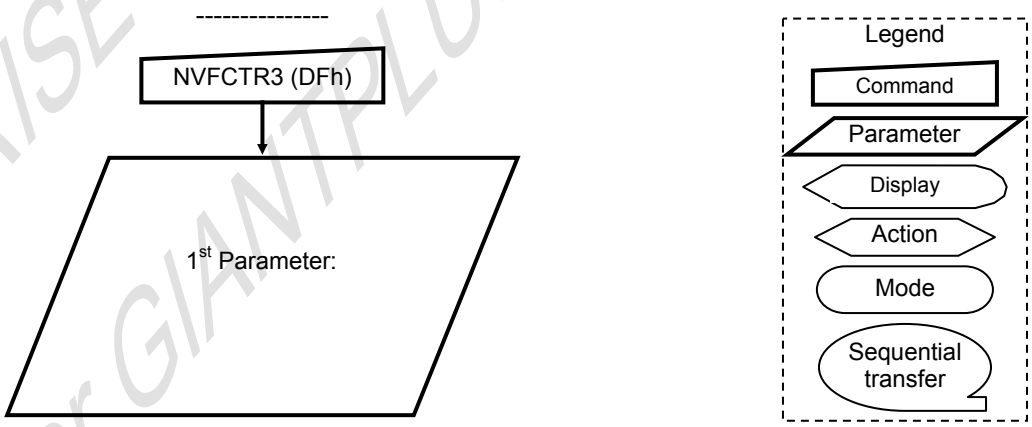
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Not Fixed
S/W Reset	Not Fixed
H/W Reset	Not Fixed

Flow Chart



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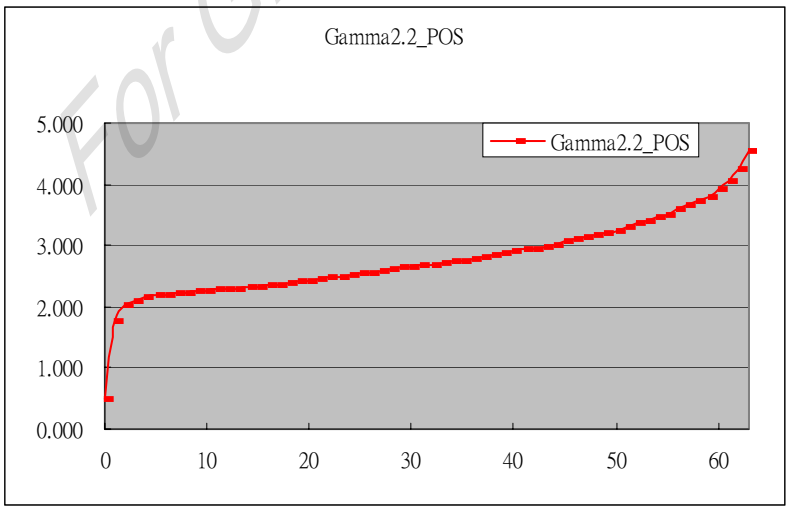
6.3.23. GMCTRP1 (E0h): Gamma Correction Characteristics Setting

E0H	GMCTRP1 (Gamma '+'polarity Correction Characteristics Setting)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GMCTRP1	0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)
1st Parameter	1	↑	1	-	-	-	-	PVR1 V0[4]	PVR1 V0[3]	PVR1 V0[2]	PVR1 V0[1]	PVR1 V0[0]	
2nd Parameter	1	↑	1	-	-	-	PVR1 V1[5]	PVR1 V1[4]	PVR1 V1[3]	PVR1 V1[2]	PVR1 V1[1]	PVR1 V1[0]	
3rd Parameter	1	↑	1	-	-	-	PVR1 V2[5]	PVR1 V2[4]	PVR1 V2[3]	PVR1 V2[2]	PVR1 V2[1]	PVR1 V2[0]	
4th Parameter	1	↑	1	-	-	-	PVR1 V61[5]	PVR1 V61[4]	PVR1 V61[3]	PVR1 V61[2]	PVR1 V61[1]	PVR1 V61[0]	
5th Parameter	1	↑	1	-	-	-	PVR1 V62[5]	PVR1 V62[4]	PVR1 V62[3]	PVR1 V62[2]	PVR1 V62[1]	PVR1 V62[0]	
6th Parameter	1	↑	1	-	-	-	-	PVR1 V63[4]	PVR1 V63[3]	PVR1 V63[2]	PVR1 V63[1]	PVR1 V63[0]	
7th Parameter	1	↑	1	-	-	-	-	PVR2 V13[4]	PVR2 V13[3]	PVR2 V13[2]	PVR2 V13[1]	PVR2 V13[0]	
8th Parameter	1	↑	1	-	-	-	-	PVR2 V50[4]	PVR2 V50[3]	PVR2 V50[2]	PVR2 V50[1]	PVR2 V50[0]	
9th Parameter	1	↑	1	-	-	-	-	-	PVR3 V4[3]	PVR3 V4[2]	PVR3 V4[1]	PVR3 V4[0]	
10th Parameter	1	↑	1	-	-	-	-	-	PVR3 V8[3]	PVR3 V8[2]	PVR3 V8[1]	PVR3 V8[0]	
11th Parameter	1	↑	1	-	-	-	-	-	PVR3 V20[3]	PVR3 V20[2]	PVR3 V20[1]	PVR3 V20[0]	
12th Parameter	1	↑	1	-	-	-	-	-	PVR3 V27[3]	PVR3 V27[2]	PVR3 V27[1]	PVR3 V27[0]	
13th Parameter	1	↑	1	-	-	-	-	-	PVR3 V36[3]	PVR3 V36[2]	PVR3 V36[1]	PVR3 V36[0]	
14th Parameter	1	↑	1	-	-	-	-	-	PVR3 V43[3]	PVR3 V43[2]	PVR3 V43[1]	PVR3 V43[0]	
15th Parameter	1	↑	1	-	-	-	-	-	PVR3 V55[3]	PVR3 V55[2]	PVR3 V55[1]	PVR3 V55[0]	
16th Parameter	1	↑	1	-	-	-	-	-	PVR3 V59[3]	PVR3 V59[2]	PVR3 V59[1]	PVR3 V59[0]	

NOTE: "-" Don't care

Description	-The default vaule for gamma register is for MVA LC type, GAMMA curve 2.2. -The gamma volatge 
Restriction	

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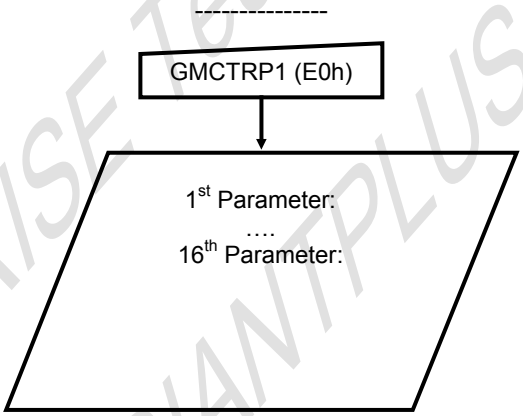
Register Availability

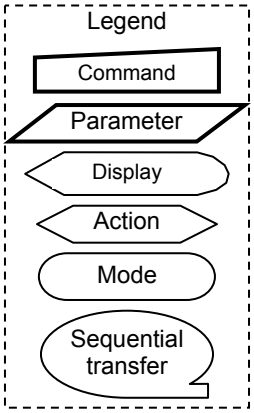
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

	Gamma 1.0 POS	Gamma 1.8 POS	Gamma 2.2 POS	Gamma 2.5 POS
VR1_V0_[4:0]	0	0	0	0
VR1_V1_[5:0]	5	8	9	0
VR1_V2_[5:0]	9	12	14	15
VR1_V61_[5:0]	63	60	58	53
VR1_V62_[5:0]	63	58	50	28
VR1_V63_[4:0]	7	7	7	7
VR2_V13_[4:0]	14	23	24	23
VR2_V50_[4:0]	7	0	0	5
VR3_V4_[3:0]	5	5	6	6
VR3_V8_[3:0]	6	3	4	4
VR3_V20_[3:0]	13	12	14	14
VR3_V27_[3:0]	8	15	15	14
VR3_V36_[3:0]	4	0	0	0
VR3_V43_[3:0]	4	3	2	2
VR3_V55_[3:0]	5	4	6	6
VR3_V59_[3:0]	11	10	12	13

Flow Chart





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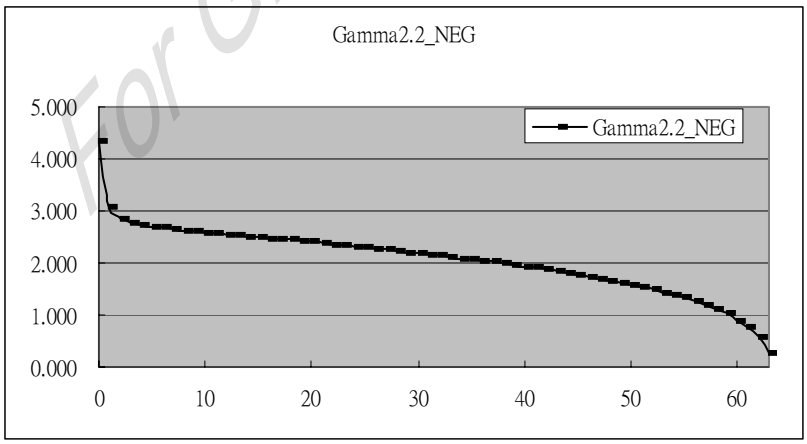
6.3.24. GMCTRP1 (E1h): Gamma Correction Characteristics Setting

E1H	GMCTRN1 (Gamma '-'polarity Correction Characteristics Setting)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GMCTRN1	0	↑	1	-	1	1	1	0	0	0	0	1	(E1h)
1st Parameter	1	↑	1	-	-	-	-	NVR1 V0[4]	NVR1 V0[3]	NVR1 V0[2]	NVR1 V0[1]	NVR1 V0[0]	
2nd Parameter	1	↑	1	-	-	-	NVR1 V1[5]	NVR1 V1[4]	NVR1 V1[3]	NVR1 V1[2]	NVR1 V1[1]	NVR1 V1[0]	
3rd Parameter	1	↑	1	-	-	-	NVR1 V2[5]	NVR1 V2[4]	NVR1 V2[3]	NVR1 V2[2]	NVR1 V2[1]	NVR1 V2[0]	
4th Parameter	1	↑	1	-	-	-	NVR1 V61[5]	NVR1 V61[4]	NVR1 V61[3]	NVR1 V61[2]	NVR1 V61[1]	NVR1 V61[0]	
5th Parameter	1	↑	1	-	-	-	NVR1 V62[5]	NVR1 V62[4]	NVR1 V62[3]	NVR1 V62[2]	NVR1 V62[1]	NVR1 V62[0]	
6th Parameter	1	↑	1	-	-	-	-	NVR1 V63[4]	NVR1 V63[3]	NVR1 V63[2]	NVR1 V63[1]	NVR1 V63[0]	
7th Parameter	1	↑	1	-	-	-	-	NVR2 V13[4]	NVR2 V13[3]	NVR2 V13[2]	NVR2 V13[1]	NVR2 V13[0]	
8th Parameter	1	↑	1	-	-	-	-	NVR2 V50[4]	NVR2 V50[3]	NVR2 V50[2]	NVR2 V50[1]	NVR2 V50[0]	
9th Parameter	1	↑	1	-	-	-	-	-	NVR3 V4[3]	NVR3 V4[2]	NVR3 V4[1]	NVR3 V4[0]	
10th Parameter	1	↑	1	-	-	-	-	-	NVR3 V8[3]	NVR3 V8[2]	NVR3 V8[1]	NVR3 V8[0]	
11th Parameter	1	↑	1	-	-	-	-	-	NVR3 V20[3]	NVR3 V20[2]	NVR3 V20[1]	NVR3 V20[0]	
12th Parameter	1	↑	1	-	-	-	-	-	NVR3 V27[3]	NVR3 V27[2]	NVR3 V27[1]	NVR3 V27[0]	
13th Parameter	1	↑	1	-	-	-	-	-	NVR3 V36[3]	NVR3 V36[2]	NVR3 V36[1]	NVR3 V36[0]	
14th Parameter	1	↑	1	-	-	-	-	-	NVR3 V43[3]	NVR3 V43[2]	NVR3 V43[1]	NVR3 V43[0]	
15th Parameter	1	↑	1	-	-	-	-	-	NVR3 V55[3]	NVR3 V55[2]	NVR3 V55[1]	NVR3 V55[0]	
16th Parameter	1	↑	1	-	-	-	-	-	NVR3 V59[3]	NVR3 V59[2]	NVR3 V59[1]	NVR3 V59[0]	

NOTE: "-" Don't care

Description	-The default vaule for gamma register is for MVA LC type, GAMMA curve 2.2. -The gamma volatge 
Restriction	

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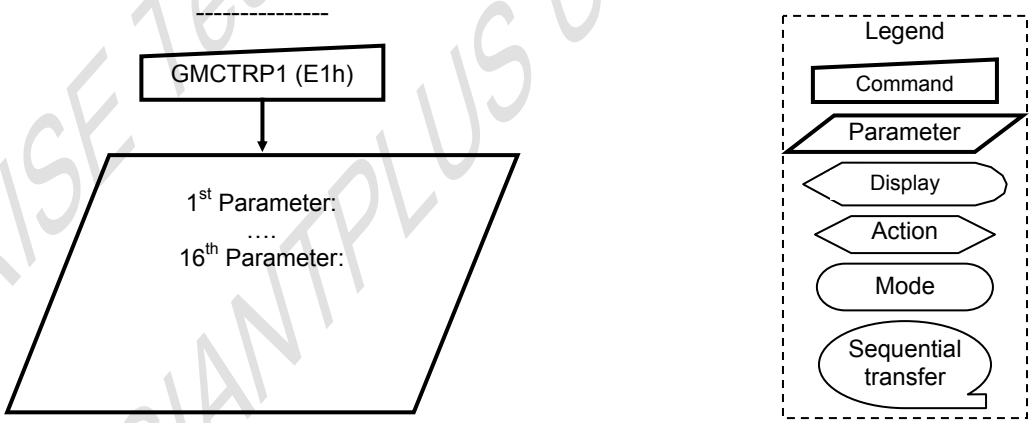
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

	Gamma 1.0 NEG	Gamma 1.8 NEG	Gamma 2.2 NEG	Gamma 2.5 NEG
VR1_V0_[4:0]	0	3	3	3
VR1_V1_[5:0]	56	49	42	19
VR1_V2_[5:0]	58	51	49	44
VR1_V61_[5:0]	18	21	22	23
VR1_V62_[5:0]	14	16	17	18
VR1_V63_[4:0]	5	4	4	4
VR2_V13_[4:0]	5	1	1	5
VR2_V50_[4:0]	18	22	24	23
VR3_V4_[3:0]	2	6	6	14
VR3_V8_[3:0]	1	5	6	7
VR3_V20_[3:0]	5	6	3	2
VR3_V27_[3:0]	2	3	0	0
VR3_V36_[3:0]	10	13	14	13
VR3_V43_[3:0]	10	12	14	14
VR3_V55_[3:0]	1	4	4	5
VR3_V59_[3:0]	2	5	6	7

Flow Chart



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7. FUNCTION DESCRIPTIONS

7.1. MCU & RGB Interface

The SPFD54124B features System interfaces and RGB interface to satisfy various needs of small or medium size's LCD panel. Based on the application requirements, there are two display modes mostly used in the LCD end product.

1. Still picture display mode
2. Moving picture display mode.

System interface is suitable for still picture display while RGB interface are suitable for moving picture display. Table 7.1 summarizes different interfaces for various display requirements.

Table 7.1 MCU & RGB Interface Comparisons table

Function	RCM1, RCM0		RCM1, RCM0			
Mode selection 1	"0x"		"10"		"11"	
	8080/ 6800 IF + SPI I/F		RGB I/F + SPI I/F			
	MCU Mode		RGB Mode 1		RGB Mode 2	
Mode selection 2	IMx=	IMx="00"	ICM='0'	ICM='1'	ICM='0'	ICM='1'
	8080/ 6800 IF	SPI I/F	RGB-1 I/F + SPI I/F		RGB-2 I/F + SPI I/F	
Motion /Still selection	Motion or Still picture	Still picture	Motion or Still picture	Still picture	Motion or Still picture	Still picture
Input data	D[17:0]	D0 = SDA	D[17:0]	SDA H/W pin enable	D[17:0]	SDA H/W pin enable
Input signal	CSX	D/CX = SCL	PCLK	D/CX = SCL	PCLK	D/CX = SCL
	WRX (R/WX), RDX (E)	CSX	VS, HS, DE	CSX	VS, HS, DE	CSX
GRAM Write cycle	Refer the WRX cycle	Refer SCL	Refer PCLK	Refer SCL	Refer PCLK	Refer SCL
GRAM Read Cycle	Refer Internal Oscillator	Refer Internal Oscillator	Refer PCLK	Refer Internal Oscillator	Refer PCLK	Refer Internal Oscillator
Command setting	D[7:0]	SDA (D0)	SDA	SDA	SDA	SDA
SMX, SMY, SRGB	-When Power On or H/W reset, those function follow H/W pins setting first.					
TE Function	-By command setting		-By command setting		-By Command setting	
Normal / Partial mode	-By command setting		-By command setting		-By Command setting	
Idle Mode (IDM H/W pin)	-By command setting -Don't care in this mode, but should be set to VDDIO or DGND				-By IDM H/W pin -IDM On/OFF (39h/28h) are disable	
Display On/ Off (SHUT H/W pin)					-By SHUT H/W pin -SLPIN(10h), SLPOUT(11h), Display On/OFF (29h/28h) are disable	
Data inverter setting (REV H/W pin)					-By REV H/W pin -INVON/OFF (21h/20h) are disable	
DE H/W pin	-Don't care in this mode, but should be set to VDDIO or DGND		-The data latched by rising edge of PCLK when DE='1' -When display data coming the DE signal should be VDDIO level		-When DE='0' area, the data of GRAM will keep the same status.	
RL H/W pin			-Don't care in this mode, but should be set to VDDIO or DGND		-By H/W pin -No commands conflict	
TB H/W pin						
Blanking porch	-Don't care in this mode		-Control by DE signal		-Control by RGBBPCTR (B5h)	
Colors format	-Control by IFPF[2:0] of COLMOD(3A)		-Control by VIPF[3:0] of COLMOD(3A)			

Note 1: RCM1 and RCM0 are H/W setting pins.

Note 2: In RGB + SPI I/F (RCM="1x"), VS, HS, DE, PCLK and D[17:0] are Hi-Z by Driver and can be stop for Host, when ICM='1'.

Note 3: In RGB + SPI I/F (RCM="1x"), the data deliver via GRAM

Note 4: When Power on Driver IC should be detect SMX, SMY, SRGB H/W setting

Note 5: When Power on Driver IC should be detect RCM1, RCM0 H/W setting and get into the I/F mode.

Note 6: When Power on Driver IC should be detect LCM1, LCM0 H/W setting and get into the setting mode.

Note 7: When Power on Driver IC should be detect GM1, GM0 H/W setting and get into the setting mode.

7.2. MPU Interface

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7.2.1. Interface Type Selection

The MPU interfaces of SPFD54124B support 8-bit, 9-bit, 16-bit, and 18-bit's 80- or 68-system Interface and Serial Peripheral Interface (SPI), which can be set by the P68 and IM2/1/0 pins. The MPU interface can set instructions and access RAM. Table 7.2.1 depicts the interface corresponding to P68and IM2/1/0 settings.

Table 7.2.1

SPI4	P68	IM2	IM1	IM0	Interface	Read back selection
0	0	0	-	-	3-Pin Serial interface	Via the read instruction (8-bits, 24-bits and 32-bits read parameter
-	0	1	0	0	8080 MCU 8-bits Parallel	RDX strobe (8-bits read data and 8-bits read parameter)
-	0	1	0	1	8080 MCU 16-bits Parallel	RDX strobe (16-bits read data and 8-bits read parameter)
-	0	1	1	0	8080 MCU 9-bits Parallel	RDX strobe (9-bits read data and 8-bits read parameter)
-	0	1	1	1	8080 MCU 18-bits Parallel	RDX strobe (18-bits read data and 8-bits read parameter)
0	1	0	-	-	3-Pin Serial interface	Via the read instruction (8-bits, 24-bits and 32-bits read parameter
-	1	1	0	0	6800 MCU 8-bits Parallel	E strobe (8-bits read data and 8-bits read parameter)
-	1	1	0	1	6800 MCU 16-bits Parallel	E strobe (16-bits read data and 8-bits read parameter)
-	1	1	1	0	6800 MCU 9-bits Parallel	E strobe (9-bits read data and 8-bits read parameter)
-	1	1	1	1	6800 MCU 18-bits Parallel	E strobe (18-bits read data and 8-bits read parameter)
1	-	0	-	-	4-Pin Serial interface	Via the read instruction (8-bits, 24-bits and 32-bits read parameter

7.2.2. 8080-Series Parallel interface(P68='0')

The MCU uses a 11-wires 8-data parallel interface or 19-wires 16-data parallel interface or 12-wires 9-data parallel interface or 21-wires 18-data parallel interface. The chip-select CSX(active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write, RDX is the parallel data read and D[17:0] is parallel data.

The Graphics Controller Chip reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits are display RAM data or command parameters. When D/C='0', D[17:0] bits are commands.

The 8080-series bi-directional interface can be used for communication between the micro controller and LCD driver chip. The selection of this interface is done when P68 pin is low state (DGND). Interface bus width can be selected with IM2, IM1 and IM0.

The interface function of 8080-series parallel interface are given in Table 7 2.2

Table 7.2.2 The function of 8080-series parallel interface

P68	IM2	IM1	IM0	Interface	D/CX	RDX	WRX	Function
0	1	0	0	8-bits Parallel	0	1	↑	Write 8-bits command (D7 to D0)
					1	1	↑	Write 8-bits display data or 8-bits parameter (D7 to D0)
					1	↑	1	Read 8-bits command (D7 to D0)
					1	↑	1	Read 8-bits parameter or status (D7 to D0)
0	1	0	1	16-bits Parallel	0	1	↑	Write 8-bits command (D7 to D0)
					1	1	↑	Write 16-bits display data (D15 to D0) or 8-bits parameter (D7 to D0)
					1	↑	1	Read 8-bits command (D7 to D0)
					1	↑	1	Read 8-bits parameter or status (D7 to D0)
0	1	1	0	9-bits Parallel	0	1	↑	Write 8-bits command (D7 to D0)
					1	1	↑	Write 9-bits display data (D8 to D0) or 8-bits parameter (D7 to D0)
					1	↑	1	Read 8-bits command (D7 to D0)
					1	↑	1	Read 8-bits parameter or status (D7 to D0)
0	1	1	1	18-bits Parallel	0	1	↑	Write 8-bits command (D7 to D0)
					1	1	↑	Write 18-bits display data (D17 to D0) or 8-bits parameter (D7 to D0)
					1	↑	1	Read 8-bits command (D7 to D0)
					1	↑	1	Read 8-bits parameter or status (D7 to D0)

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7.2.2.1 Write cycle sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control (D/CX, RDX, WRX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data (='1').

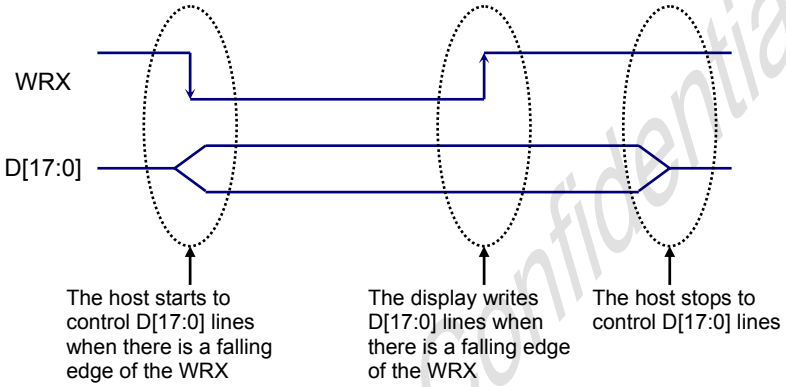

Fig. 7.2.2.1.1 8080-Series WRX Protocol

Note: WRX is an unsynchronized signal (It can be stopped)

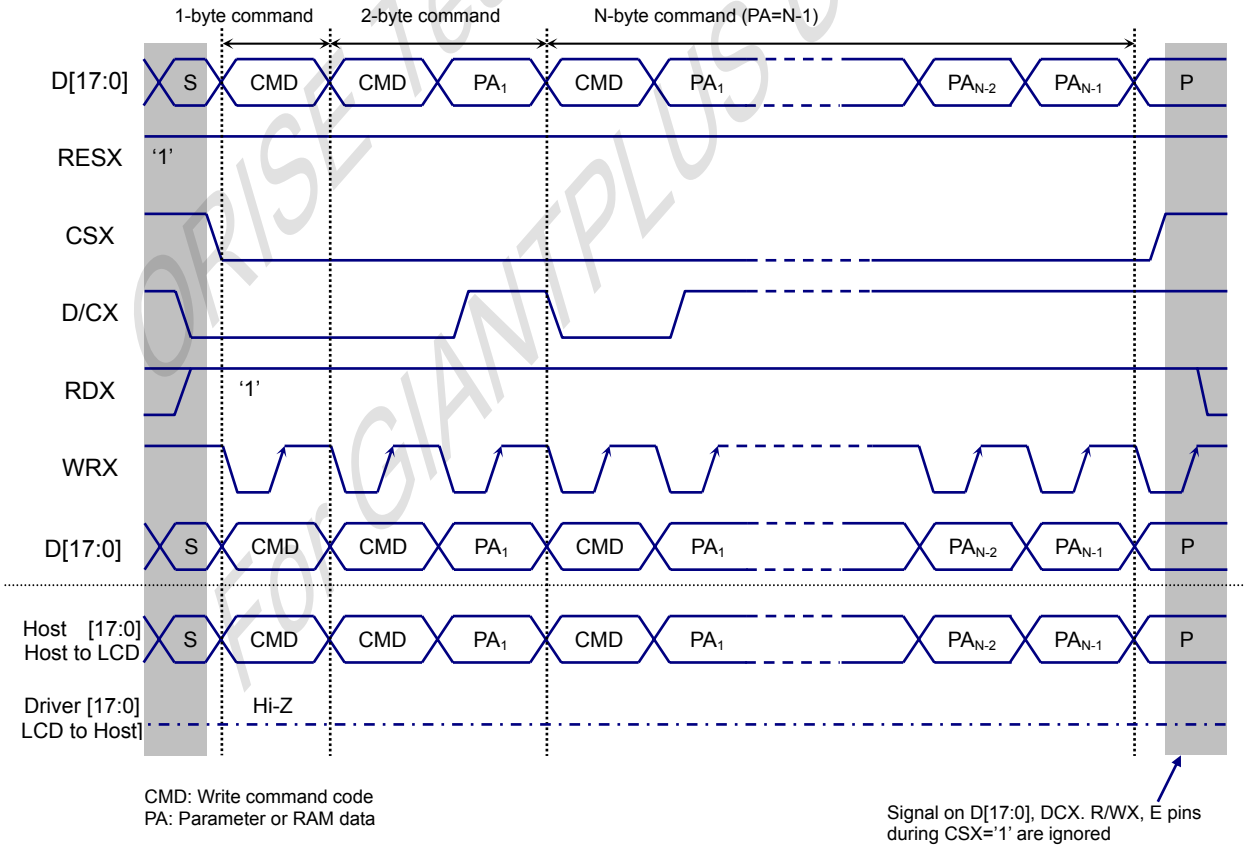

Fig. 7.2.2.1.2 8080-Series parallel bus protocol, Write to register or display RAM

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7.2.2.2 Read Cycle Sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from display via interface. The display sends data (D[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

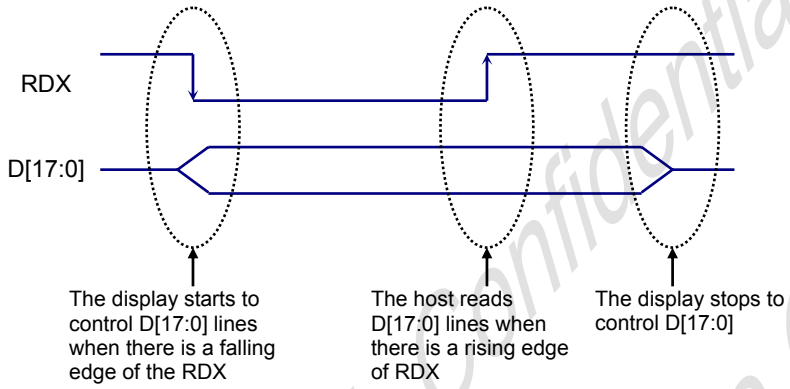

Fig. 7.2.2.2.1 8080-Series RDX Protocol

Note: RDX is an unsynchronized signal (It can be stopped)

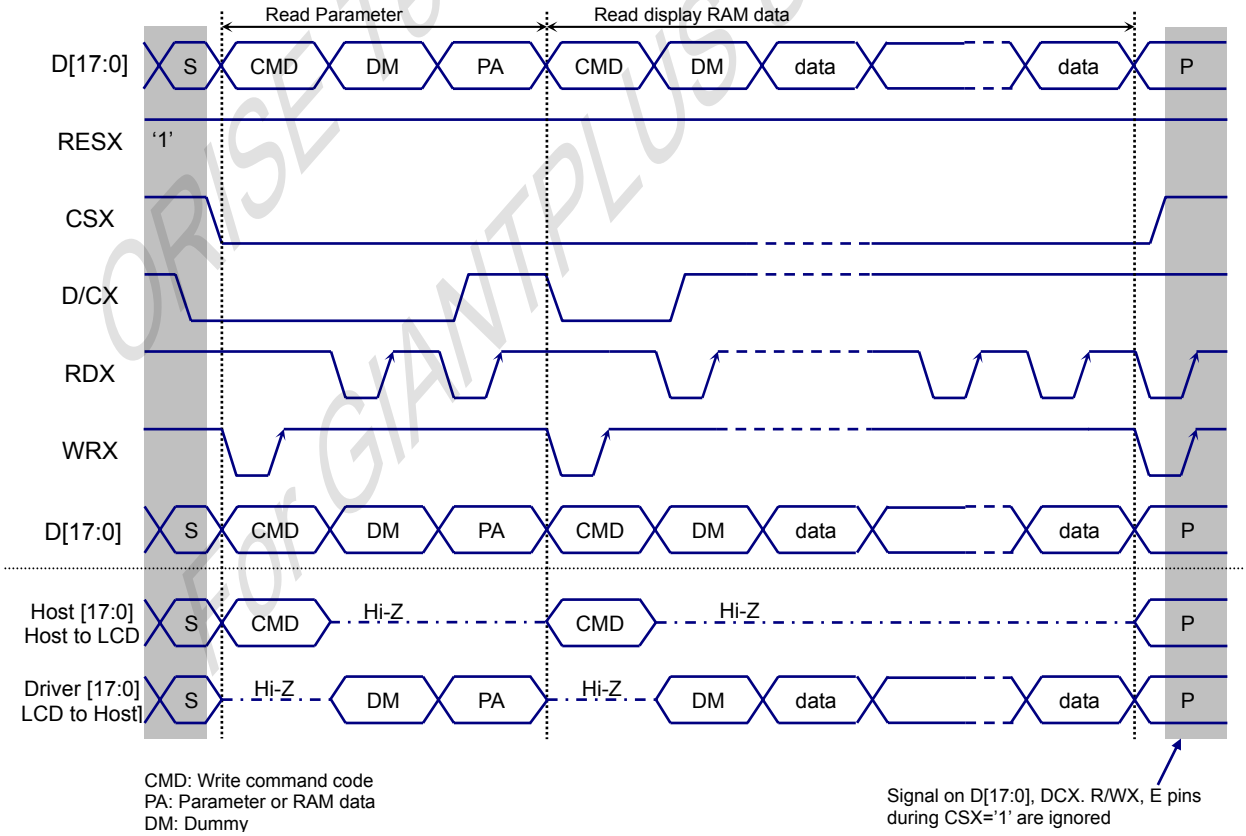

Fig. 7.2.2.2.2 8080-Series parallel bus protocol, Read data from register or display RAM

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7.2.3. 6800-Series Parallel Interface (P68='1')

The MCU uses a 11-wires 8-data parallel interface or 19-wires 16-data parallel interface or 12-wires 9-data parallel interface or 21-wires 18-data parallel interface. The chip-select CSX(active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. The R/WX is the Read/Write flag and D[17:0] is parallel data.

The Graphics Controller Chip reads the data at the falling edge of E signal when R/WX='1' and Writes the data at the falling of the E signal when R/WX='0'. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits are display RAM data or command parameters. When D/C='0', D[17:0] bits are commands.

The 6800-series bi-directional interface can be used for communication between the micro controller and LCD driver chip. The selection of this interface is done when P68 pin is high state (VDDIO). Interface bus width can be selected with IM2, IM1 and IM0.

The interface functions of 6800-series parallel interface are given in Table 7.2.3.

Table 7.2.3 The function of 6800-series parallel interface

P68	IM2	IM1	IM0	Interface	D/CX	R/WX	E	Function
1	1	0	0	8-bits Parallel	0	0	↓	Write 8-bits command (D7 to D0)
					1	0	↓	Write 8-bits display data or 8-bits parameter (D7 to D0)
					1	1	↓	Read 8-bits command (D7 to D0)
					1	1	↓	Read 8-bits parameter or status (D7 to D0)
1	1	0	1	16-bits Parallel	0	0	↓	Write 8-bits command (D7 to D0)
					1	0	↓	Write 16-bits display data (D15 to D0) or 8-bits parameter (D7 to D0)
					1	1	↓	Read 8-bits command (D7 to D0)
					1	1	↓	Read 8-bits parameter or status (D7 to D0)
1	1	1	0	9-bits Parallel	0	0	↓	Write 8-bits command (D7 to D0)
					1	0	↓	Write 9-bits display data (D8 to D0) or 8-bits parameter (D7 to D0)
					1	1	↓	Read 8-bits command (D7 to D0)
					1	1	↓	Read 8-bits parameter or status (D7 to D0)
1	1	1	1	18-bits Parallel	0	0	↓	Write 8-bits command (D7 to D0)
					1	0	↓	Write 18-bits display data (D17 to D0) or 8-bits parameter (D7 to D0)
					1	1	↓	Read 8-bits command (D7 to D0)
					1	1	↓	Read 8-bits parameter or status (D7 to D0)

7.2.3.1 Write cycle sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (E low-high-low sequence) consists of 3 control (D/CX, E, R/WX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data (='1').

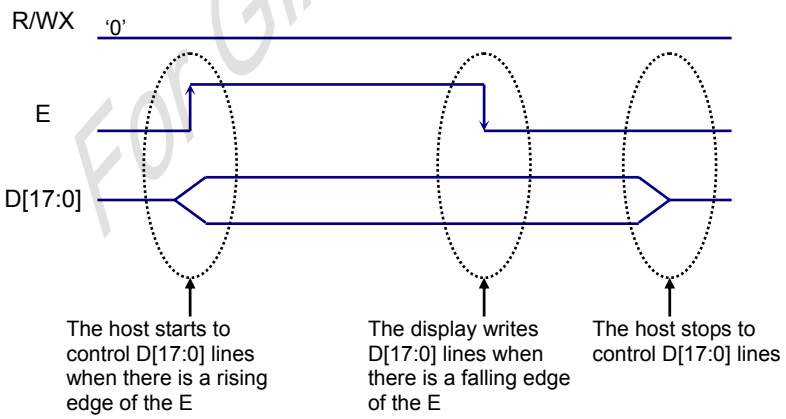

Fig. 7.2.3.1.1 6800-Series Write Protocol

Note: E is an unsynchronized signal (It can be stopped)

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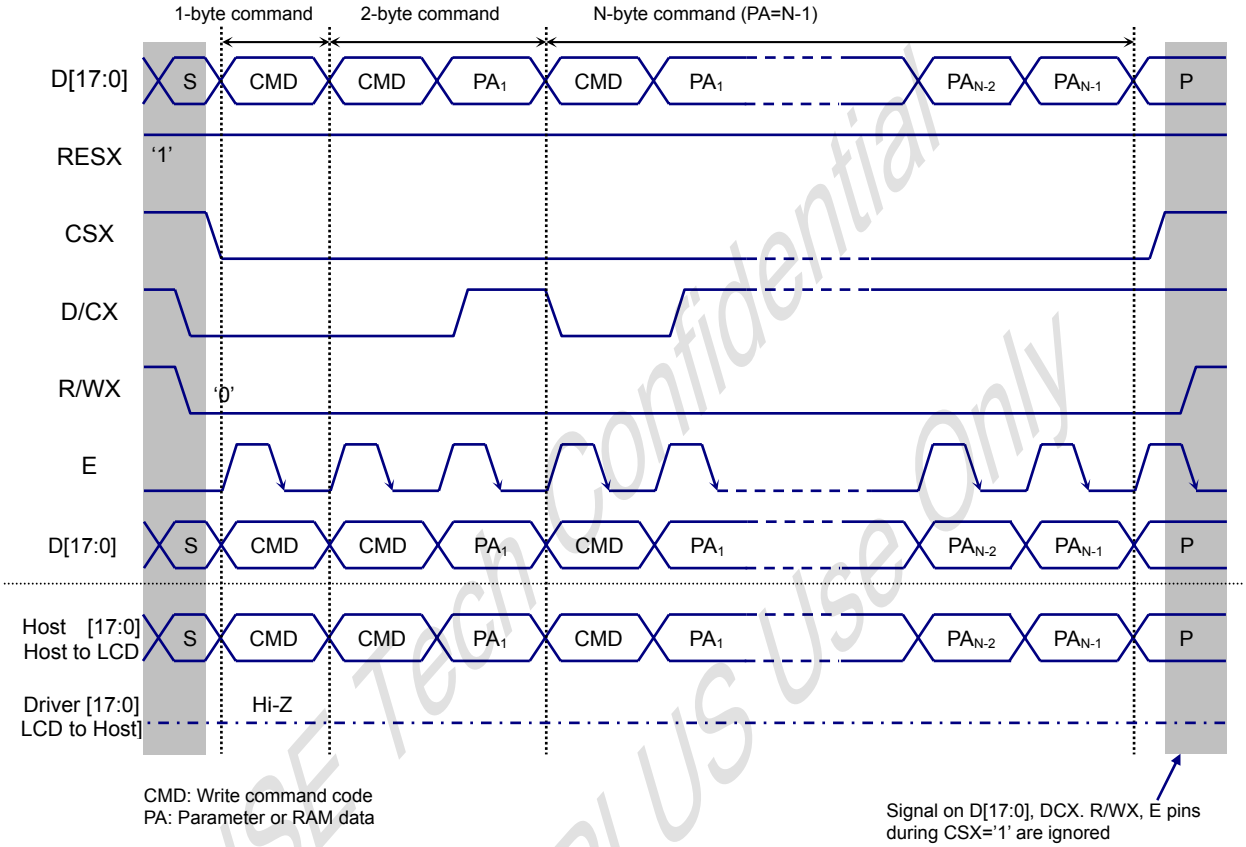

Fig. 7.2.3.1.2 6800-Series parallel bus protocol, Write to register or display RAM

7.2.3.2 Read cycle sequence

The read cycle means that the host reads information (command or/and data) to the display via the interface. Each read cycle (E low-high-low sequence) consists of 3 control (D/CX, E, R/WX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data (='1').

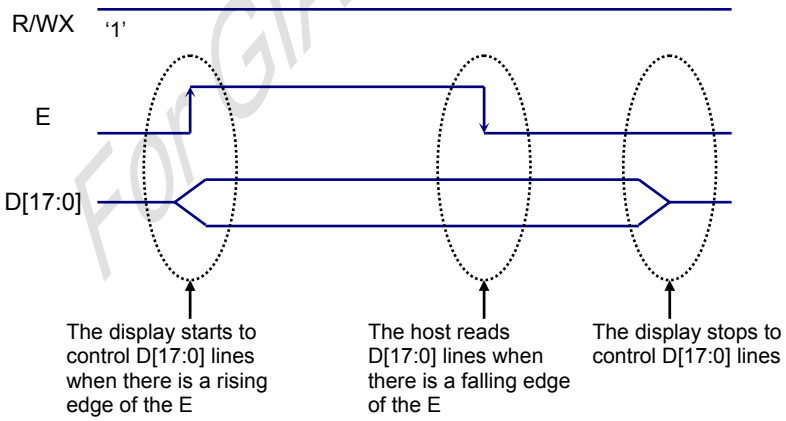

Fig. 7.2.3.2.1 6800-Series Read Protocol

Note: E is an unsynchronized signal (It can be stopped)

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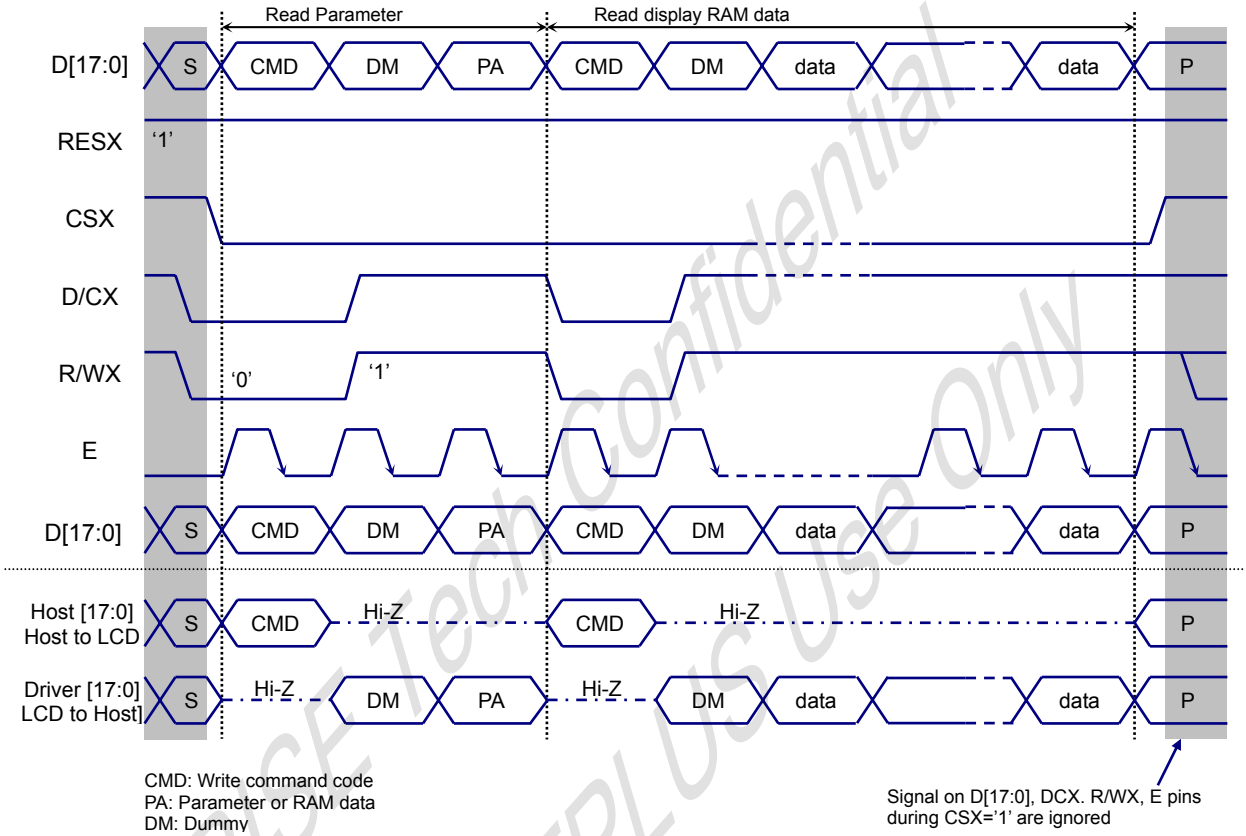

Fig. 7.2.3.2.2 6800-Series parallel bus protocol, Read data from register or display RAM

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7.2.4. Serial Peripheral interface

7.2.4.1 3-pin 9-bits SPI

The selection of this interface is done by IM2 and SPI4. See the Table 7.2.4.1.

The serial interface is a 3-pin 9-bits bi-directional interface for communication between the micro controller and the LCD driver chip. The 3-pin serial use: CSX (chip enable), SCL (serial clock) and SDA (serial data input/output). Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

Table 7.2.4.1 Serial Interface Type Selection

SPI4	P68	IM2	IM1	IM0	Interface	Read back selection
0	'-'	0	'-'	'-'	3-Pin Serial interface	Via the read instruction (8-bits, 24-bits and 32-bits read parameter

7.2.4.1.1 Command Write Mode

The write mode of the interface means the micro controller writes commands and data to the 3-Pin serial data packet contains a control bit D/CX and a transmission byte. If D/CX is low, the transmission byte is interpreted as command byte. If D/CX is high, the transmission byte is stored in the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to the DRIVER. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

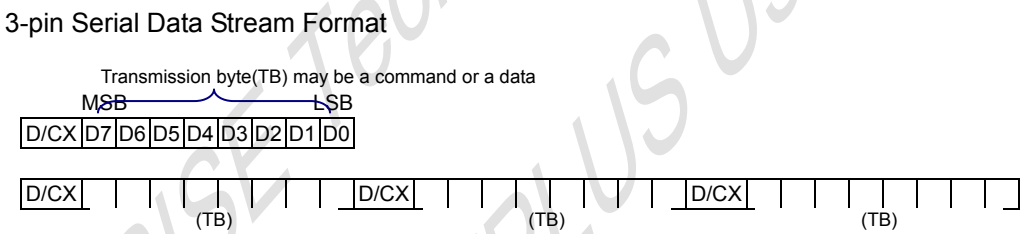

Fig. 7.2.4.1.1 Serial interface data Stream format

When CSX is high, SCL clock is ignored. During the high time of CSX the serial interface is initialized. At the falling edge of CSX, SCL can be high or low. SDA is sampled at the rising edge of CSX. D/CX indicates, whether the byte is command code (D/CX='0') or parameter/RAM data (D/CX='1'). It is sampled when first rising edge of CSX. If CSX stay low after the last bit of command/data byte, the serial interface expects the D/CX bit of the next byte at the next rising edge of SCL.

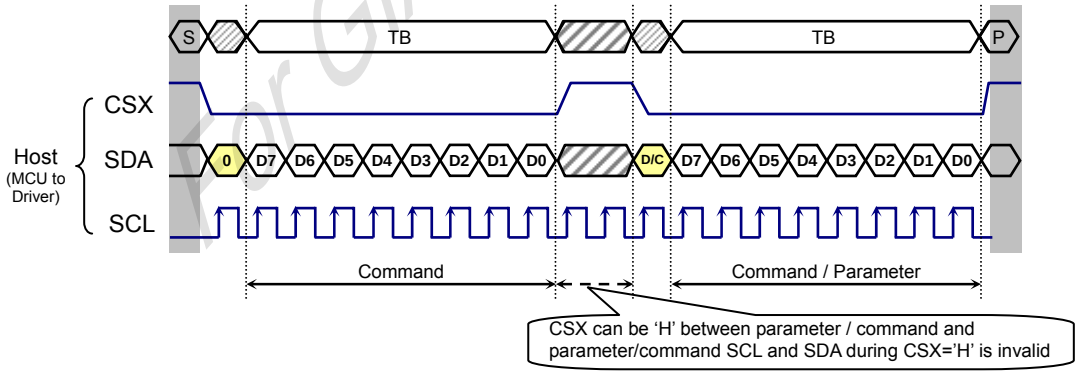

Fig. 7.2.4.1.2 Serial interface Write protocol (Write to register with control bit in transmission)

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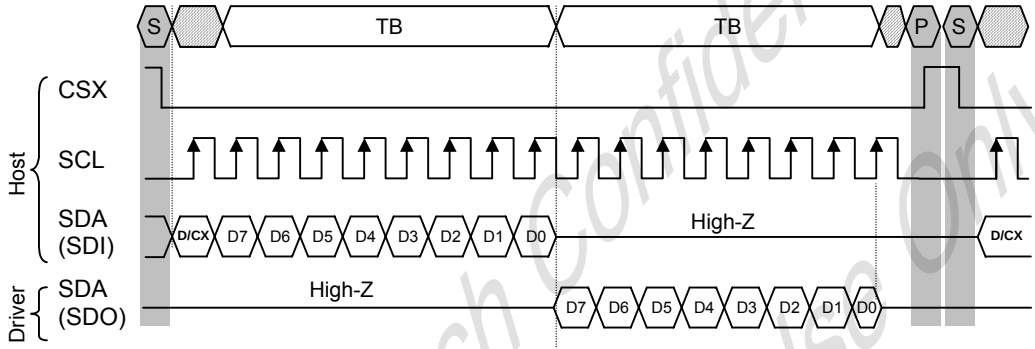
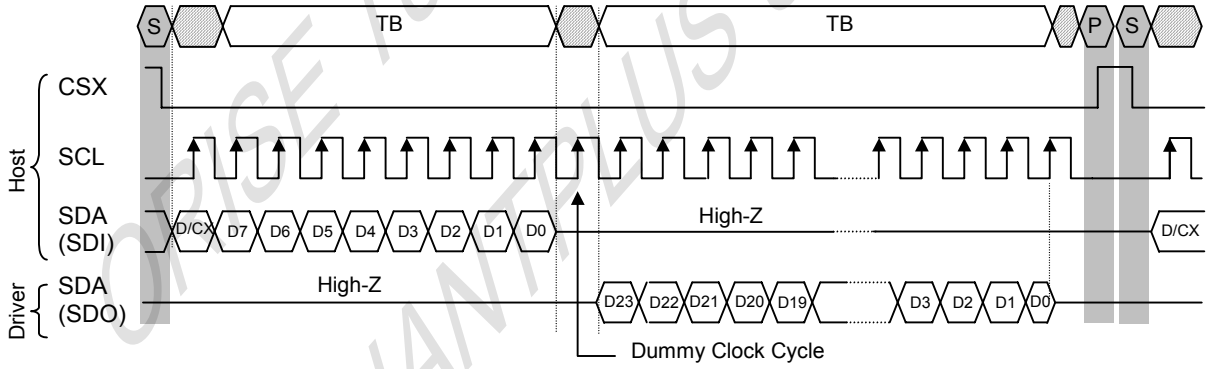
7.2.4.1.2 Read Functions

The read mode of the interface means that the micro controller reads register value from the Driver. To do the micro controller first has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. After the read status command has been sent, the SDA lin must be set to tri-state no later than at the falling edge of SCL of the last bit.

3-Pin Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



3-Pin Serial Protocol (for RDDID command: 24-bit read)



3-Pin Serial Protocol (for RDDST command: 32-bit read)

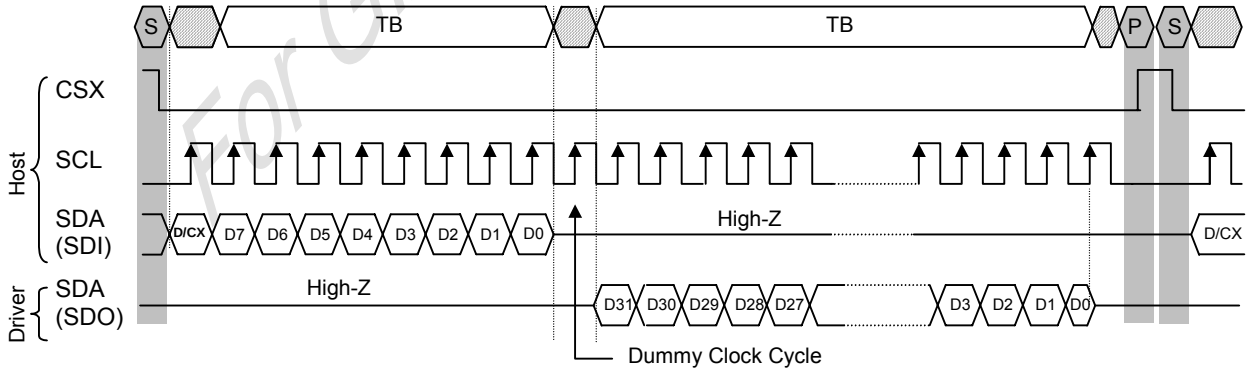


Fig. 7.2.4.1.2 3-pin Serial interface Read protocol

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7.2.4.2 4-pin 8-bits SPI

The selection of this interface is done by IM2 and SPI4. See the Table 7.2.4.2.

The serial interface is a 4-pin 8-bits bi-directional interface for communication between the micro controller and the LCD driver chip. The 4-pin serial use: CSX (chip enable), SCL (serial clock), DCX(command or data) and SDA (serial data input/output). Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

Table 7.2.4.2 Serial Interface Type Selection

SPI4	P68	IM2	IM1	IM0	Interface	Read back selection
1	'-'	0	'-'	'-'	4-Pin Serial interface	Via the read instruction (8-bits, 24-bits and 32-bits read parameter

7.2.4.2.1 Command Write Mode

The write mode of the interface means the micro controller writes commands and data to the 4-Pin serial data packet. If D/CX is low, the transmission byte is interpreted as command byte. If D/CX is high, the transmission byte is stored in the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to the DRIVER. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

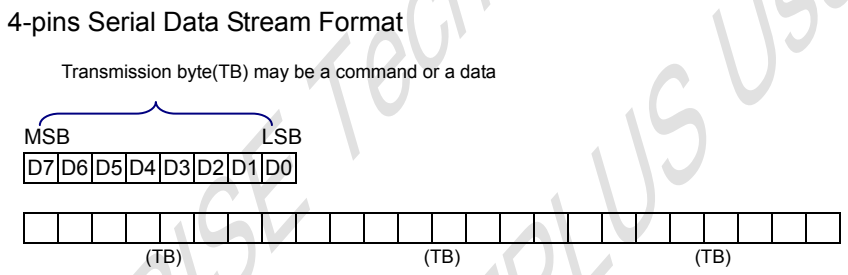

Fig. 7.2.4.2.1 Serial interface data Stream format

When CSX is high, SCL clock is ignored. During the high time of CSX the serial interface is initialized. At the falling edge of CSX, SCL can be high or low. SDA is sampled at the rising edge of CSX. D/CX indicates, whether the byte is command code (D/CX='0') or parameter/RAM data (D/CX='1'). It is sampled when first rising edge of CSX. If CSX stay low after the last bit of command/data byte, the serial interface expects the D/CX bit of the next byte at the next rising edge of SCL.

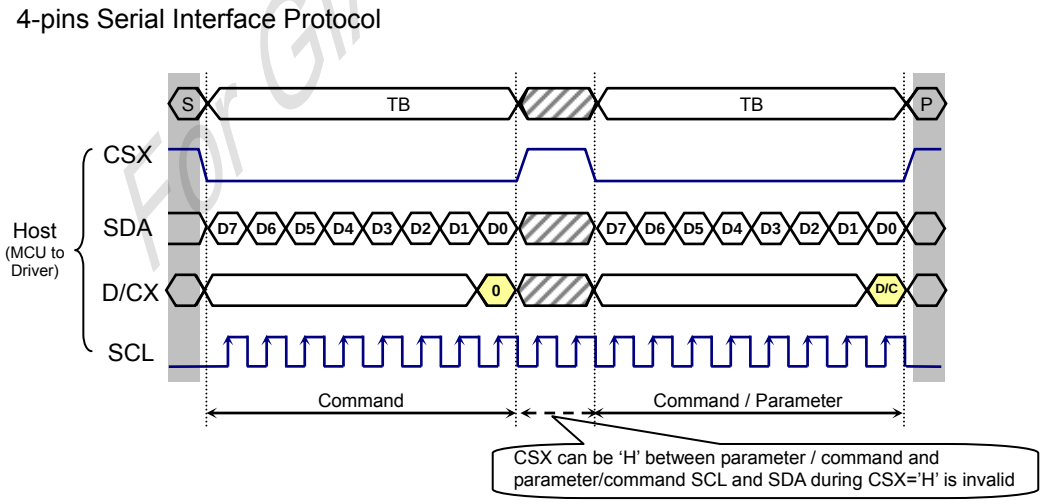

Fig. 7.2.4.2.2 4-pins Serial interface Write protocol (Write to register with control bit in

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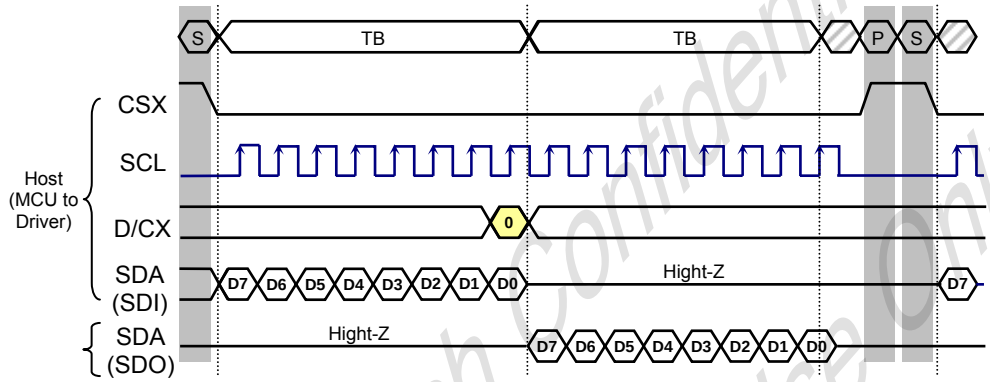
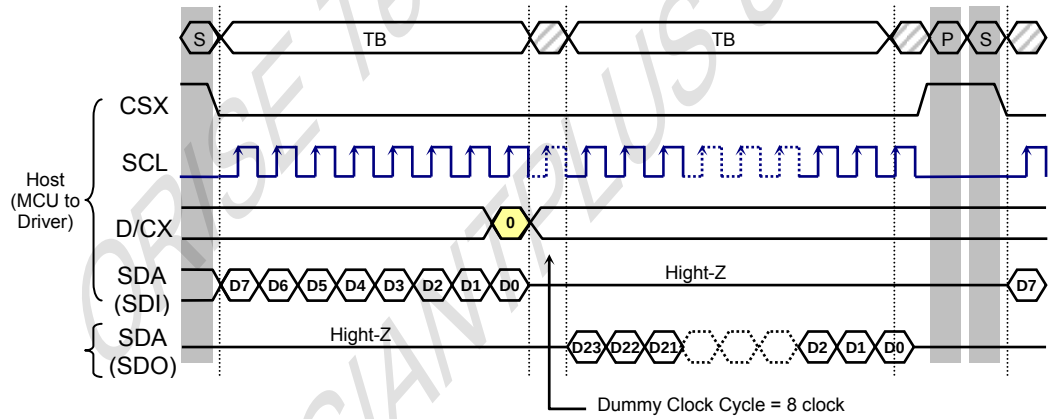
7.2.4.2.2 Read Functions

The read mode of the interface means that the micro controller reads register value from the Driver. To do the micro controller first has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. After the read status command has been sent, the SDA lin must be set to tri-state no later than at the falling edge of SCL of the last bit.

4-pins Serial Protocol (for RDID1/ RDID2/ RDID3/ 0AH/ 0BH/ 0CH/ 0DH/ 0EH/ 0FH command: 8-bits read)



4-pins Serial Protocol (for RDDID command: 24-bits read)



4-pins Serial Protocol (for RDDST command: 32-bits read)

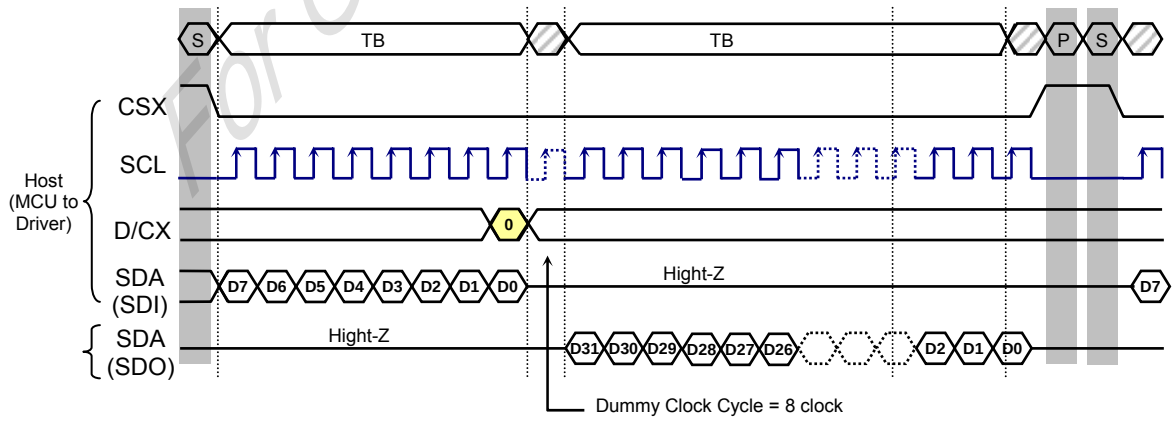


Fig. 7.2.4.2.2 4-pins Serial interface Read protocol

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7.2.5. Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then DRIVER will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been High state. See the following example

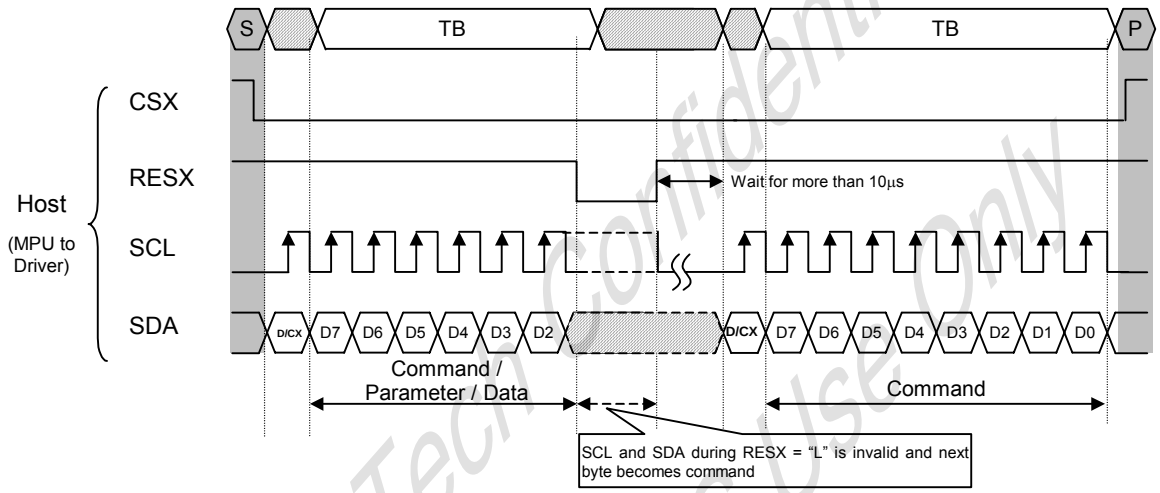

Fig. 7.2.5.1 Serial bus protocol, write mode – interrupted by RESX

If there is a break in data transmission by CSX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then DRIVER will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following example

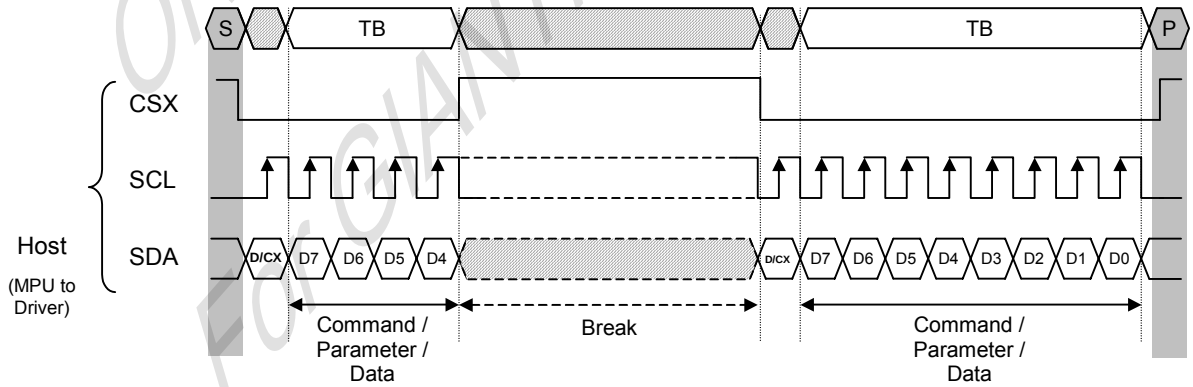

Fig. 7.2. 5.2 Serial bus protocol, write mode – interrupted by CSX

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If 1, 2 or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

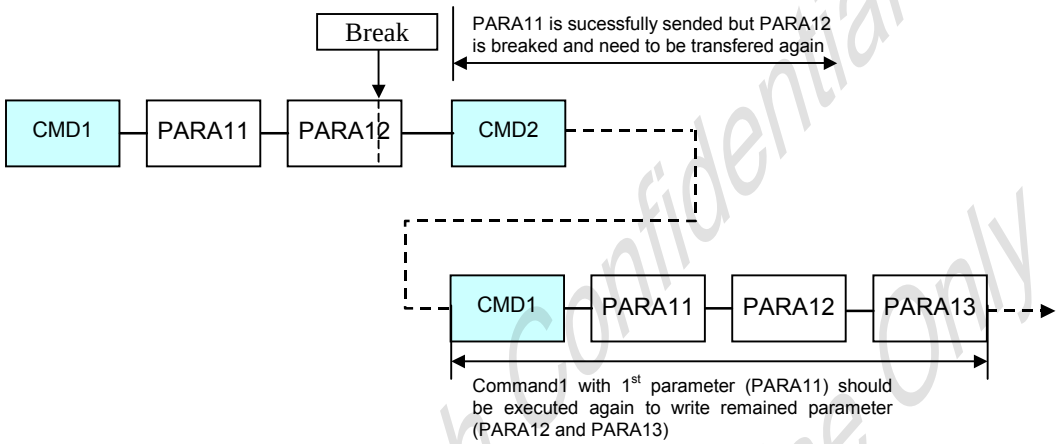

Fig.7.2.5.3 Write interrupts recovery (serial interface)

If a 2 or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.

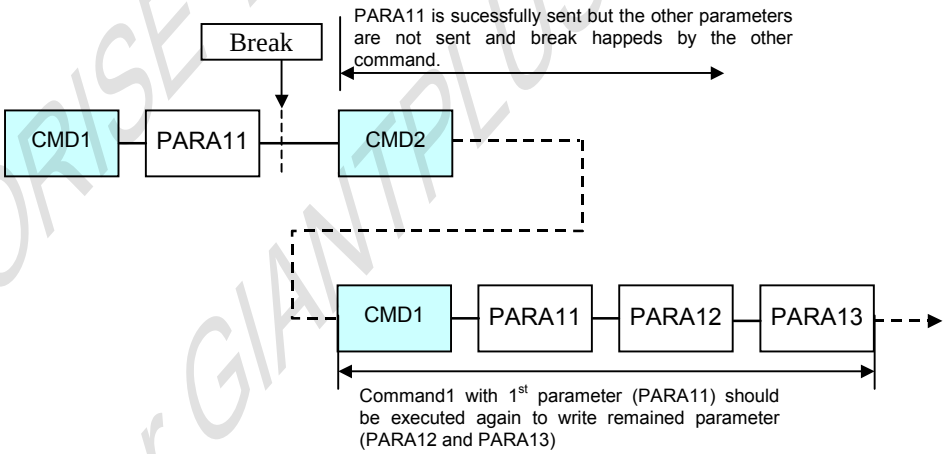

Fig. 7.2.5.4 Write interrupts recovery (both serial and parallel interface)

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7.2.6. Data Transfer Pause

It will be possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then DRIVER will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select Line is released after a whole byte of a command has been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below.

This applies to the following 4 conditions:

1) Command-Pause-Command

2) Command-Pause-Parameter

3) Parameter-Pause-Command

4) Parameter-Pause-Parameter

7.2.6.1 Serial Interface Pause

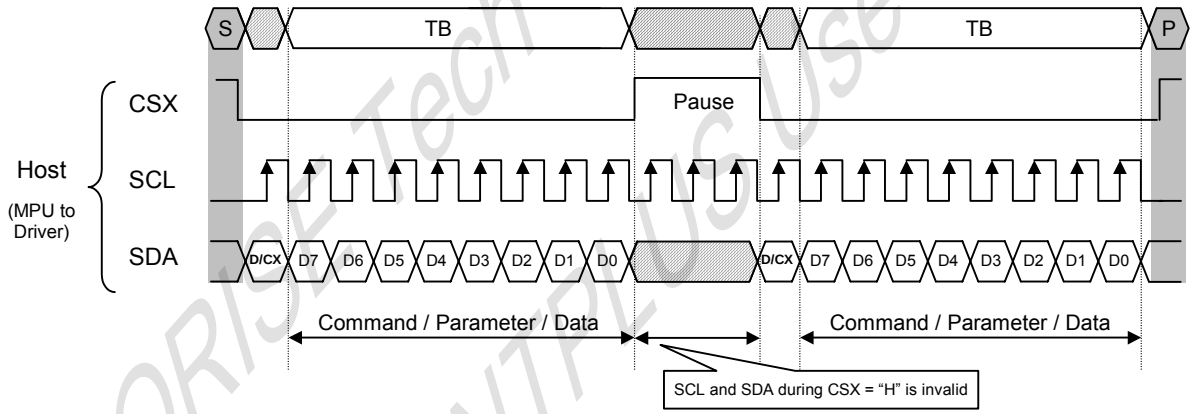

Fig. 7.2.6.1 Serial interface Pause Protocol (pause by CSX)

7.2.6.2 Parallel Interface Pause

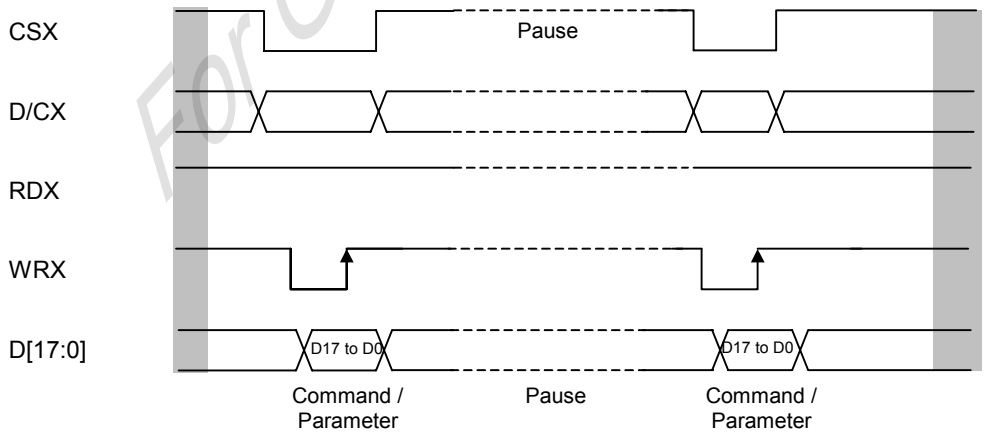

Fig. 7.2.6.2 Parallel bus Pause Protocol (paused by CSX)

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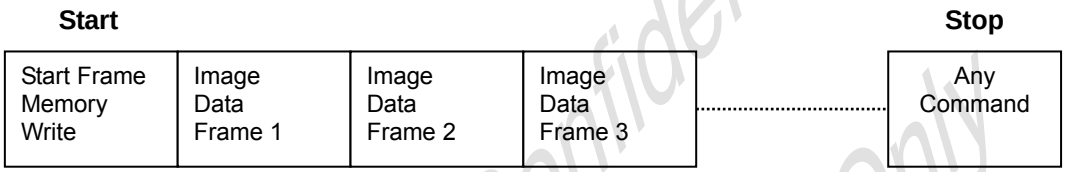
7.2.7. Data Transfer Modes

The Module has three kinds colour modes for transferring data to the display RAM. These are 12-bit colour per pixel, 16-bit colour per pixel and 18-bit colour per pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

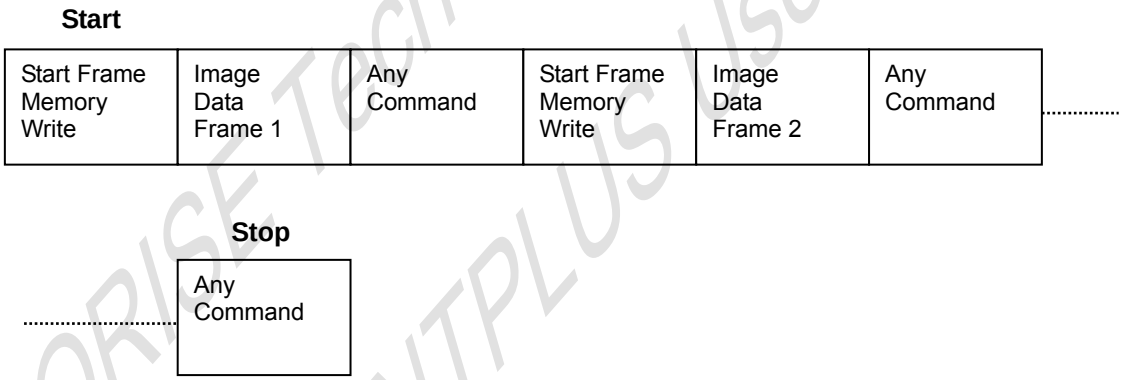
6.2.7.1 Method 1

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.



6.2.7.2 Method 2

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame is downloaded.



Note:

1) These apply to all data transfer Colour modes on both serial and parallel interfaces.

2) The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

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7.3. MCU Data Colour Coding

7.3.1. MCU Data Colour Coding for RAM data ***Write***

- Parallel 8-Bits Bus Interface (IM1, IM0= “00”)

Table 7.3.1.1 8-Bits Parallel Interface Set Table

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	**2CH**
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Colour
03h	x	x	x	x	x	x	x	x	x	x	R3	R2	R1	R0	G3	G2	G1	G0	4K-Colour (2-pixels/ 3-byyes)
	x	x	x	x	x	x	x	x	x	x	B3	B2	B1	B0	R3	R2	R1	R0	
	x	x	x	x	x	x	x	x	x	x	G3	G2	G1	G0	B3	B2	B1	B0	
05h	x	x	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	65K-Colour (1-pixels/ 2-byyes)
	x	x	x	x	x	x	x	x	x	x	G2	G1	G0	B4	B3	B2	B1	B0	
06h	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Colour (1-pixels/ 3byyes)
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

- Parallel 16-Bits Bus Interface (IM1, IM0= “01”)

Table 7.3.1.2 16-Bits Parallel Interface Set Table

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	**2CH**
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Colour
03h	x	x	x	x	x	x	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0	4K-Colour
05h	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	65K-Colour
06h	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	262K-Colour (2-pixels/ 3byyes)
	x	x	B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x	
	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x	

- Parallel 9-Bits Bus Interface (IM1, IM0= “10”)

Table 7.3.1.3 9-Bits Parallel Interface Set Table

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	**2CH**
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Colour
06h	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Colour (1-pixels/ 2bytes)
	x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

- Parallel 18-Bits Bus Interface (IM1, IM0= “11”)

Table 7.3.1.4 18-Bits Parallel Interface Set Table

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	**2CH**
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Colour
03h	x	x	x	x	x	x	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0	**4K-Colour**
05h	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	**65K-Colour**
06h	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	**262K-Colour**

Note: ‘x’ Don’t care, but need to set VDDIO or DGND level.

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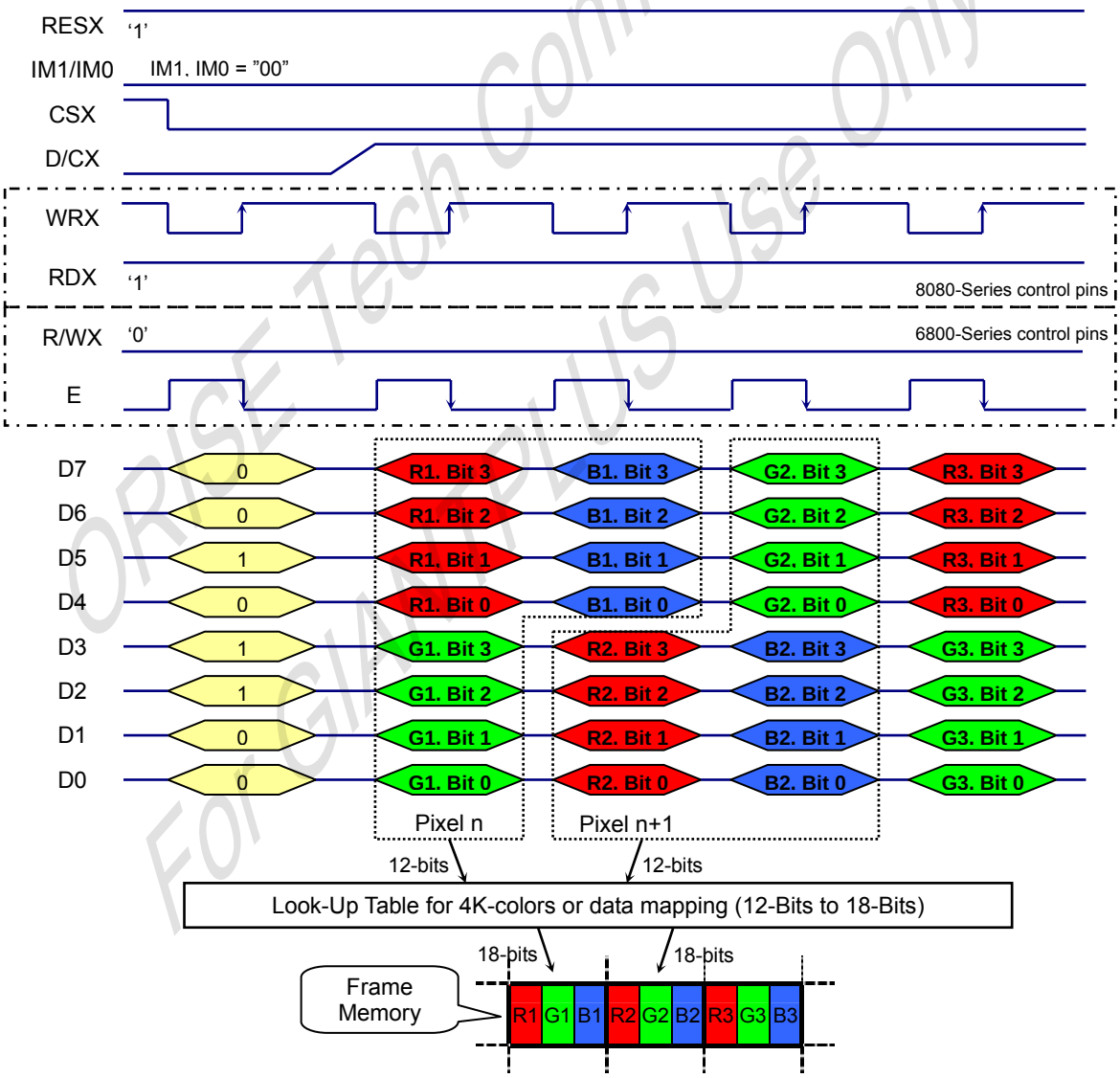
7.3.1.1 Parallel 8-Bits Bus Interface for RAM Data Write (IM1, IM0= "00")

Different display data formats are available for three colours depth supported by listed below.

- 4K-Colours, RGB 4,4,4-bits input data. (3AH="03h")
- 65K-Colours, RGB 5,6,5-bits input data. (3AH="05h")
- 262K-Colours, RGB 6,6,6-bits input data. (3AH="06h")

(1). 8-bits data bus for 12-bits/pixel (RGB 4-4-4-bits input), 4K-colours, 3AH="03h"

There are 2 pixels (6 sub-pixels) per 3-bytes.



Note1. The data order is ad follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

Note 2.3-times transfer is used to transmit 1 pixel data with the 12-bits color depth information.

Note 3. '-' = Don't care - Can be set to VDDIO or DGND level

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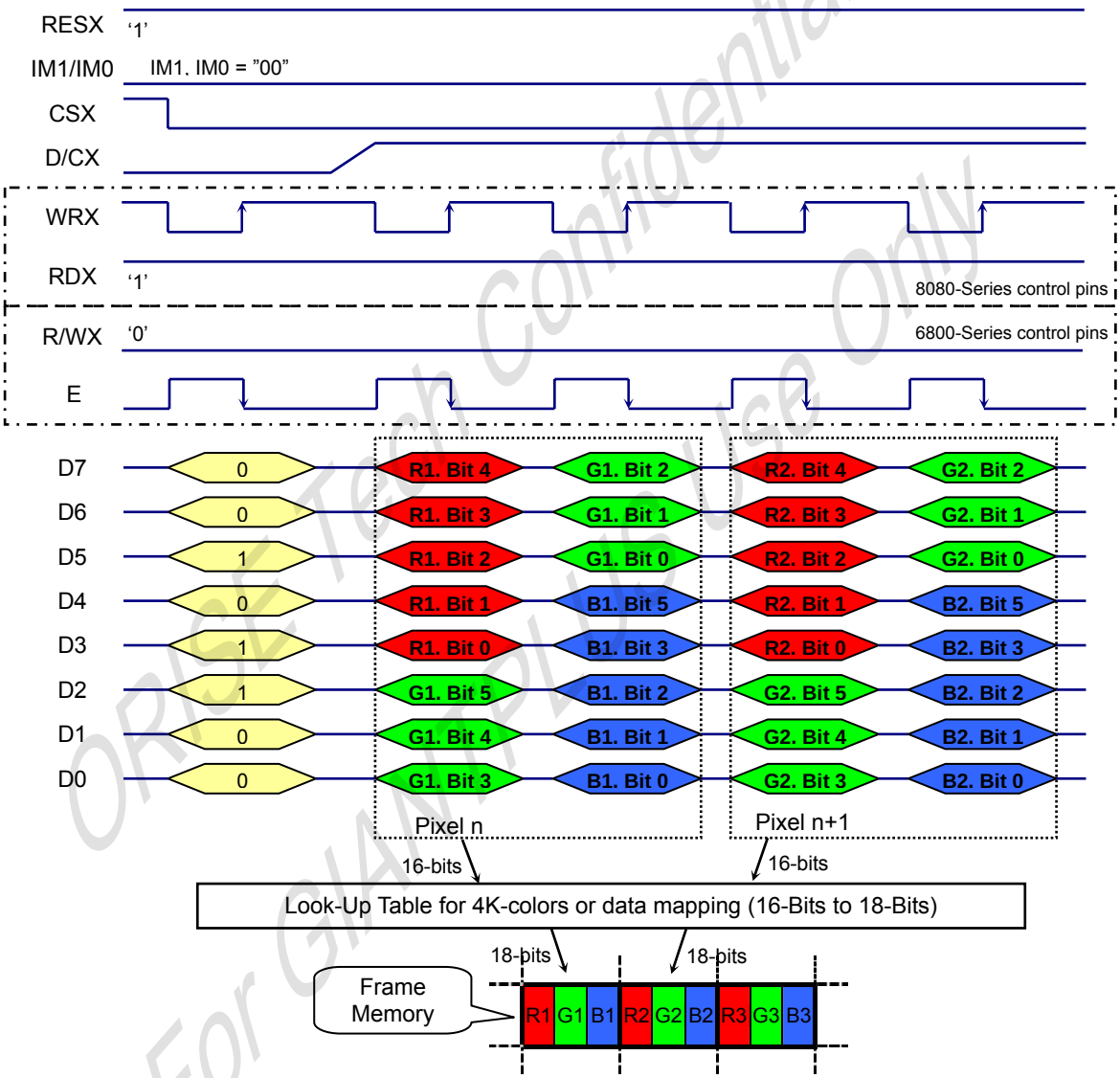
(2). 8-bits data bus for 16-bits/pixel (RGB 5-6-5-bits input), 65K-colours, 3AH="05h"

There are 1 pixels (3 sub-pixels) per 2-bytes.



Note1. The data order is ad follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2.2-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.

Note 3. '-' = Don't care - Can be set to VDDIO or DGND level

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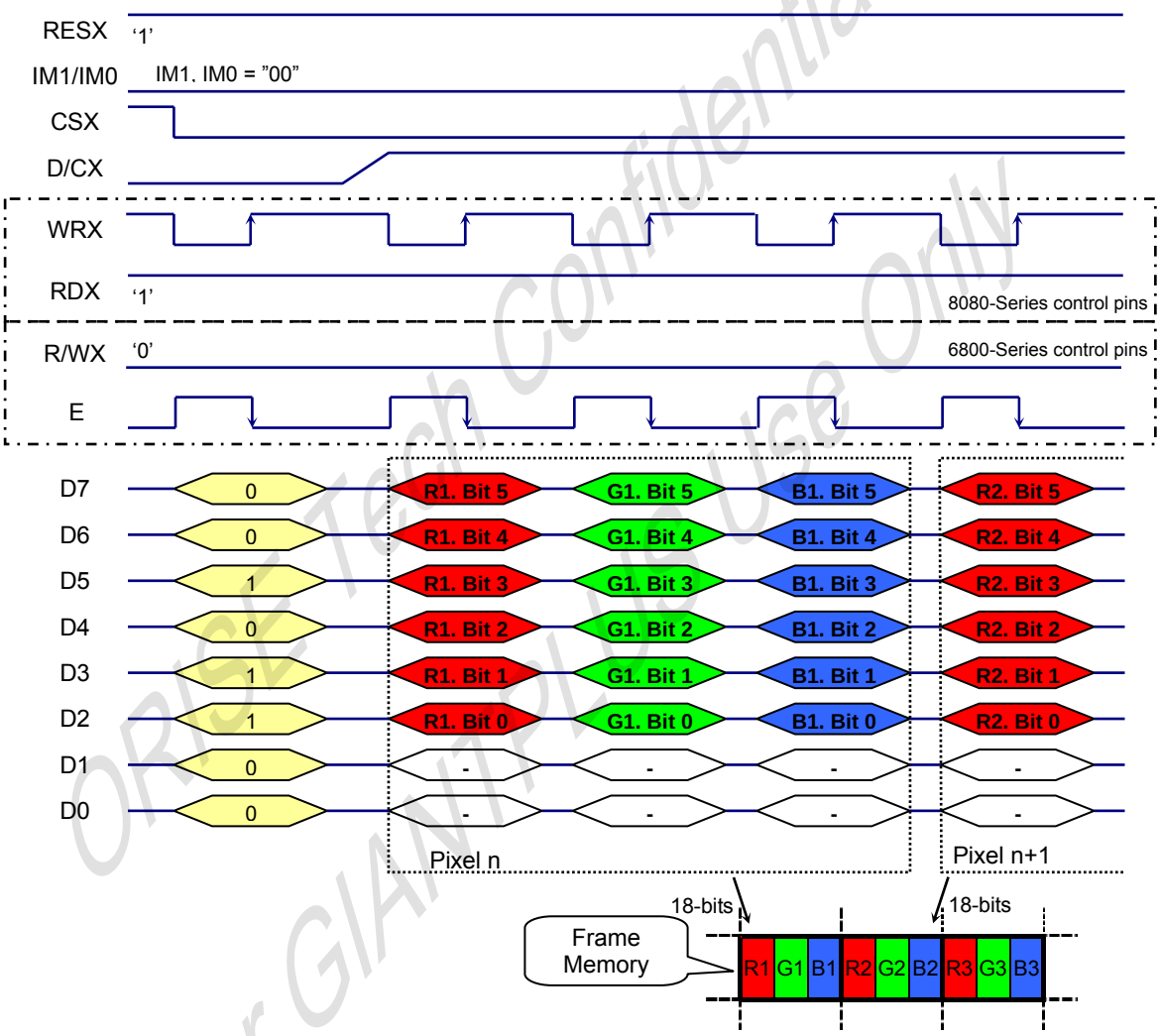
(3). 8-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colours, 3AH="06h"

There are 1 pixels (3 sub-pixels) per 3-bytes.



Note1. The data order is ad follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2.3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Note 3. '-' = Don't care - Can be set to VDDIO or DGND level

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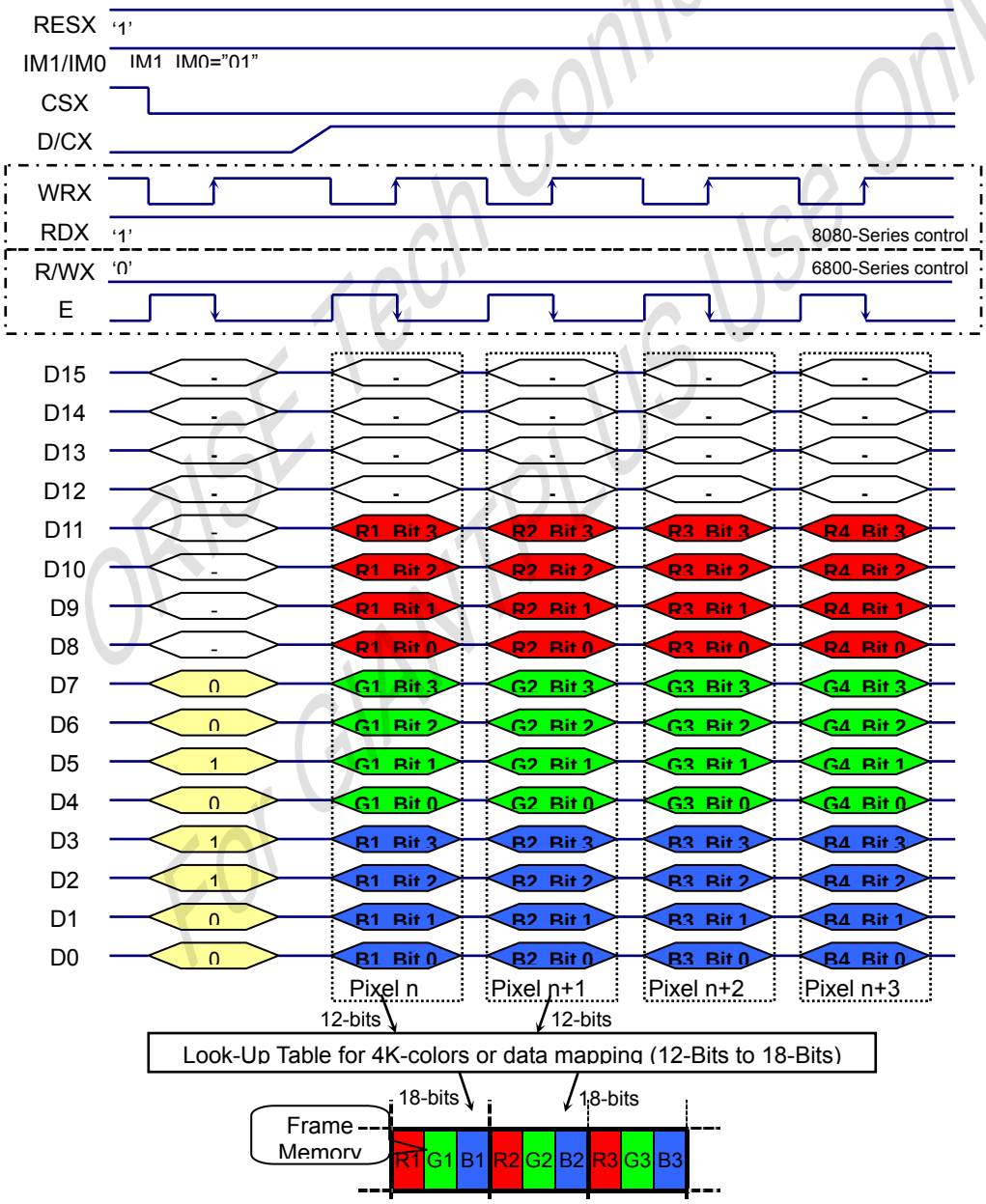
7.3.1.2 Parallel 16-Bits Bus Interface for RAM Data Write (IM1, IM0="01")

Different display data formats are available for three colors depth supported by listed below.

- 4K-Colours, RGB 4,4,4-bits input data. (3AH="03h")
- 65K-Colours, RGB 5,6,5-bits input data. (3AH="05h")
- 262K-Colours, RGB 6,6,6-bits input data. (3AH="06h")

(1). 16-bits data bus for 12-bits/pixel (RGB 4-4-4-bits input), 4K-colours, 3AH="03h"

There are 1 pixel (3 sub-pixels) per 1 bytes



Note1. The data order is ad follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

Note 2.1-times transfer is used to transmit 1 pixel data with the 12-bits color depth information.

Note 3. '-' = Don't care - Can be set to VDDIO or DGND level

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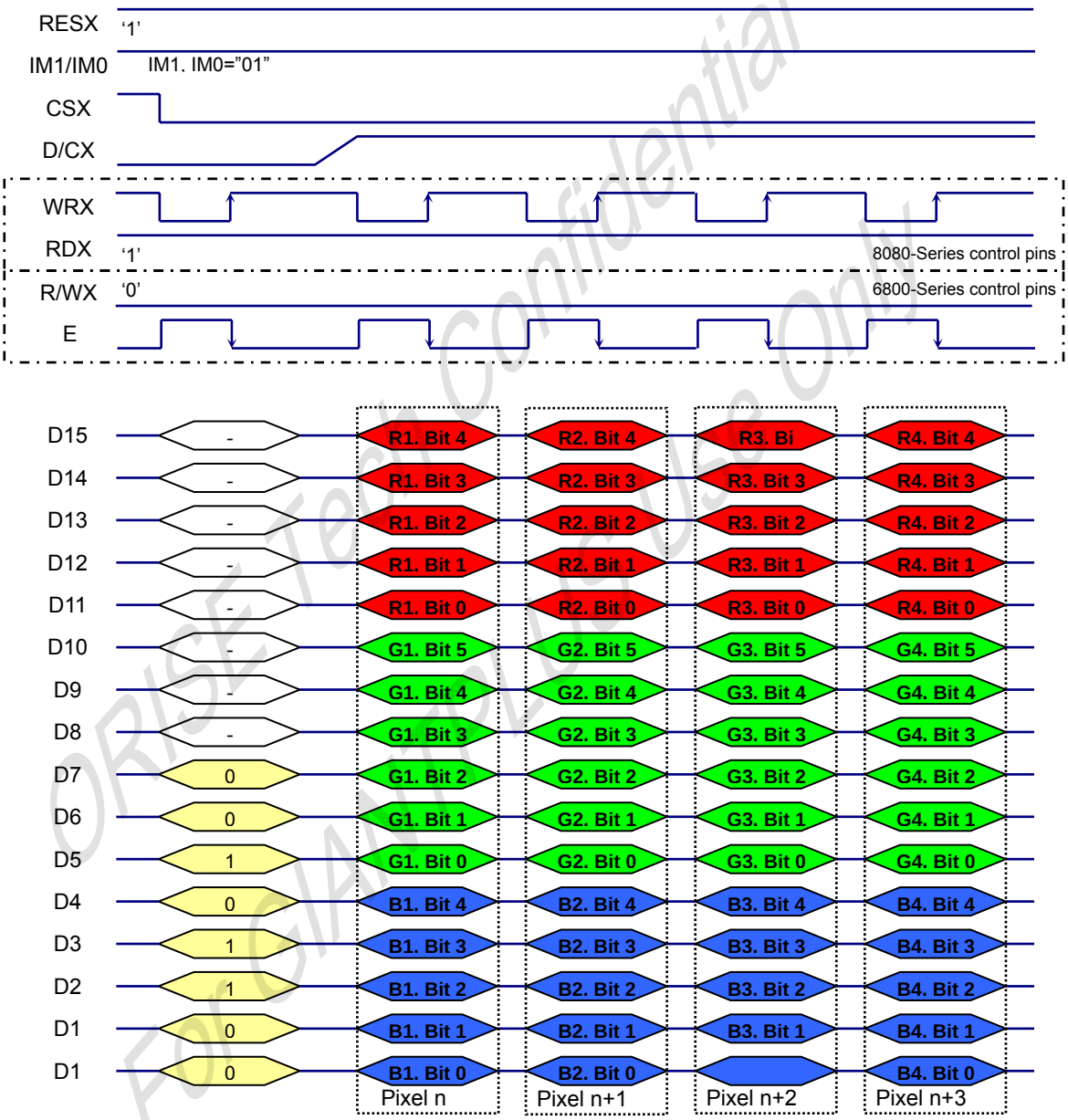
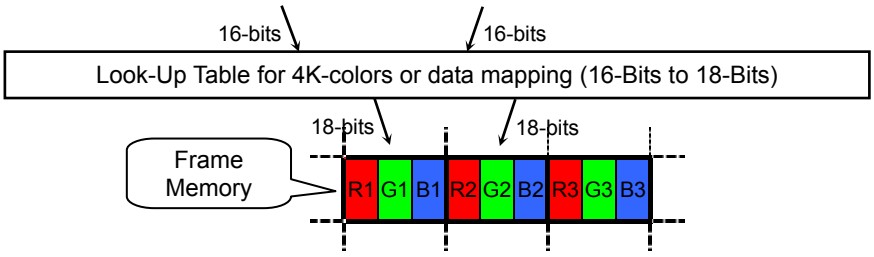
(2). 16-bits data bus for 16-bits/pixel (RGB 5-6-5-bits input), 65K-colours, 3AH="05h"

There are 1 pixel (3 sub-pixels) per 1 bytes





Note1. The data order is ad follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2.1-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.

Note 3. '-' = Don't care - Can be set to VDDIO or DGND level

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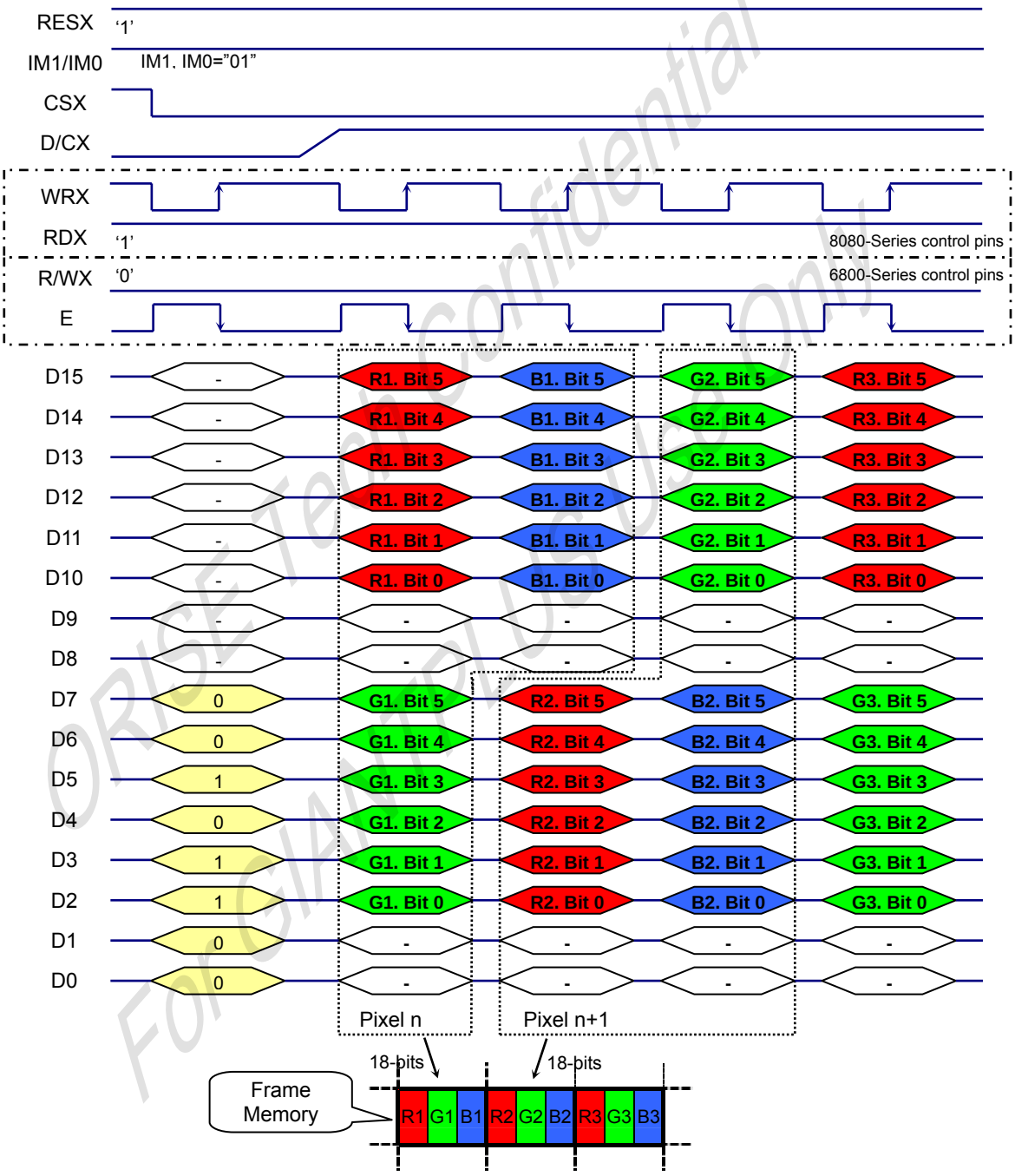
(3). 16-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colours, 3AH="06h"

There are 2 pixel (6 sub-pixels) per 3 bytes



Note1. The data order is ad follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2.3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Note 3. '-' = Don't care - Can be set to VDDIO or DGND level

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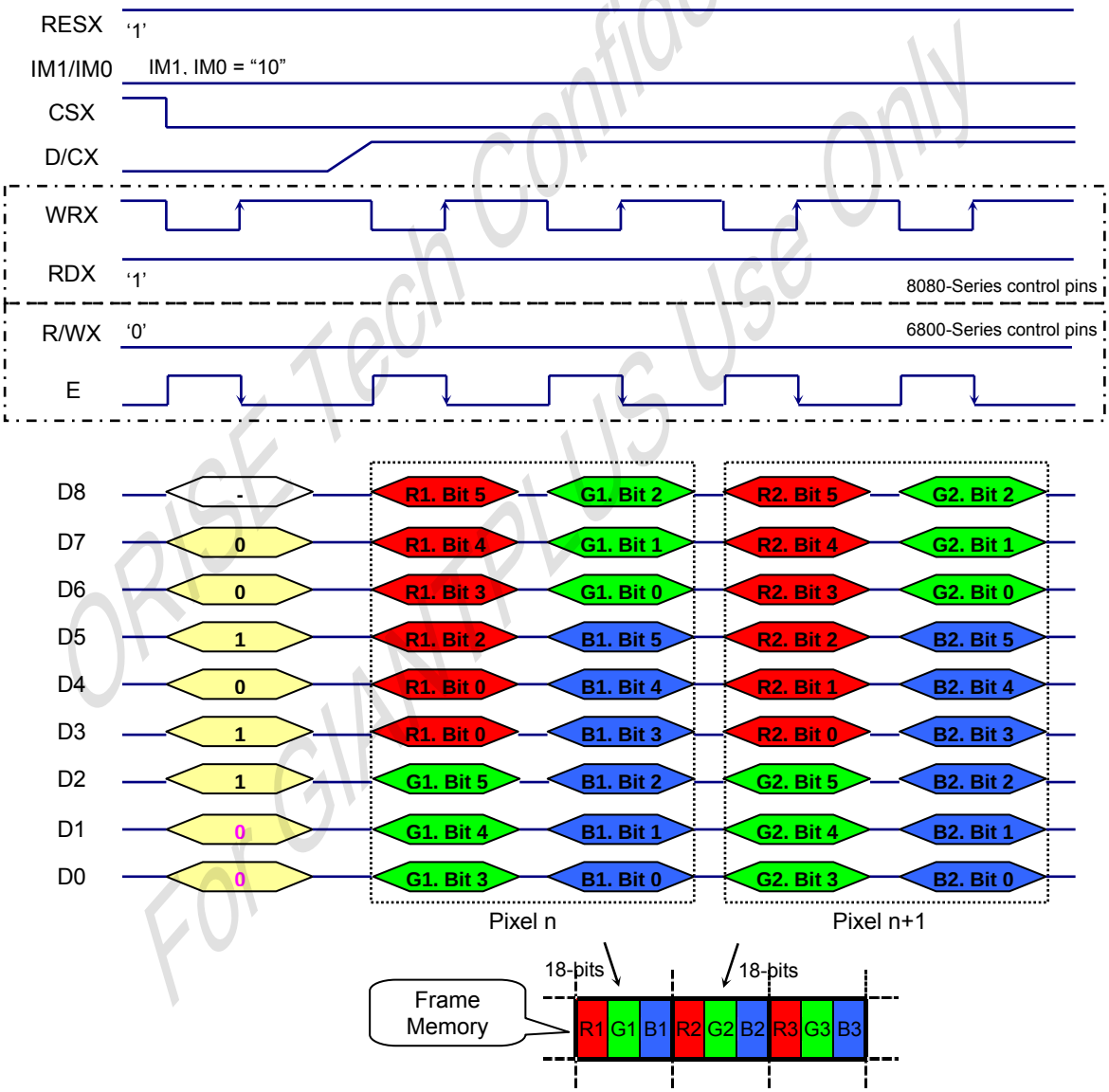
7.3.1.3 Parallel 9-Bits Bus Interface for RAM Data Write (IM1, IM0="10")

Different display data formats are available for three colors depth supported by listed below.

- 262K-Colours, RGB 6,6,6-bits input data. (3AH="06h")

(1). 9-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colours, 3AH="06h"

There is 1 pixel (3 sub-pixels) per 2 bytes



Note1. The data order is ad follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2.3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3. '-' = Don't care - Can be set to VDDIO or DGND level

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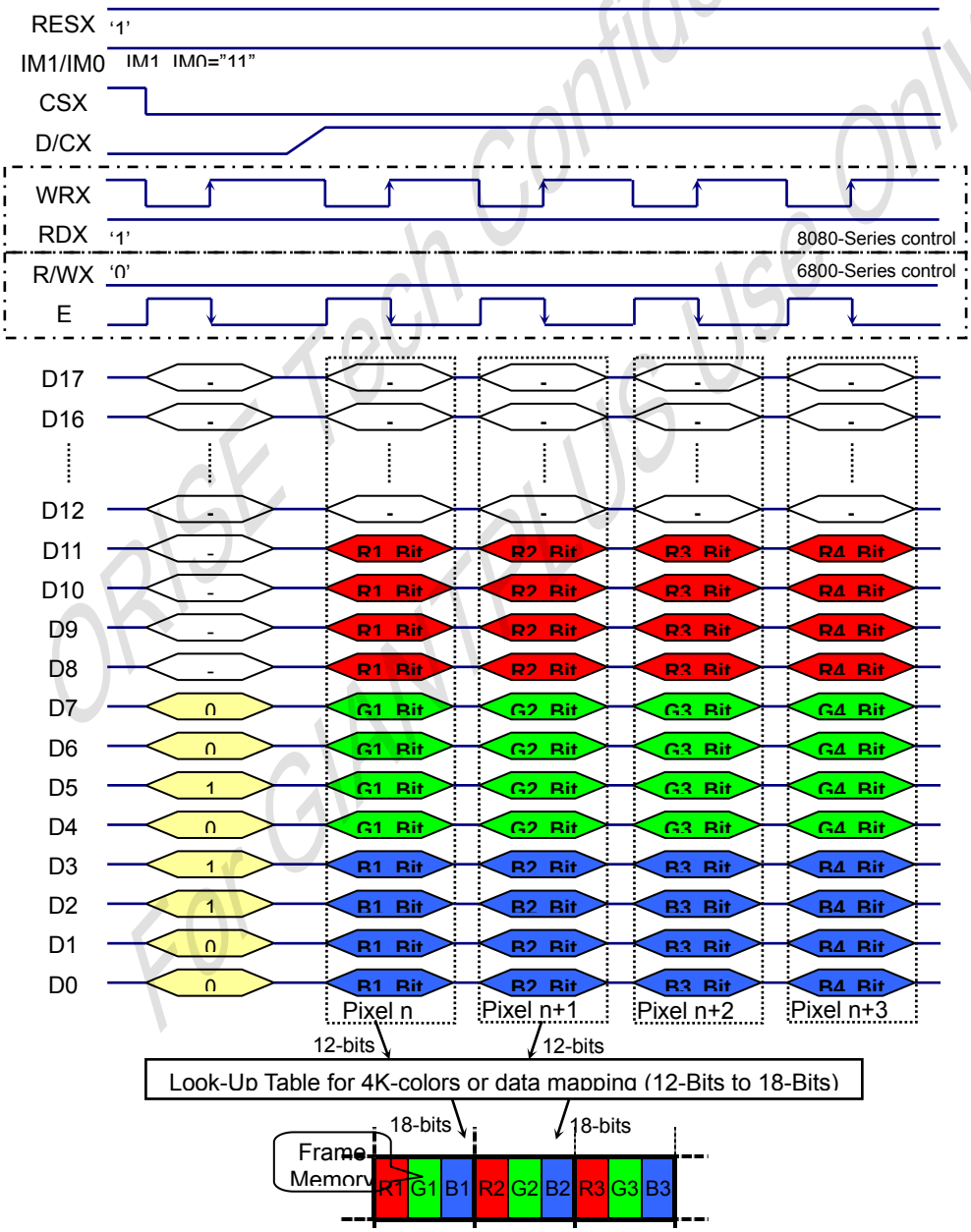
7.3.1.4 Parallel 18-Bits Bus Interface for RAM Data Write (IM1, IM0="11")

Different display data formats are available for three colors depth supported by listed below.

- 4K-Colours, RGB 4,4,4-bits input data. (3AH="03h")
- 65K-Colours, RGB 5,6,5-bits input data. (3AH="05h")
- 262K-Colours, RGB 6,6,6-bits input data. (3AH="06h")

(1). 18-bits data bus for 12-bits/pixel (RGB 4-4-4-bits input), 4K-colours, 3AH="03h"

There is 1 pixel (3 sub-pixels) per 1 bytes



Note1. The data order is ad follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

Note 2.1-times transfer is used to transmit 1 pixel data with the 12-bits color depth information.

Note 3. '-' = Don't care - Can be set to VDDIO or DGND level

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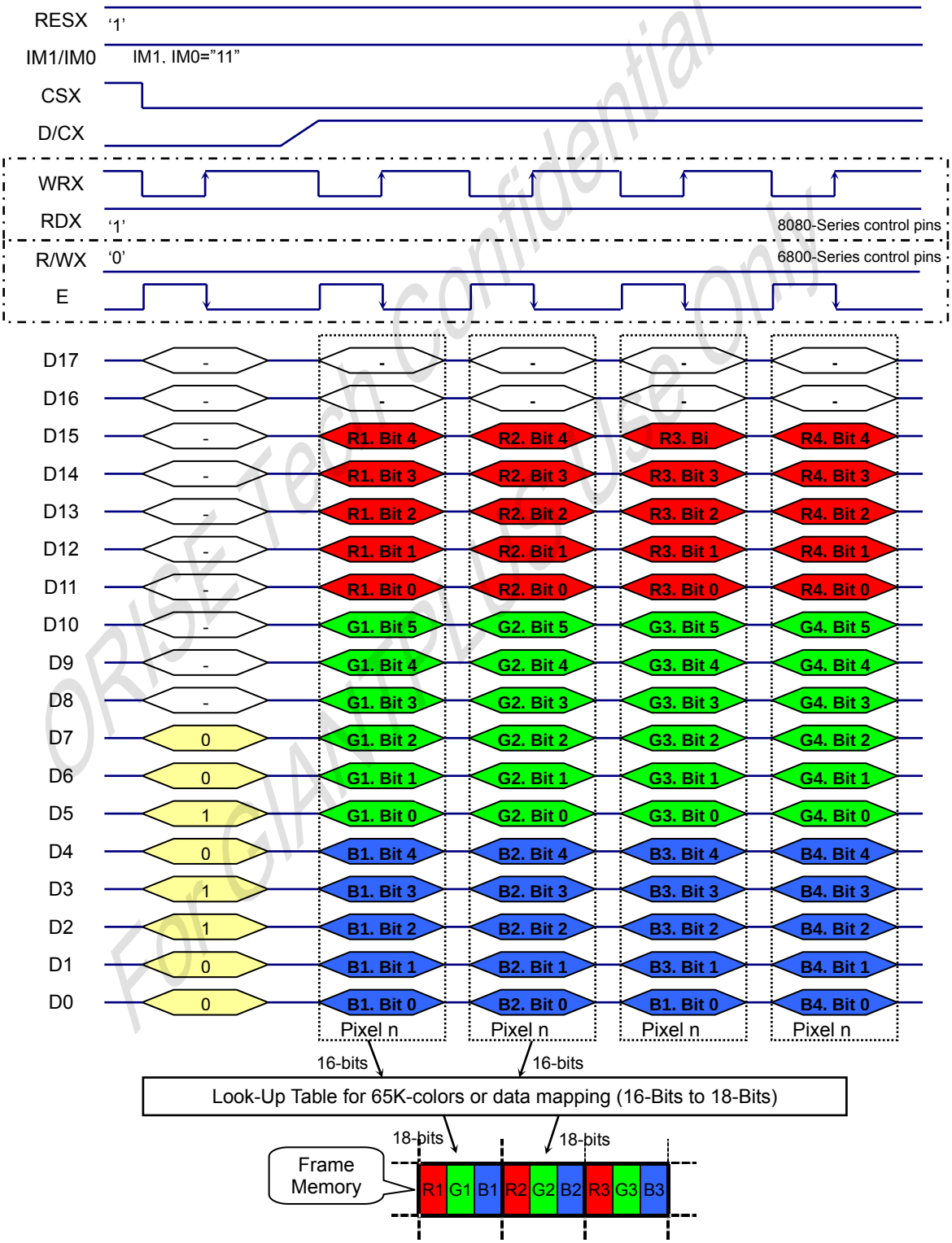
(2). 18-bits data bus for 16-bits/pixel (RGB 5-6-5-bits input), 65K-colours, 3AH="05h"

There are 1 pixel (3 sub-pixels) per 1 bytes



Note1. The data order is ad follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2.1-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.

Note 3. '-' = Don't care - Can be set to VDDIO or DGND level

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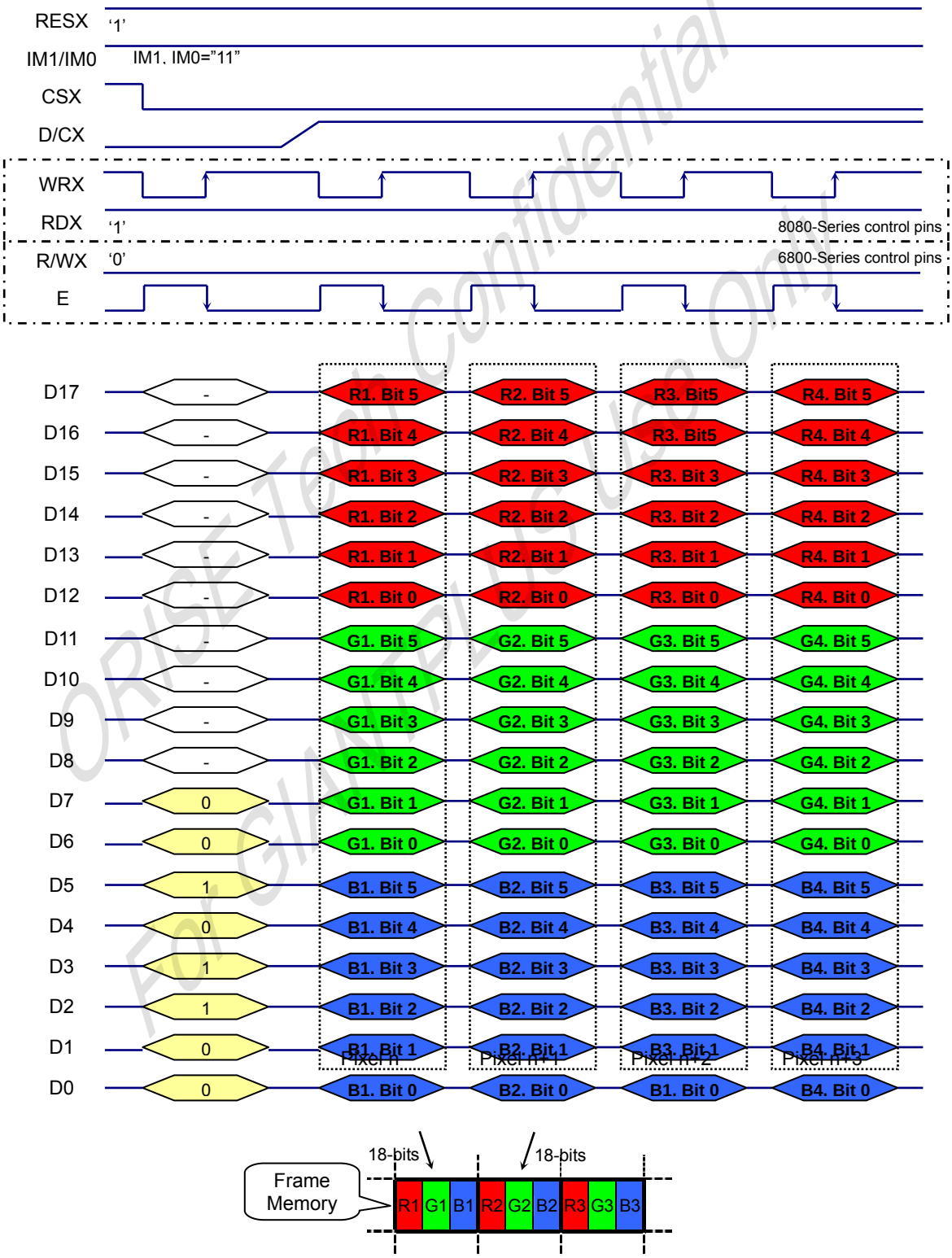
(3). 18-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colours, 3AH="06h"

There are 1 pixel (6 sub-pixels) per 1 bytes



Note1. The data order is ad follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2.1-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Note 3. '-' = Don't care - Can be set to VDDIO or DGND level

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7.3.2. MCU Data Colour Coding for RAM data ***Read***

- Parallel 8-Bits Bus Interface (IM1, IM0= “00”)

Table 7.3.2.1 8-Bits Parallel Interface Set Table

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	**2EH**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Colour
	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Colour (1-pixels/ 3byyes)
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

- Parallel 16-Bits Bus Interface (IM1, IM0= “01”)

Table 7.3.2.2 16-Bits Parallel Interface Set Table

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	**2EH**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Colour
	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	262K-Colour (2-pixels/ 3byyes)
	x	x	B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x	
	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x	

- Parallel 9-Bits Parallel Interface (IM1, IM0= “10”)

Table 7.3.2.3 9-Bits Parallel Interface Set Table

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	**2EH**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Colour
	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Colour (1-pixels/ 2bytes)
	x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

- Parallel 18-Bits Parallel Interface (IM1, IM0= “11”)

Table 7.3.2.4 18-Bits Parallel Interface Set Table

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	**2EH**
Read Data Format	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	**262K-Colour**

Note . ‘x’ Don’t care, but need to set VDDIO or DGND level.

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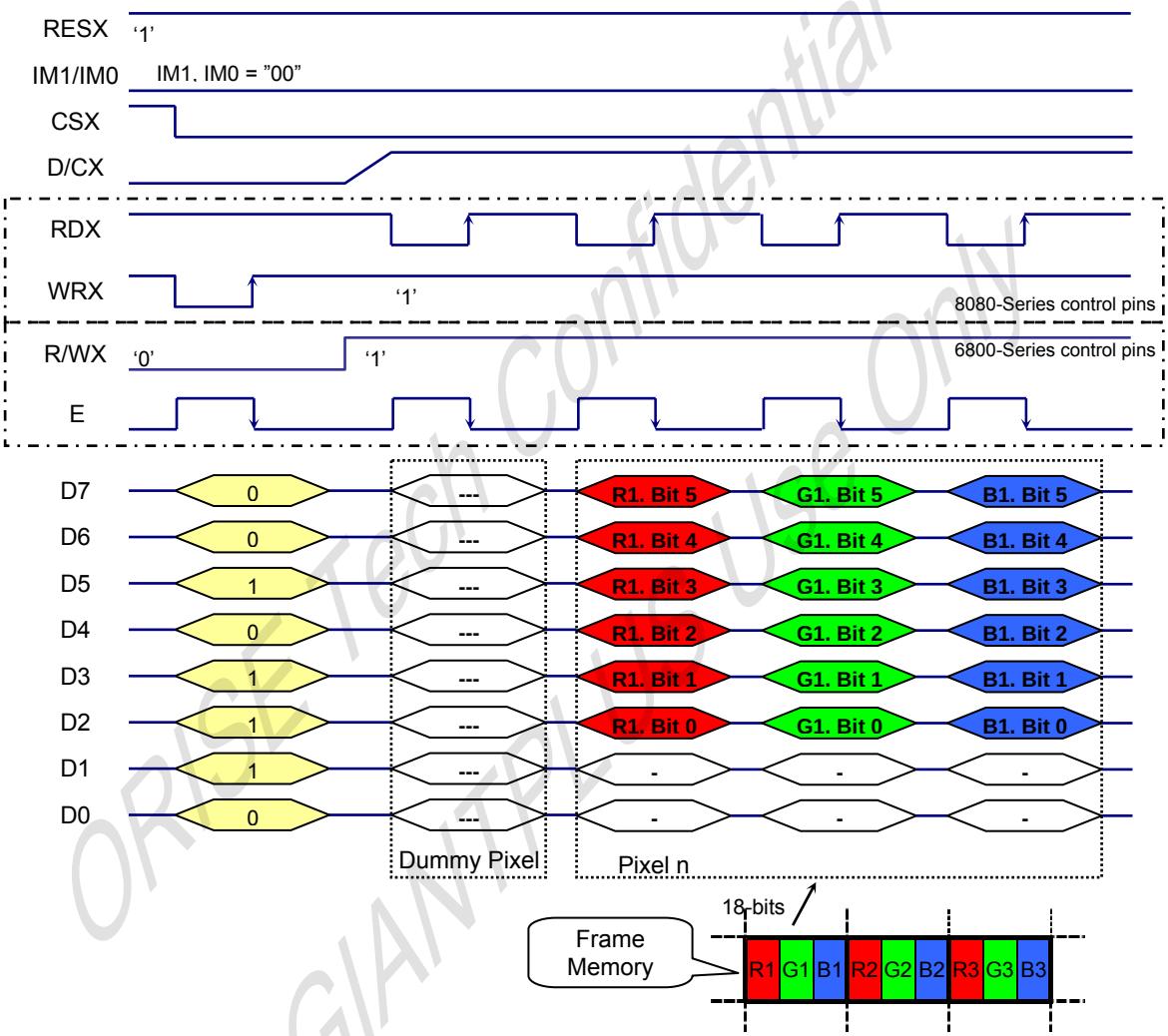
7.3.2.1 Parallel 8-Bits Bus Interface for RAM Data Read (IM1, IM0= "00")

There are 1 pixels (3 sub-pixels) per 3-bytes. (RGB 6-6-6-bits output)



Note1. The data order is ad follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.
Note 2.3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.
Note 3. '-' = Don't care - Can be set to VDDIO or DGND level

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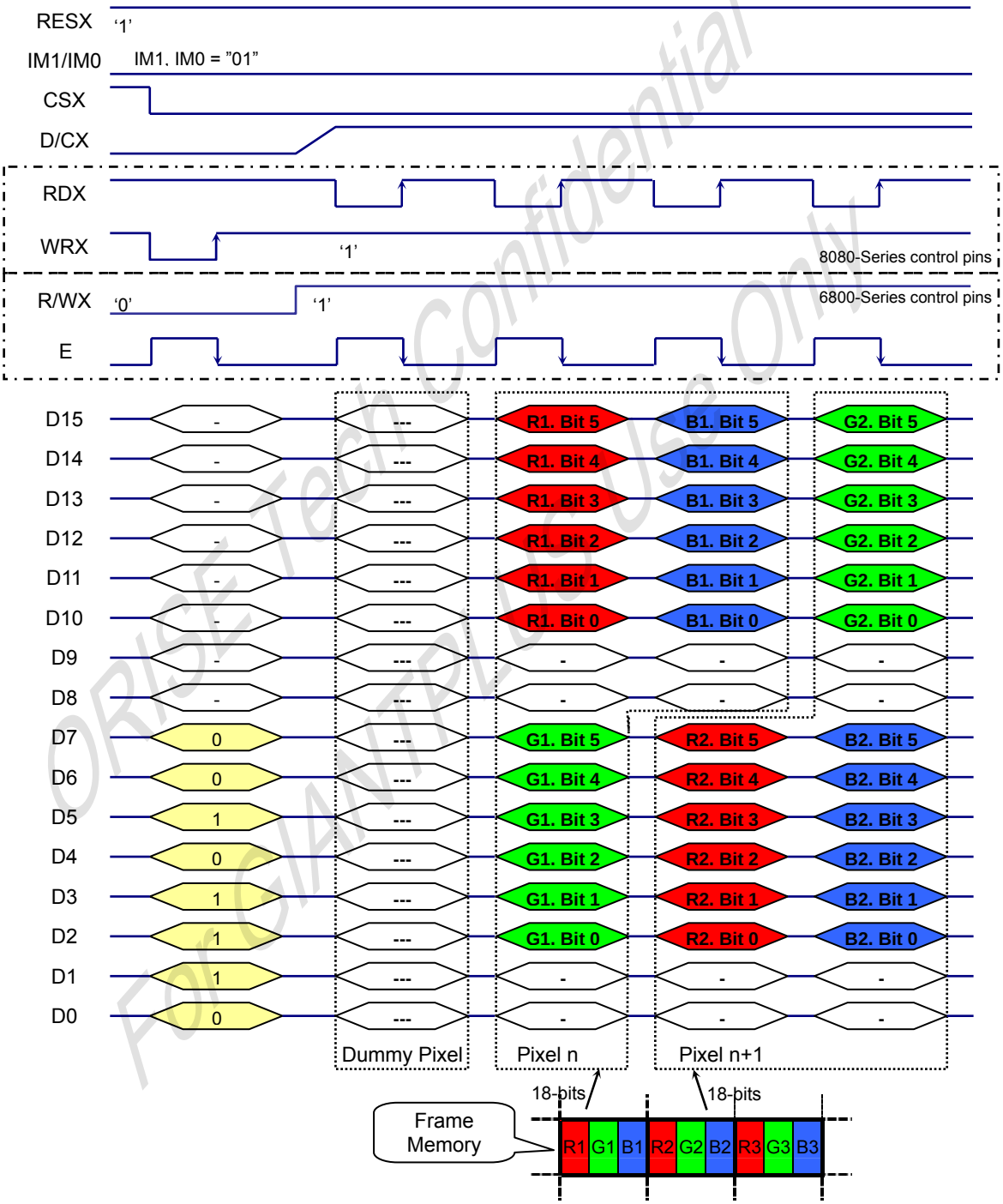
7.3.2.2 Parallel 16-Bits Bus Interface for RAM Data Read (IM1, IM0= "01")

There are 2 pixel (6 sub-pixels) per 3 bytes (RGB 6-6-6-bits output)



Note1. The data order is ad follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2.3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Note 3. '-' = Don't care - Can be set to VDDIO or DGND level

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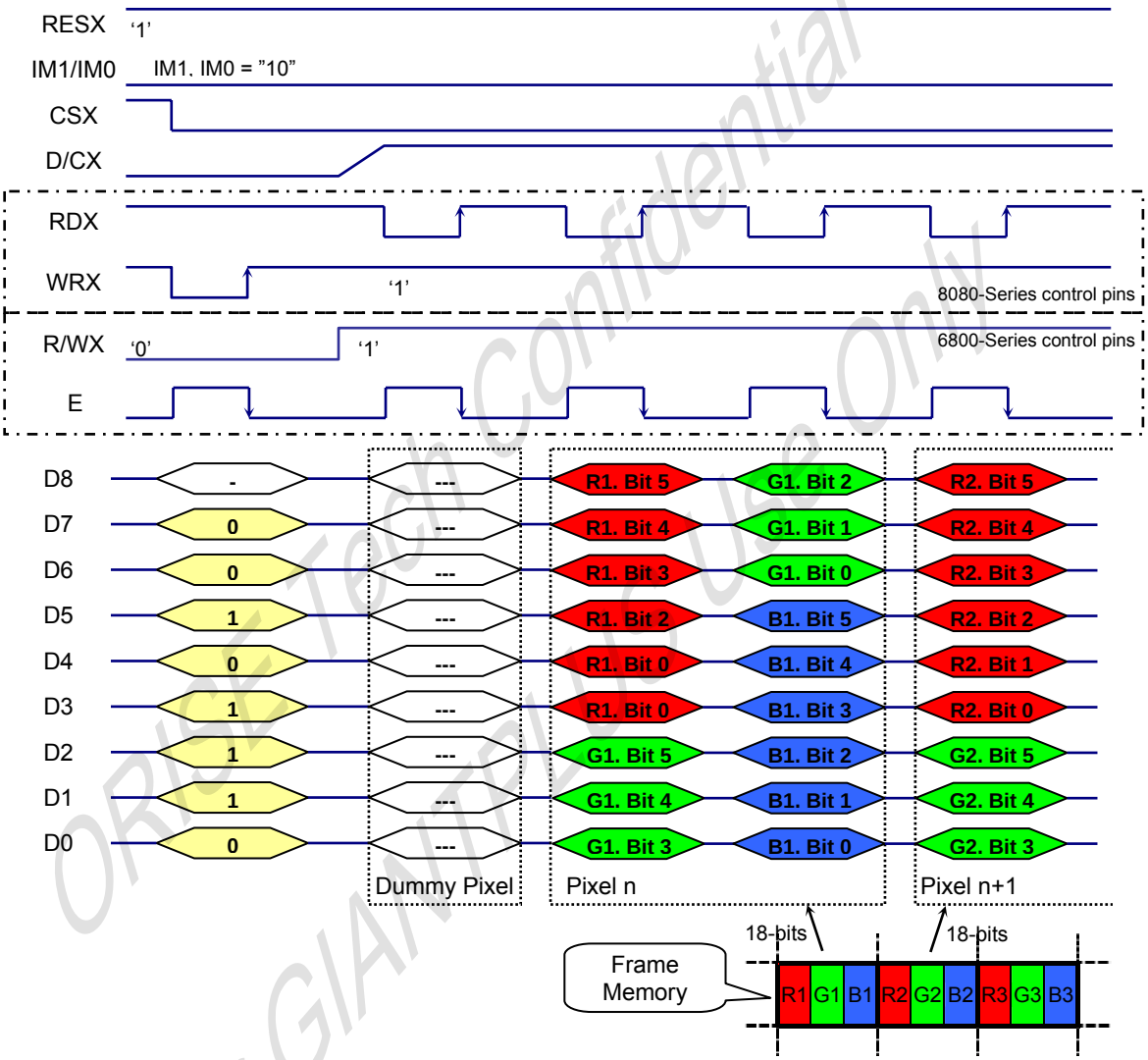
7.3.2.3 Parallel 9-Bits Bus Interface for RAM Data Read (IM1, IM0= "10")

There are 1 pixel (3 sub-pixels) per 2 bytes (RGB 6-6-6-bits output)



Note1. The data order is ad follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.
Note 2.3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.
Note 3. '-' = Don't care - Can be set to VDDIO or DGND level

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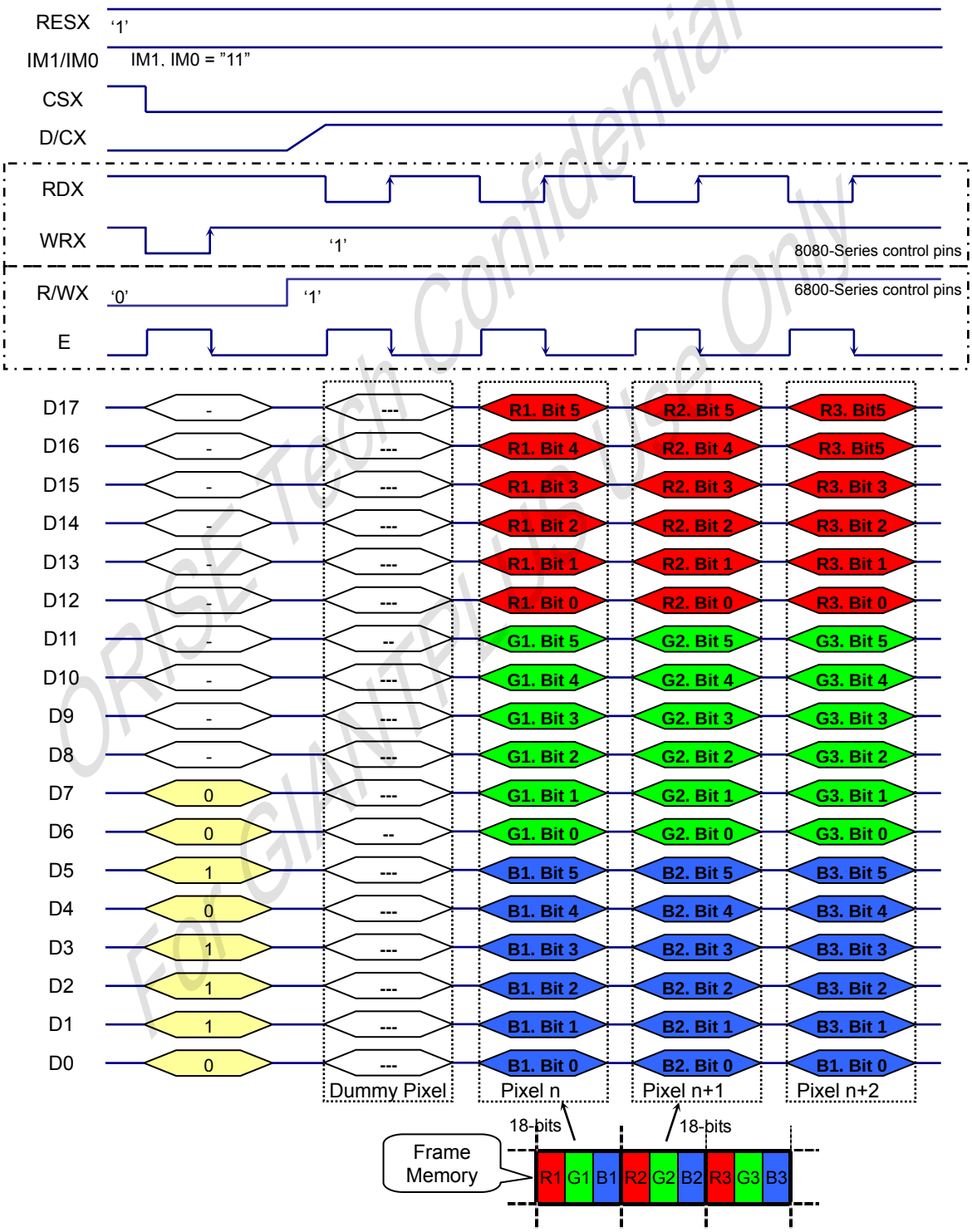
7.3.2.4 Parallel 18-Bits Bus Interface for RAM Data Read (IM1, IM0= "11")

There are 1 pixel (3 sub-pixels) per 1 bytes (RGB 6-6-6-bits output)



Note1. The data order is ad follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2.1-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Note 3. '-' = Don't care - Can be set to VDDIO or DGND level

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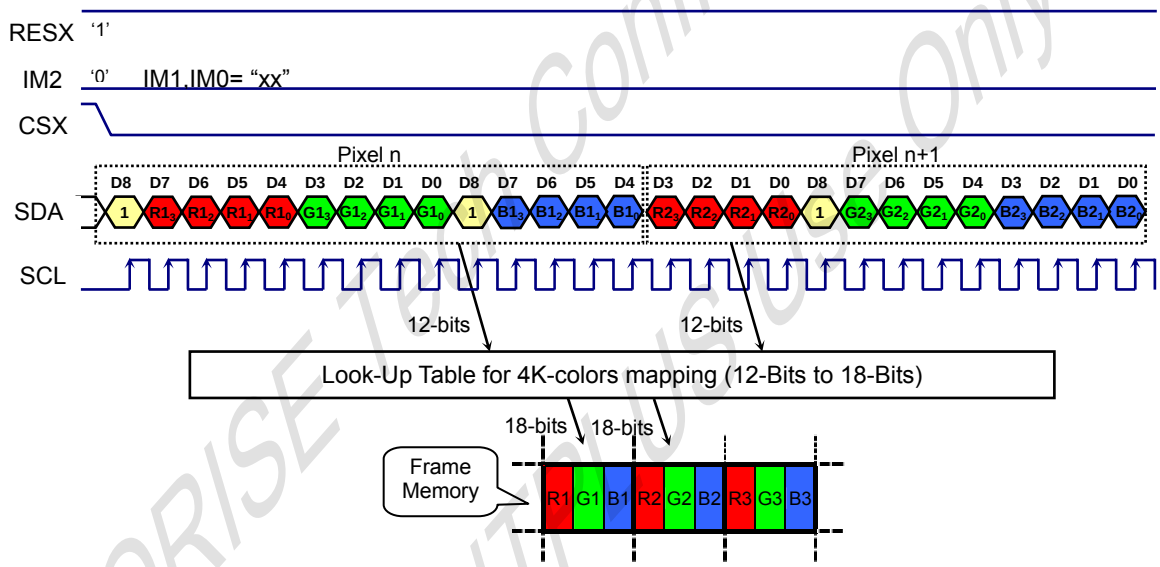
7.3.3. Serial Interface (IM2 = '0')

Different display data formats are available for three colors depth supported by the LCM listed below.

- 4K-Colours, RGB 4,4,4-bits input data. (3AH="03h")
- 65K-Colours, RGB 5,6,5-bits input data. (3AH="05h")
- 262K-Colours, RGB 6,6,6-bits input data. (3AH="06h")

7.3.3.1 Write data for 12-bits/pixel (RGB 4-4-4-bits input), 4K-colours, 3AH="03h"



Note 1. pixel data with the 12-bits color depth information
Note 2. The most significant bits are: Rx_3, Gx_3 and Bx_3
Note 3. The least significant bits are: Rx_0, Gx_0 and Bx_0
Note 4. '-' = Don't care - Can be set to VDDIO or DGND level

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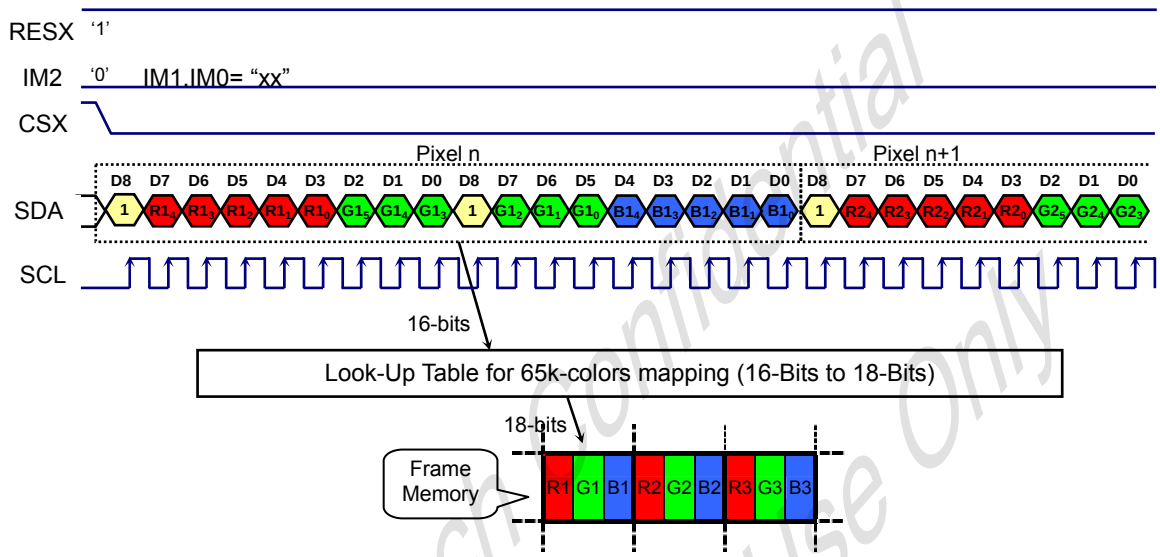
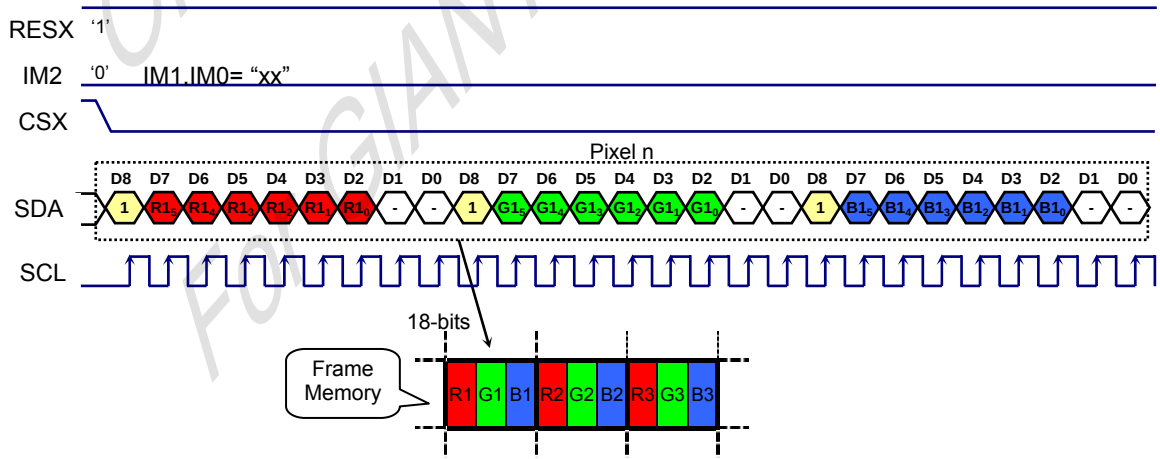
7.3.3.2 Write data for 16-bits/pixel (RGB 5-6-5-bits input), 65K-colours, 3AH="05h"



Note 1. pixel data with the 16-bits color depth information
Note 2. The most significant bits are: Rx_4, Gx_5 and Bx_4
Note 3. The least significant bits are: Rx_0, Gx_0 and Bx_0
Note 4. '-' = Don't care - Can be set to VDDIO or DGND level

7.3.3.3 Write data for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colours, 3AH="06h"



Note 1. pixel data with the 18-bits color depth information
Note 2. The most significant bits are: Rx_5, Gx_5 and Bx_5
Note 3. The least significant bits are: Rx_0, Gx_0 and Bx_0
Note 4. '-' = Don't care - Can be set to VDDIO or DGND level

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7.4. RGB interface

7.4.1. General Description

The module uses 6, 16 and 18-bits parallel RGB interface which includes: VS, HS, DE, PCLK, D[17:0]. The interface is activated after Power On sequence.

Pixel clock (PCLK) is running all the time without stoping and it is used to entering VS, HS, DE and D[17:0] states when there is a rising edge of the PCLK. The PCLK cannot be used as continues internal clock for other functions of the display module e.g. Sleep In –mode etc.

Vertical synchronization (VS) is used to tell when there is received a new frame of the display. This is negative ('0', low) active and its state is read to the display module by a rising edge of he PCLK signal.

Horizontal synchronization (HS) is used to tell when there is received a new line of the frame. This is negative ('0', low) active and its state is read to the display module by a rising edge of the PCLK signal.

Data Enable (DE) is used to tell when there is received a RGB information that should be transferred on the display. This is a positive ('1', high) active and its state is read to the display module by a rising edge of the PCLK signal.

D[17:0] (18-bit: R5-R0, G5-G0 and B5-B0; 16-bit: R4-R0, G5-G0 and B4-B0) are used to tell what is the information of the image that is transferred on the display (When DE='1' and there is a rising edge of PCLK). D[17:0] can be '0' (low) or '1' (high). These lines are read by a rising edge of the PCLK signal.

The PCLK cycle is described in the following figure.

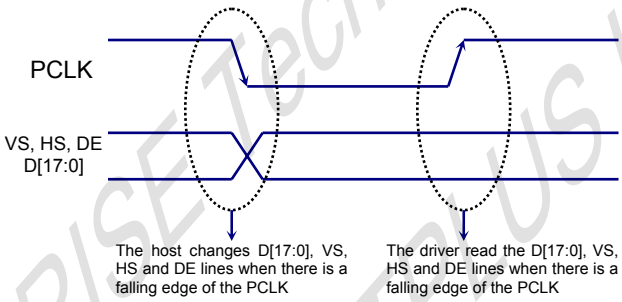

Fig. 7.4.1 PCLK cycle

Note: PCLK is an unsynchronized signal (It can be stopped).

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7.4.2. General Timing Diagram

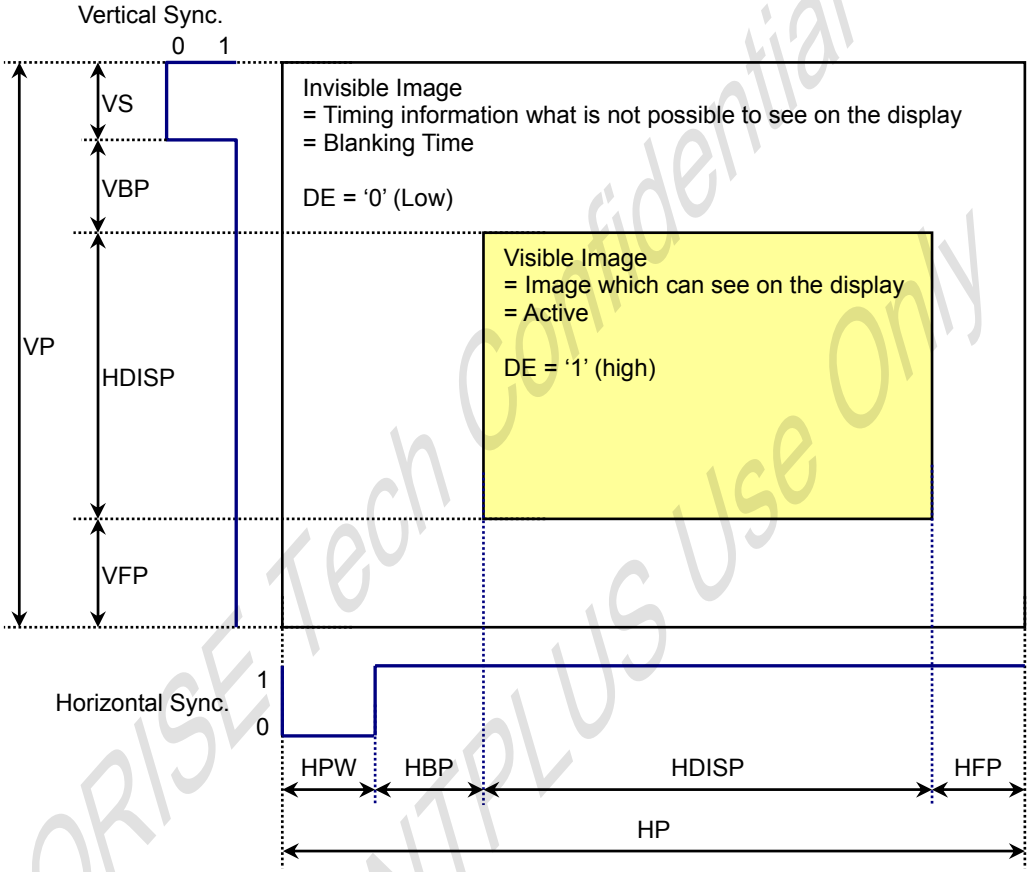

Fig. 7.4.2 RGB General Timing diagram

The image information must be correct on the display, when the timings are in range on the interface.

However, the image information can be incorrect on the display, when timings are not out of range on the interface (Out of the range timings cannot on the host side). The correct image information must be displayed automatically (by the display module) on the next frame (vertical sync.) when there is returned from out of the range to in range interface timing.

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7.4.3. Updating Order on Display Active Area (Normal Display Mode On + Sleep Out)

There is defined different kind of updating orders for display. These updating orders are controlled by H/W (SMX, SMY) and S/W (MX, MY,) bits.

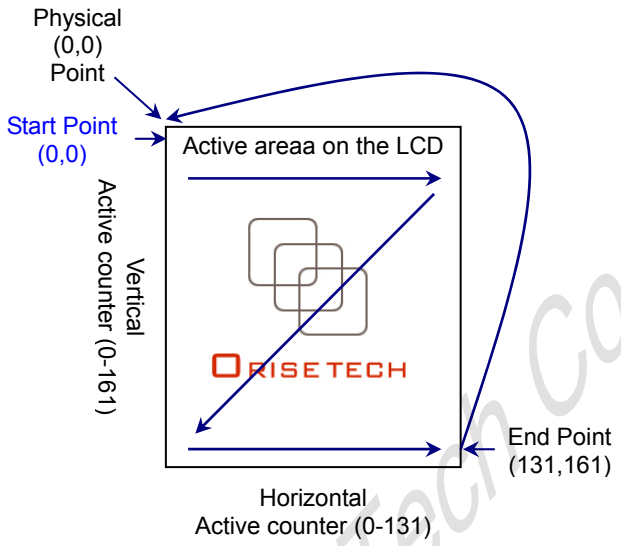

Fig. 7.4.3.1 Updating order when MADCTL's MX='0' and MY = '0'

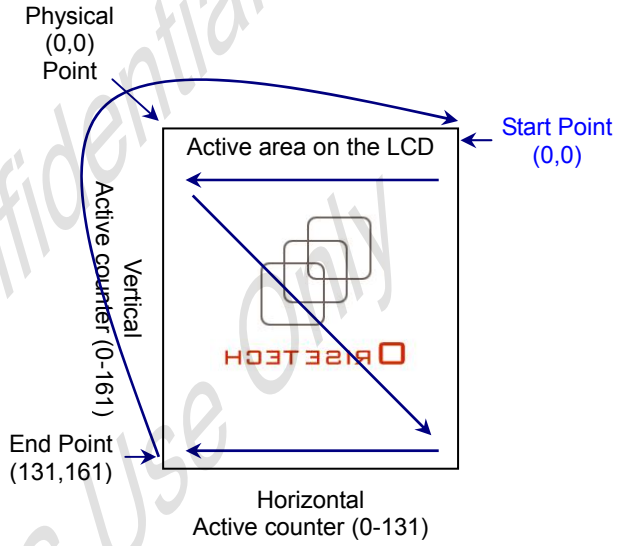

Fig. 7.4.3.2 Updating order when MADCTL's MX='1' and MY = '0'

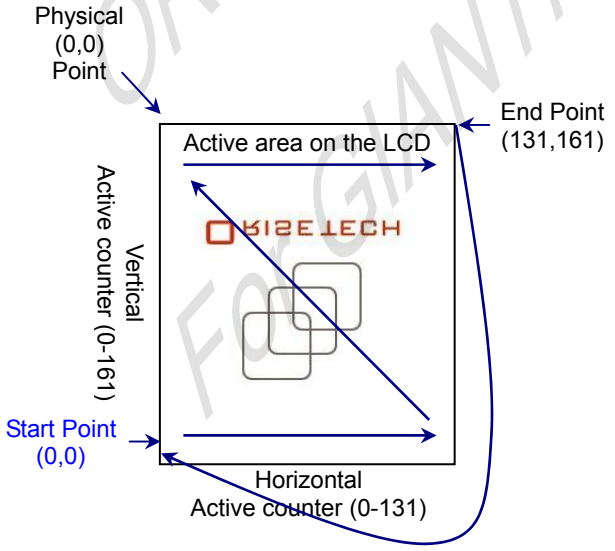

Fig. 7.4.3.3 Updating order when MADCTL's MX='0' and MY = '1'

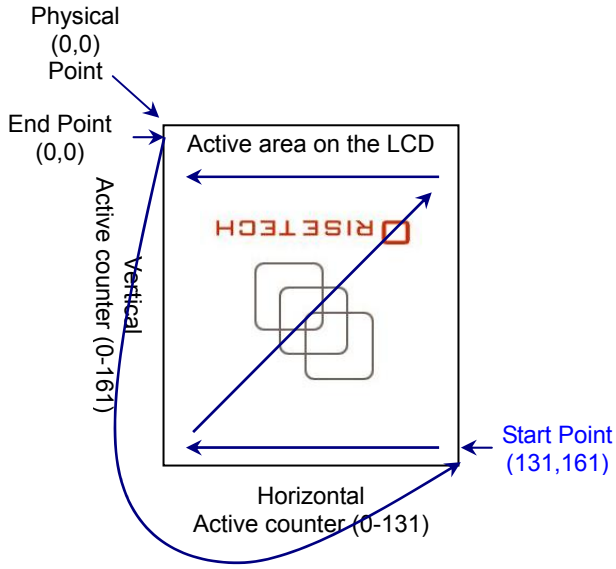

Fig. 7.4.3.4 Updating order when MADCTL's MX='1' and MY = '1'

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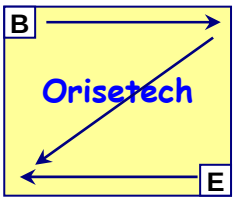
Table 7.4.3.1 Rules for Updating Order

Condition	Horizontal Counter	Vertical Counter
An active VS signal is received	Return to 0	Return to 0
Signal Pixel information of the active area is received	Increment by 1	No change
An active HS signal between two active area lines	Return to 0	Increment by 1
The Horizontal counter is larger than 127 and the Vertical counter is larger than 159	Return to 0	Return to 0

Note 1. Pixel order is RGB on the display.

Note 2. Data streaming direction from the host to the display is described in the following figure.



Data Stream from RGB I/F is like in this figure

Fig. 7.4.3.5 Data streaming order from RGB I/F

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7.4.4. RGB Interface Bus Width set

All 4-kinds of bus width can be available during RGB interface mode (selected by COLMOD (3Ah) command for 8-bits, 16-bits and 18-bits data width)

Table 7.4.4.1 RGB interface Bus Width Set Table

VIPF[3:0]	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus width
0101	R4	R3	R2	R1	R0	x	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	x	16-bits data
0110	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	18-bits data
VIPF[3:0]	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus width
1110	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	6-bits data
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

Note 1: When VIPF[3:0]="1110", 6-bits data width of 3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Note 2: Only VIPF[3:0]= "0101","0110" and "1110" are valid on RGB I/F, Others are invalid.

Note 3. 'x' Don't care, but need to set VDDIO or DGND level.

7.4.5. RGB Interface Mode Set

Table 7.4.5.1 RGB Interface Mode Set

RGB I/F Mode	PCLK	DE	VS	HS	Video Data bus D[17:0]	Register for Blanking Porch setting	Reference clock for Display
RGB Mode 1	Used	Used	Used	Used	Used	Not Used	Internal Oscillator
RGB Mode 2	Used	Used	Used	Used	Used	Used	Internal Oscillator

There are 2-kinds of RGB mode which is selected by RCM1 & RCM0 hardware pins.

In RGB Mode 1 (RCM1, RCM0 = "10"), writing data to frame memory is done by PCLK and Video Data Bus (D[17:0]), when DE is high state. The external synchronization signals (PCLK, VS and HS) are used for internal display signals. So, controller (host) must always transfer PCLK, VS, HS and DE signals to SPFD54124B.

In RGB Mode 2 (RCM1, RCM0 = "11"), blanking porch setting of VS and HS signals are defined by RGBBPCTR (B5h) command. When DE pin is high, valid data is directly stored to frame memory.

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7.4.6. RGB Interface Timing Diagram

7.4.6.1 General Timings for RGB I/F

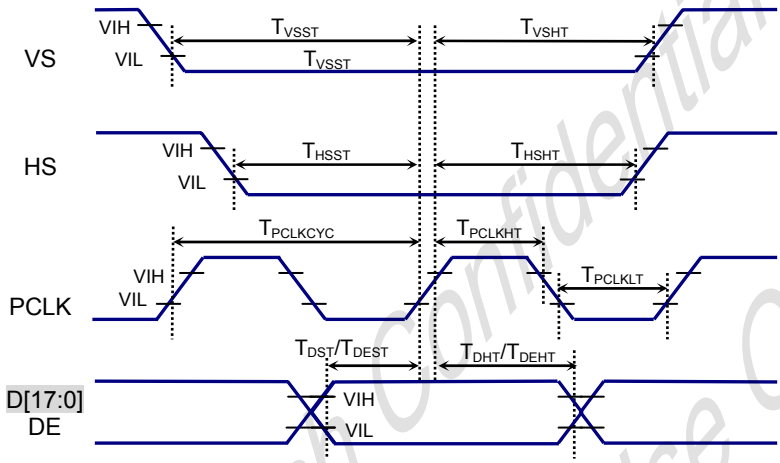

Fig. 7.4.6.1.1 General Timing for RGB I/F

Table 7.4.6.1.1 General Timing for RGB I/F

Item	Symbol	Condition	Specification			Unit
			Min	Type.	Max	
Pixel low pulse width	T_{PCLKLT}		15			
Pixel high pulse width	T_{PCLKHT}		15			
Vertical Sync. set-up time	T_{VSST}		15			ns
Vertical Sync. hold time	T_{VSSHT}		15			ns
Horizontal Sync. set-up time	T_{HSST}		15			ns
Horizontal Sync. hold time	T_{VSSHT}		15			ns
Data Enable set-up time	T_{DEST}		15			
Data Enable hold time	T_{DEHT}		15			
Data set-up time	T_{DST}		15			
Data hold time	T_{DHT}		15			

Note 1: VDDIO=1.6 to 3.6V, VDD=2.6 to 3.6V, AGND=DGND=0V, Ta=-30 to 70℃ (to +85℃ no damage)

Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Note 3. Data lines can be set to "High" or "Low" during blanking time – Don't care.

Note 4. Logic high and low levels are specified as 30% and 70% of VDDIO for Input signals.

Note 5. HP is multiples of eight PCLK.

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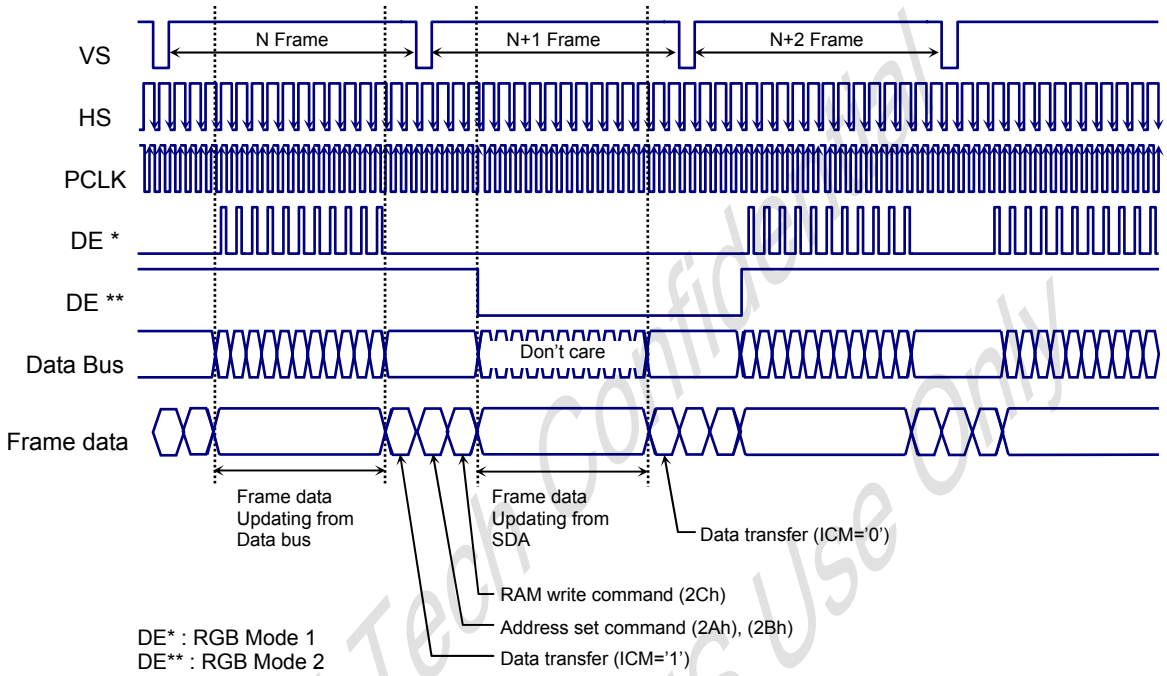

Fig. 7.4.6.1.2 RAM Access via SPI Interface in RGB Mode

Note: DP='0', EP='0', HSP='0' and VSP='0' of RGBCTR (B0h) command.

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7.4.6.2 RGB Interface Mode 1 Timing Diagram

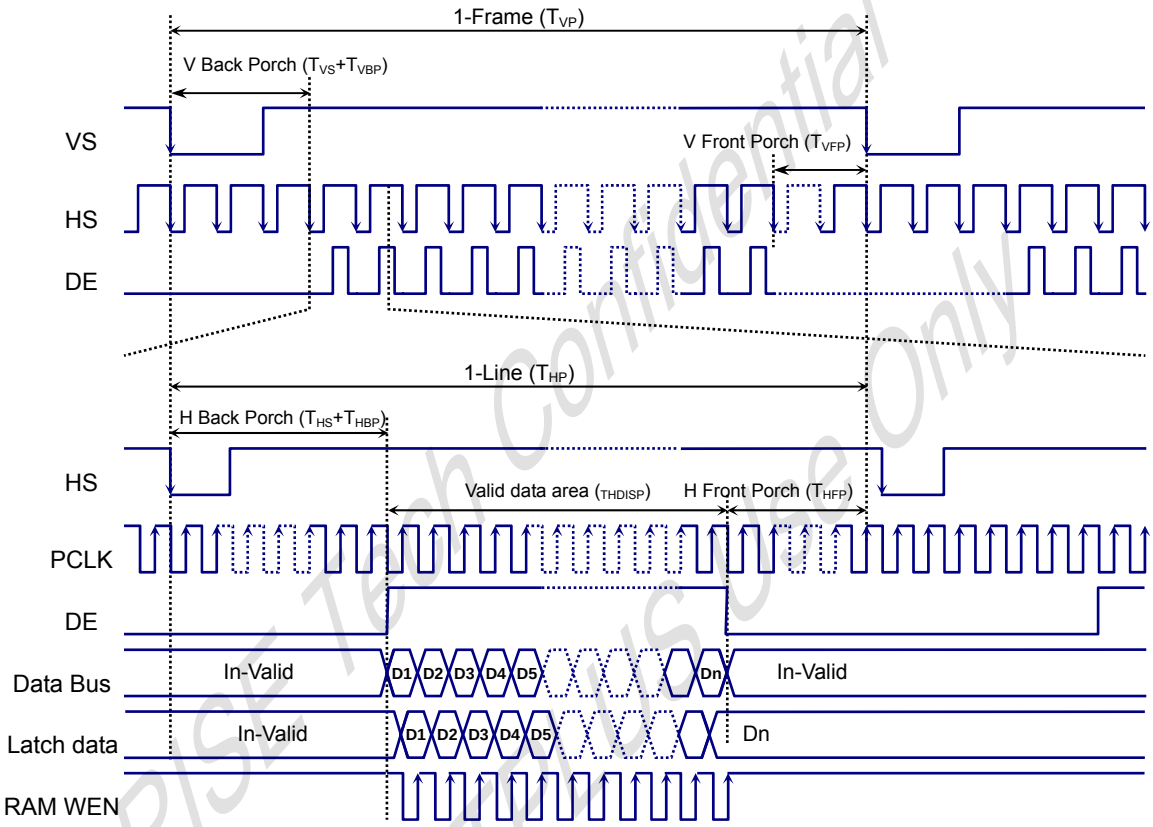

Fig. 7.4.6.2.1 RGB Mode 1 Timing Diagram

Note: DP='0', EP='0', HSP='0' and VSP='0' of RGBCTR (B0h) command.

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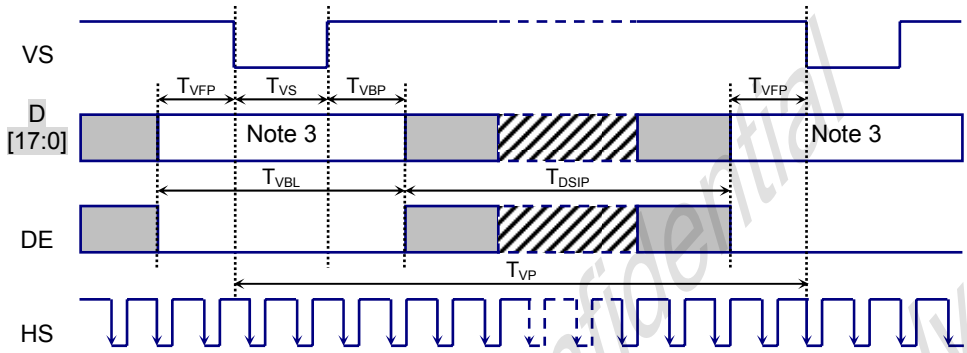
Vertical Timing for RGB I/F



Horizontal Timing for RGB I/F

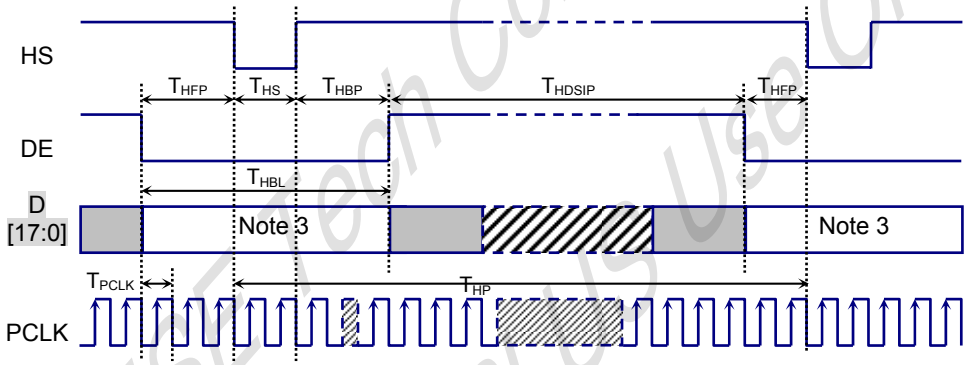


Fig. 7.4.6.2.2 Vertical and Horizontal timing for RGB I/F

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Table 7.4.6.2.1 Vertical and Horizontal Timing for RGB I/F

Item	Symbol	Condition	Specification			Unit
			Min	Type.	Max	
Vertical Timing						
Vertical cycle period	T_{VP}	GM="00" & "01"	166		172	HS
		GM="10"	134		140	HS
Vertical low pulse width	T_{VS}		2		4	HS
Vertical front porch	T_{VFP}		2		4	HS
Vertical back porch	T_{VBP}		2		4	HS
Vertical data start line		$T_{VS} + T_{VBP}$	4		8	HS
Vertical blanking period	T_{VBL}	$T_{VS} + T_{VBP} + T_{VFP}$	6		12	HS
Vertical active area	T_{VDISP}	GM="00" & "01"		160		HS
		GM="10"		128		
Vertical refresh rate	TVRR	Frame rate	61.75	65	68.25	Hz
Horizontal Timing						
Horizontal cycle period	T_{HP}	GM="00" & "10"	160		745	PCLK
		GM="01"	152		745	PCLK
Horizontal low pulse width	T_{HS}		2		256	PCLK
Horizontal front porch	T_{HFP}		2		256	PCLK
Horizontal back porch	T_{HBP}		2		256	PCLK
Horizontal data start point		$T_{HS} + T_{HBP}$	30		766	PCLK
		$ff_{HS} + f_{HBP}$	1.0			μs
Horizontal blanking period	T_{HBL}		32		768	PCLK
Horizontal active area	T_{HDISP}	GM="00" & "10"		128		PCLK
		GM="01"		120		PCLK
Pixel clock cycle	$T_{PCLKCYC}$	GM="00" TVRR=65Hz	100		579	ns
	$f_{PCLKCYC}$		1.7		10	MHz
	$T_{PCLKCYC}$	GM="01" TVRR=65Hz	100		610	ns
	$f_{PCLKCYC}$		1.6		10	MHz
	$T_{PCLKCYC}$	GM="10" TVRR=65Hz	100		718	ns
	$f_{PCLKCYC}$		1.4		10	MHz

Note 1. VDDIO=1.6 to 3.6V, VDD=2.6 to 3.6V, AGND=DGND=0V, Ta=-30 to 70℃ (to +85℃ no damage)

Note 2. Data lines can be set to "High" or "Low" during blanking time – Don't care.

Note 3. HP is multiples of eight PCLK.

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7.4.6.3 RGB Interface Mode 2 Timing Diagram

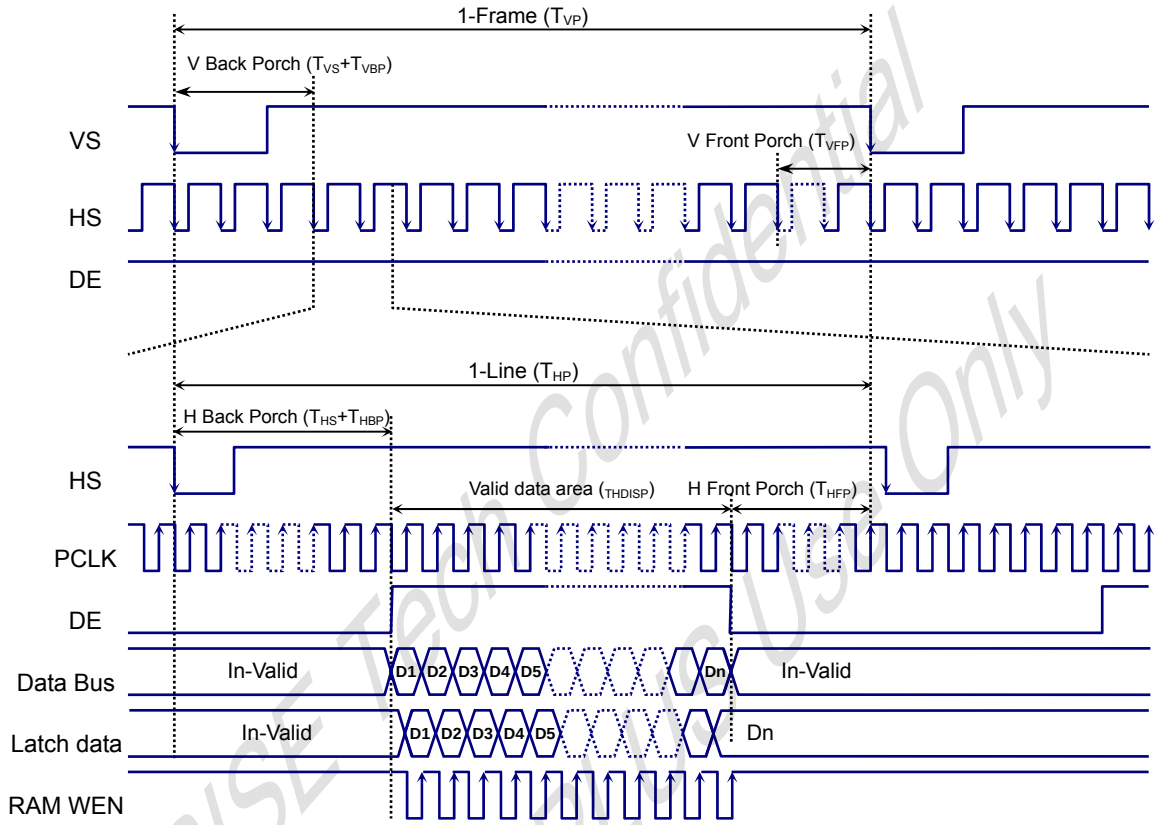

Fig. 7.4.6.3.1 RGB Mode 2 Timing Diagram

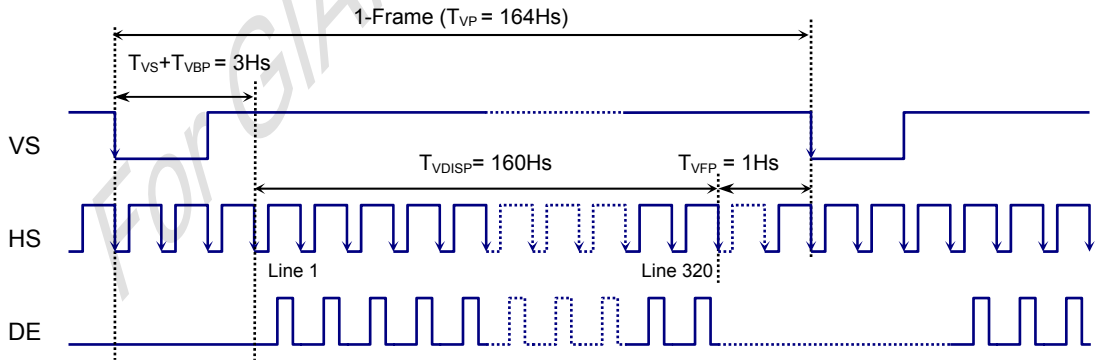

Fig. 7.4.6.3.2 RGB Mode 2 Vertical Timing Diagram

Note: DP='0', EP='0', HSP='0' and VSP='0' of RGBCTR (B0h) command.

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-128xRGBx160

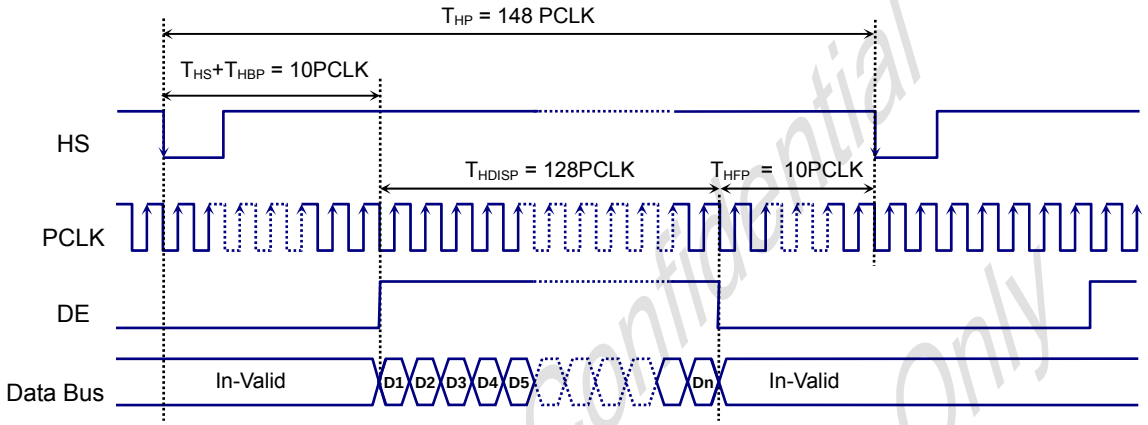

Fig. 7.4.6.3.3 RGB Mode 2 Horizontal Timing Diagram

Note: DP='0', EP='0', HSP='0' and VSP='0' of RGBCTR (B0h) command.

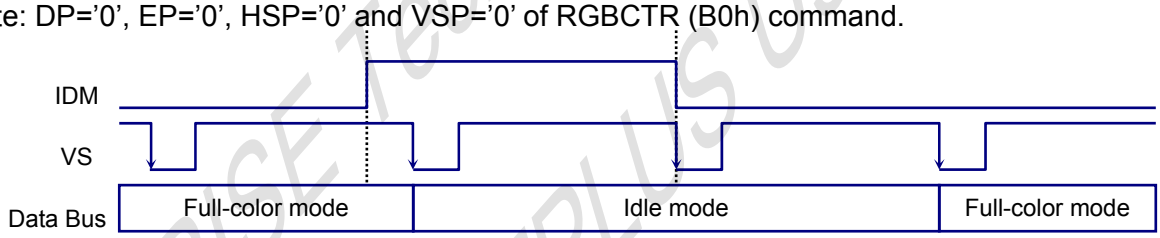

Fig. 7.4.6.3.4 RGB Mode 2 Idle mode Timing Diagram

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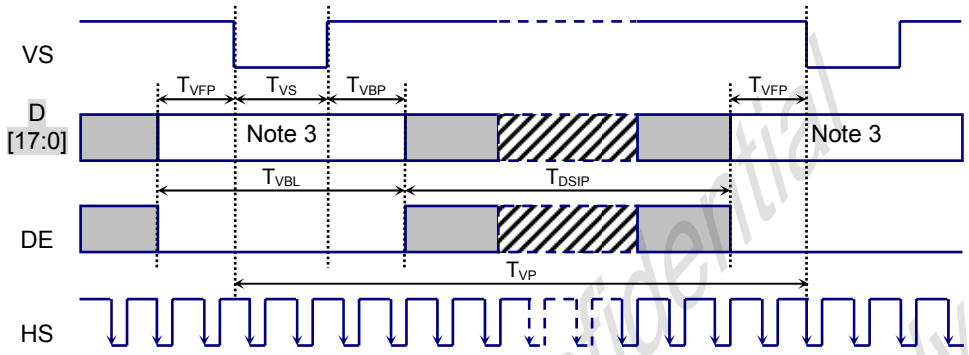
Vertical Timing for RGB I/F



Horizontal Timing for RGB I/F

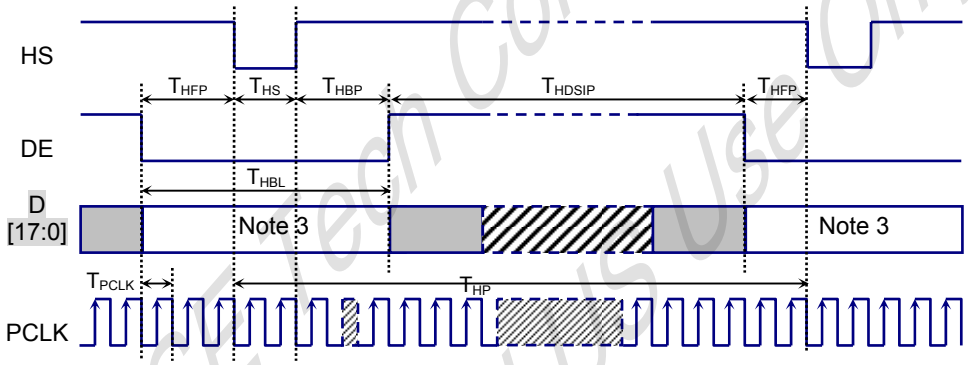


Fig. 7.4.6.3.5 Vertical and Horizontal timing for RGB I/F

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Table 7.4.6.3.1 Vertical and Horizontal Timing for RGB I/F

Item	Symbol	Condition	Specification			Unit
			Min	Type.	Max	
Vertical Timing						
Vertical cycle period	T_{VP}	GM="00" & "01"	163	164		HS
		GM="10"	131	132		HS
Vertical low pulse width	T_{VS}		1		4	HS
Vertical front porch	T_{VFP}		1	1	1023	HS
Vertical back porch	T_{VBP}		1		1022	HS
Vertical data start line		$T_{VS} + T_{VBP}$	2	3	1023	HS
Vertical blanking period	T_{VBL}	$T_{VS} + T_{VBP} + T_{VFP}$	3	4	1023	HS
Vertical active area	T_{VDISP}	GM="00" & "01"		160		HS
		GM="10"		128		HS
Vertical refresh rate	TVRR	Frame rate	61.75	65	68.25	Hz
Horizontal Timing						
Horizontal cycle period	T_{HP}	GM="00" & "10"	131	148	511	PCLK
		GM="01"	123	140	511	PCLK
Horizontal low pulse width	T_{HS}		1		63	PCLK
Horizontal front porch	T_{HFP}		1		63	PCLK
Horizontal back porch	T_{HBP}		1		62	PCLK
Horizontal data start point		$T_{HS} + T_{HBP}$	1	10	63	PCLK
		$ff_{HS} + f_{HBP}$	TBD			µs
Horizontal blanking period	T_{HBL}	$T_{HS} + T_{HBP} + T_{HFP}$	3	20	256	PCLK
Horizontal active area	T_{HDISP}	GM="00" & "10"		128		PCLK
		GM="01"		120		PCLK
Pixel clock cycle	$T_{PCLKCYC}$	(GM='0')	100	634	720	Ns
	$f_{PCLKCYC}$		1.39	1.58	10	MHz
	$T_{PCLKCYC}$	(GM='1')	100	670	767	Ns
	$f_{PCLKCYC}$		1.30	1.49	10	MHz
	$T_{PCLKCYC}$		100	788	896	Ns
	$f_{PCLKCYC}$		1.12	1.27	10	MHz

Note 1. VDDIO=1.6 to 3.6V, VDD=2.6 to 3.6V, AGND=DGND=0V, Ta=-30 to 70℃ (to +85℃ no damage)

Note 2. Data lines can be set to "High" or "Low" during blanking time – Don't care.

Note 3. HP is multiples of eight PCLK.

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7.4.6.4 Power On Sequence on RGB Mode 2

The Driver operates power up and display ON by VDD, VDDIO, SHUT, VS, HS, DE, PCLK on RGB mode 2 as show as following figure.

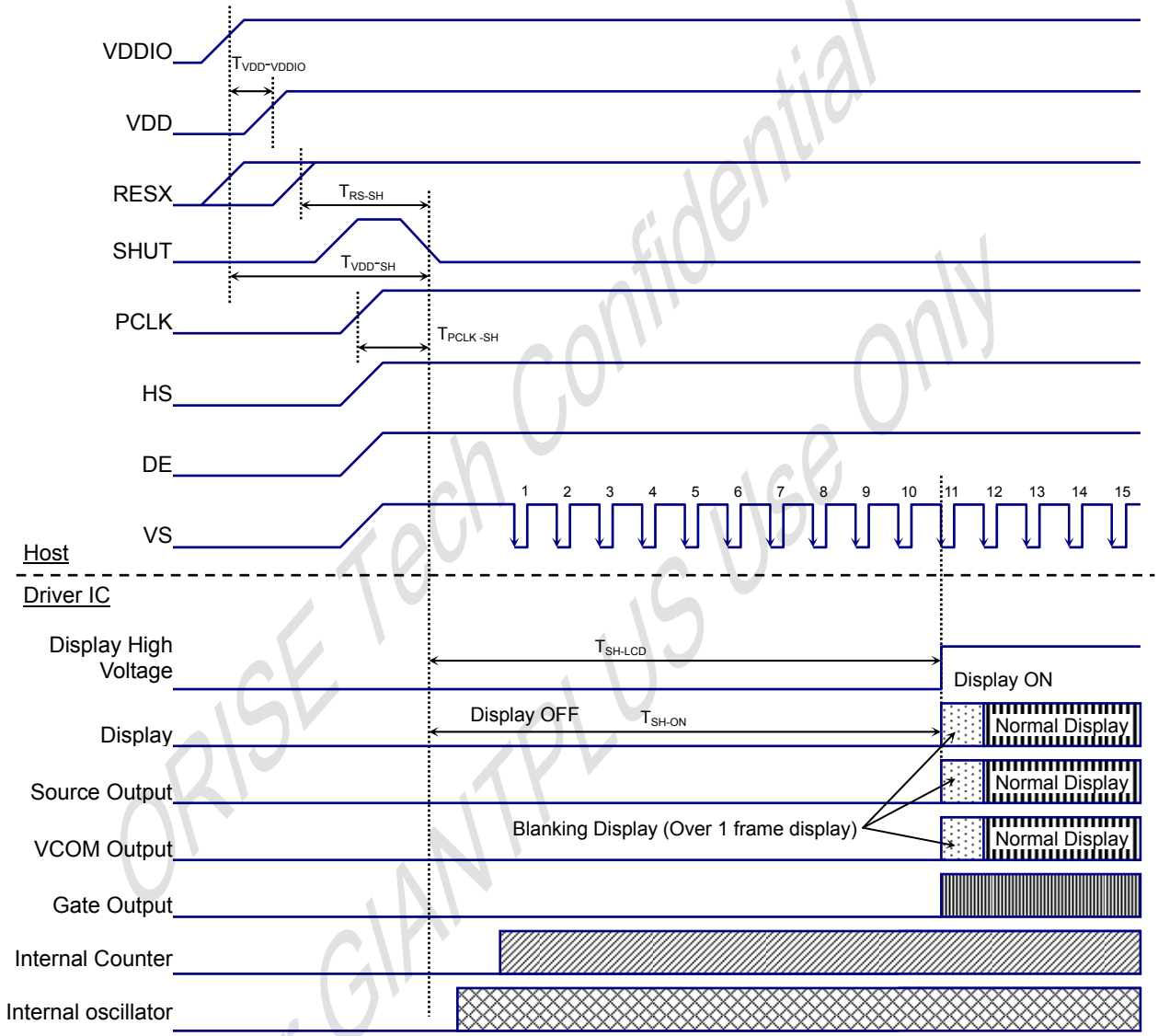

Fig. 7.4.6.4.1 Power On Sequence on RGB Mode 2

Table 7.4.6.4.1 Power ON AC Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit	Remark
VDDIO On to VDD On	$T_{VDDIO-VDD}$	0			ns	Note1
VDDIO/VDD on to falling edge of SHUT	T_{VDD-SH}	1			ms	
RESX to falling of SHUT	T_{RS-SH}	10			us	
Signals input to falling edge of SHUT *	T_{CLK-SH}	1			PCLK	Note2
Falling edge of SHUT to LCD power ON	T_{SH-LCD}			120	ms	
Falling edge of SHUT to Display start	T_{SH-ON}		10		VS	

Note 1: $T_{VDDIO-VDD}$ can be <=0ns, >0ns. In any case, VDDIO and VDD power up sequence should not have any impact on the driver / display functionalities / performance.

Note 2: Signals mean VS, HS, DE and PCLK signal.

Note 3: DP='0', EP='0', HSP='0' and VSP='0' of RGBCTR (B0h) command.

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7.4.6.5 Power OFF Sequence on RGB Mode 2

The Driver operates power off and display OFF by VDD, VDDIO, SHUT, VS, HS and DE on RGB mode 2 as show as following figure.

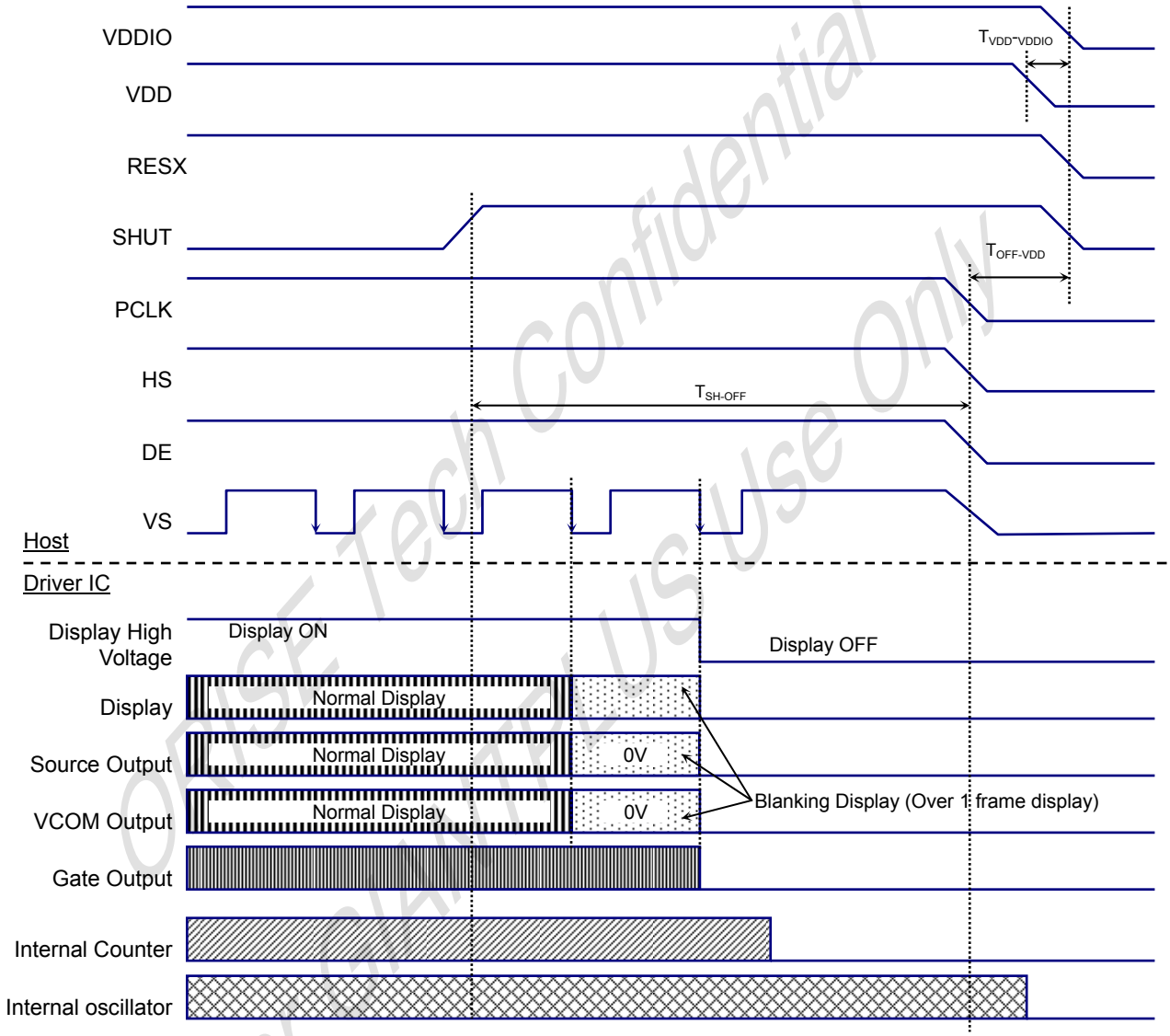

Fig. 7.4.6.5.1 Power OFF Sequence on RGB Mode 2

Table 7.4.6.5.1 Power OFF AC Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit	Remark
VDDIO On to VDD On	$T_{VDDIO-VDD}$	0			ns	Note1
Signals input to VDDIO/VDD off	T_{SH-OFF}	1			us	Note2
Rising edge of SHUT to Display off	T_{SH-OFF}	2			VS	

Note 1: $T_{VDDIO-VDD}$ can be <=0ns, >0ns. In any case, VDDIO and VDD power up sequence should not have any impact on the driver / display functionalities / performance.

Note 2: Signals mean VS, HS, DE and PCLK signal.

Note 3: DP='0', EP='0', HSP='0' and VSP='0' of RGBCTR (B0h) command.

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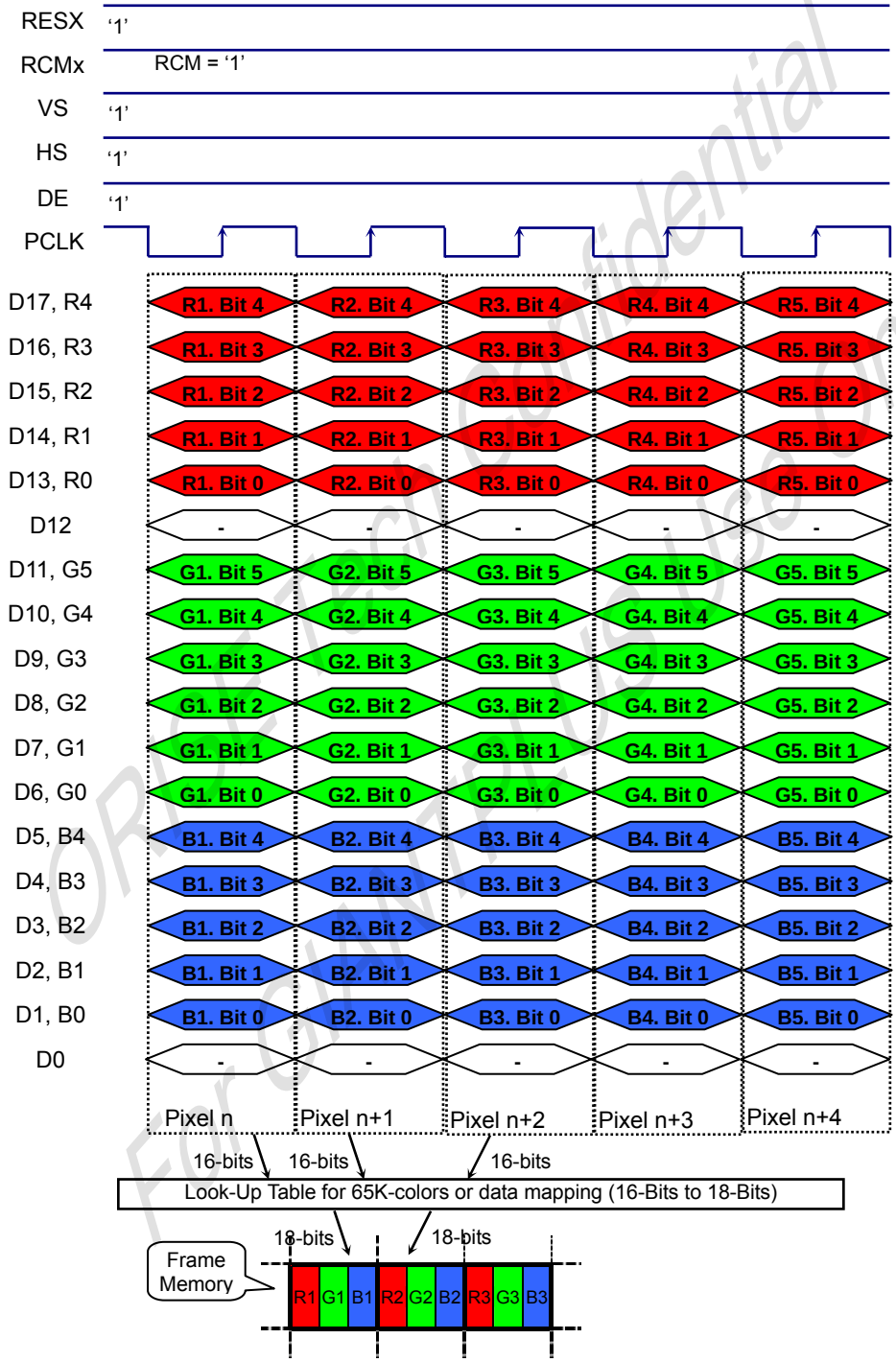
7.4.7. RGB Data Color Coding

7.4.7.1 16-bits/pixel Colour Order on the RGB Interface



Note 1: The data order is as follows, MSB=D23, LSB=D0 and picture data is MSB=Bit5, LSB=Bit0 for Green data and MSB=Bit4, LSB=Bit0 for Red and Blue data.

Note 2. '-' Don't care, but need set to VDDIO or DGND level.

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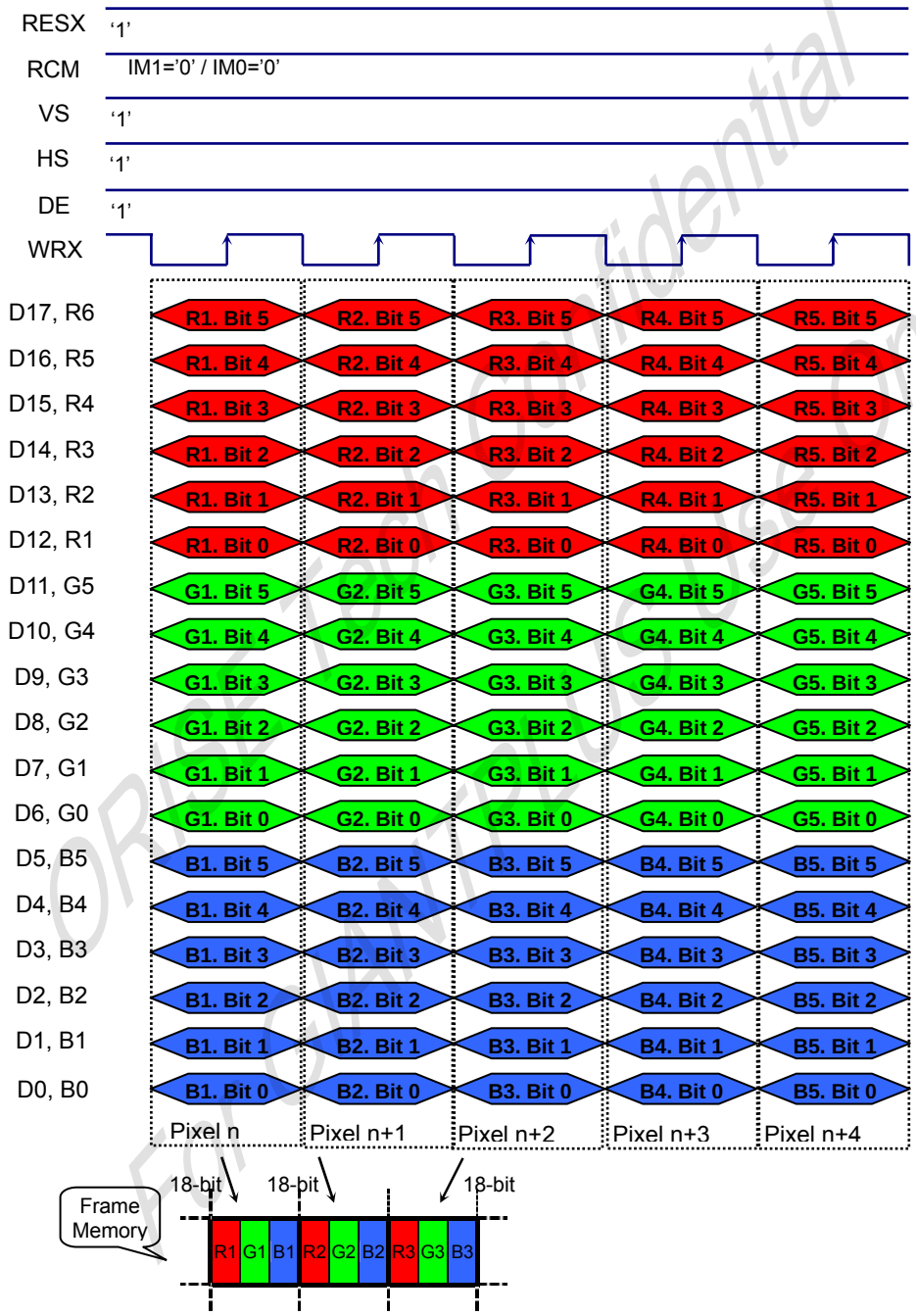
7.4.7.2 18-bits/pixel Colour Order on the RGB Interface



Note 1: The data order is as follows, MSB=D23, LSB=D0 and picture data is MSB=Bit5, LSB=Bit0 for Red, Green and Blue data.
Note 2. '-' Don't care, but need set to VDDIO or DGND level.

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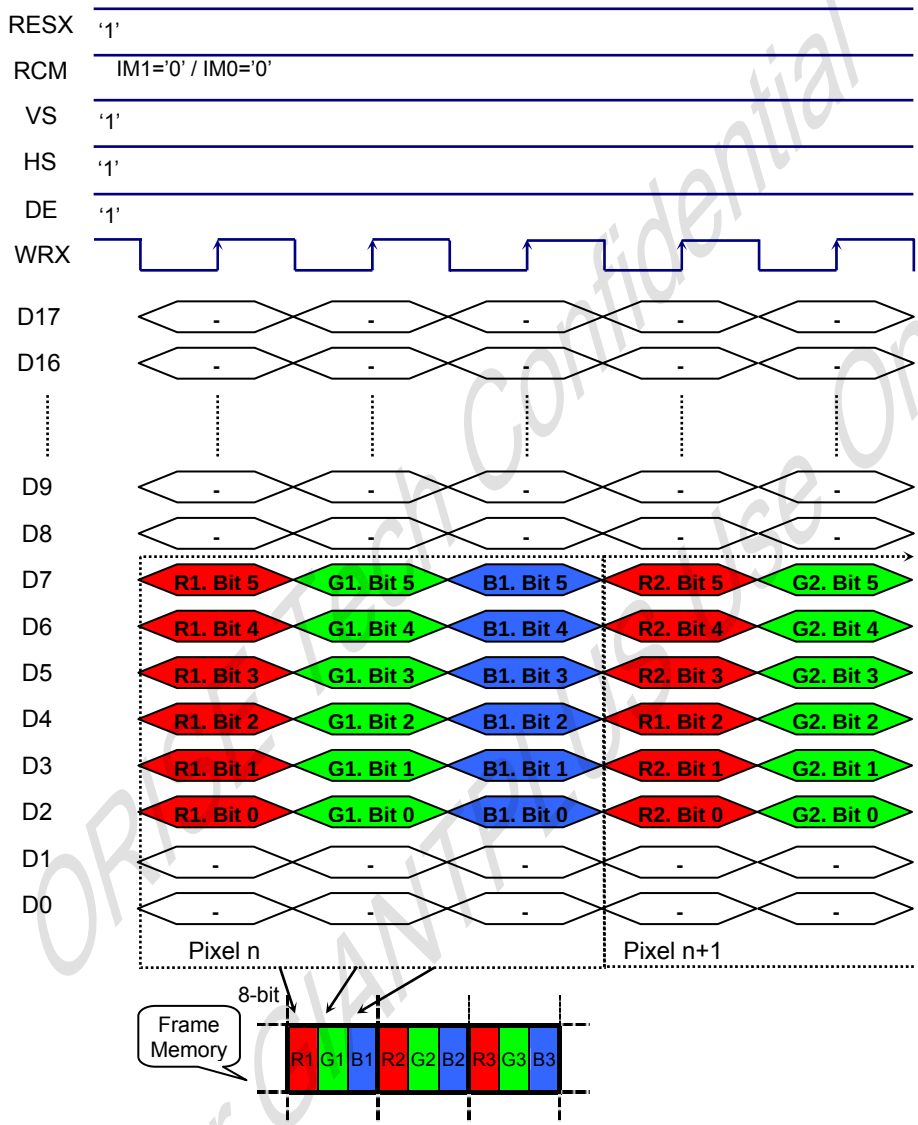
7.4.7.3 6-bits/pixel Colour Order on the RGB Interface



Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit5, LSB=Bit0 for Red, Green and Blue data.
Note 2. '-' Don't care, but need set to VDDIO or DGND level.

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7.5. Display Data RAM

7.5.1. Configuration

The display module has an integrated 132x162x18-bit graphic type static RAM. This 384,912-bits memory allows to store on-chip a 132xRGBx162 image with an 18-bpp resolution (262K-color).

There will be no abnormal visible effect on the display when there is a simultaneous Panel Read

and interface Read or Write to the same location of the Frame Memory.

Display Data RAM Organization (GM='00')

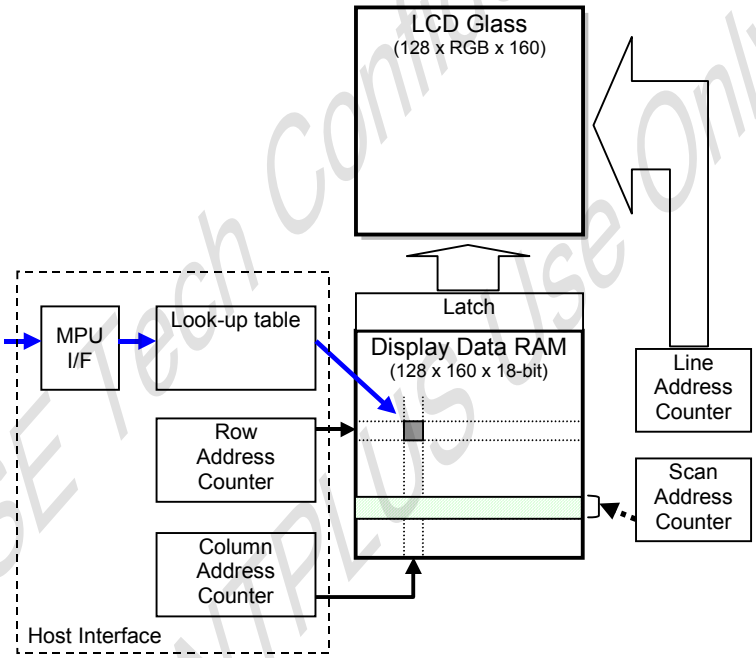

Fig. 7.5.1.1 Display Date RAM Organization

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7.5.2. Memory to Display Address Mapping

7.5.2.1 When using 128RGB x 160 resolution (GM1, GM0 = “00”, SMX=SMY=SRGB=’0’)

			Pixel 1			Pixel 2			--------	Pixel 127			Pixel 128				
Gate Out	**Source Out**		**S7**	**S8**	**S9**	**S10**	**S11**	**S12**	--------	**S385**	**S386**	**S387**	**S388**	**S389**	**S390**		
	RA		RGB=0		RGB=1	RGB=0		RGB=1	RGB Order	RGB=0		RGB=1	RGB=0		RGB=1	SA	
	MY=’0’	MY=’1’														ML=’0’	ML=’1’
2	0	159	R0	G0	B0	R1	G1	B1	--------	R126	G126	B126	R127	G127	B127	0	159
3	1	158							--------							1	158
4	2	157							--------							2	157
5	3	156							--------							3	156
6	4	155							--------							4	155
7	5	154							--------							5	154
8	6	153							--------							6	153
9	7	152							--------							7	152
154	152	7							--------							152	7
155	153	6							--------							153	6
156	154	5							--------							154	5
157	155	4							--------							155	4
158	156	3							--------							156	3
159	157	2							--------							157	2
160	158	1							--------							158	1
161	159	0							--------							159	0
	CA	MX=’0’	0			1			--------	126			127				
		MX=’1’	127			126			--------	1			0				

Note

RA = Row Address,

CA = Column Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Column address direction parameter), D7 parameter of MADCTL command

MX =Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

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7.5.2.2 When using 120RGB x 160 resolution (GM1, GM0 = “01”, SMX=SMY=SRGB=’0’)

			Pixel 1			Pixel 2			--------	Pixel 119			Pixel 120				
Gate Out	**Source Out**		**S7**	**S8**	**S9**	**S10**	**S11**	**S12**	--------	**S361**	**S362**	**S363**	**S364**	**S365**	**S366**		
	RA		RGB=0		RGB=1	RGB=0		RGB=1	RGB Order	RGB=0		RGB=1	RGB=0		RGB=1	SA	
	MY=’0’	MY=’1’														ML=’0’	ML=’1’
2	0	159	R0	G0	B0	R1	G1	B1	--------	R118	G118	B118	R119	G119	B119	0	159
3	1	158							--------							1	158
4	2	157							--------							2	157
5	3	156							--------							3	156
6	4	155							--------							4	155
7	5	154							--------							5	154
8	6	153							--------							6	153
9	7	152							--------							7	152
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
154	152	7							--------							152	7
155	153	6							--------							153	6
156	154	5							--------							154	5
157	155	4							--------							155	4
158	156	3							--------							156	3
159	157	2							--------							157	2
160	158	1							--------							158	1
161	159	0							--------							159	0
	CA	MX=’0’	0			1			--------	118			119				
		MX=’1’	119			118			--------	1			0				

Note

RA = Row Address,

CA = Column Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Column address direction parameter), D7 parameter of MADCTL command

MX =Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

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7.5.2.3 When using 128RGB x 128 resolution (GM1, GM0 = “10”, SMX=SMY=SRGB=’0’)

			Pixel 1			Pixel 2			--------	Pixel 127			Pixel 128				
Gate Out	**Source Out**		**S7**	**S8**	**S9**	**S10**	**S11**	**S12**	--------	**S385**	**S386**	**S387**	**S388**	**S389**	**S390**		
	RA		RGB=0		RGB=1	RGB=0		RGB=1	RGB Order	RGB=0		RGB=1	RGB=0		RGB=1	SA	
	MY=’0’	MY=’1’														ML=’0’	ML=’1’
2	0	127	R0	G0	B0	R1	G1	B1	--------	R126	G126	B126	R127	G127	B127	0	127
3	1	126							--------							1	126
4	2	125							--------							2	125
5	3	124							--------							3	124
6	4	123							--------							4	123
7	5	122							--------							5	122
8	6	121							--------							6	121
9	7	120							--------							7	120
122	120	7							--------							120	7
123	121	6							--------							121	6
124	122	5							--------							122	5
125	123	4							--------							123	4
126	124	3							--------							124	3
127	125	2							--------							125	2
128	126	1							--------							126	1
129	127	0							--------							127	0
	CA	MX=’0’	0			1			--------	126			127				
		MX=’1’	127			126			--------	1			0				

Note

RA = Row Address,

CA = Column Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Column address direction parameter), D7 parameter of MADCTL command

MX =Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

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7.5.2.4 When using 132RGB x 162 resolution (GM1, GM0 = “11”, SMX=SMY=SRGB=’0’)

			Pixel 1			Pixel 2			--------	Pixel 131			Pixel 132				
Gate Out	**Source Out**		**S1**	**S2**	**S3**	**S4**	**S5**	**S6**	--------	**S391**	**S392**	**S393**	**S394**	**S395**	**S396**		
			RGB=0		RGB=1	RGB=0		RGB=1	RGB Order	RGB=0		RGB=1	RGB=0		RGB=1		
	RA															SA	
	MY=’0’	MY=’1’														ML=’0’	ML=’1’
1	0	161	R0	G0	B0	R1	G1	B1	--------	R130	G130	B130	R131	G131	B131	0	161
2	1	160							--------							1	160
3	2	159							--------							2	159
4	3	158							--------							3	158
5	4	157							--------							4	157
6	5	156							--------							5	156
7	6	155							--------							6	155
8	7	154							--------							7	154
155	154	7							--------							154	7
156	155	6							--------							155	6
157	156	5							--------							156	5
158	157	4							--------							157	4
159	158	3							--------							158	3
160	159	2							--------							159	2
161	160	1							--------							160	1
162	161	0							--------							161	0
	CA	MX=’0’	0			1			--------	130			131				
		MX=’1’	131			130			--------	1			0				

Note

RA = Row Address,

CA = Column Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Column address direction parameter), D7 parameter of MADCTL command

MX =Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

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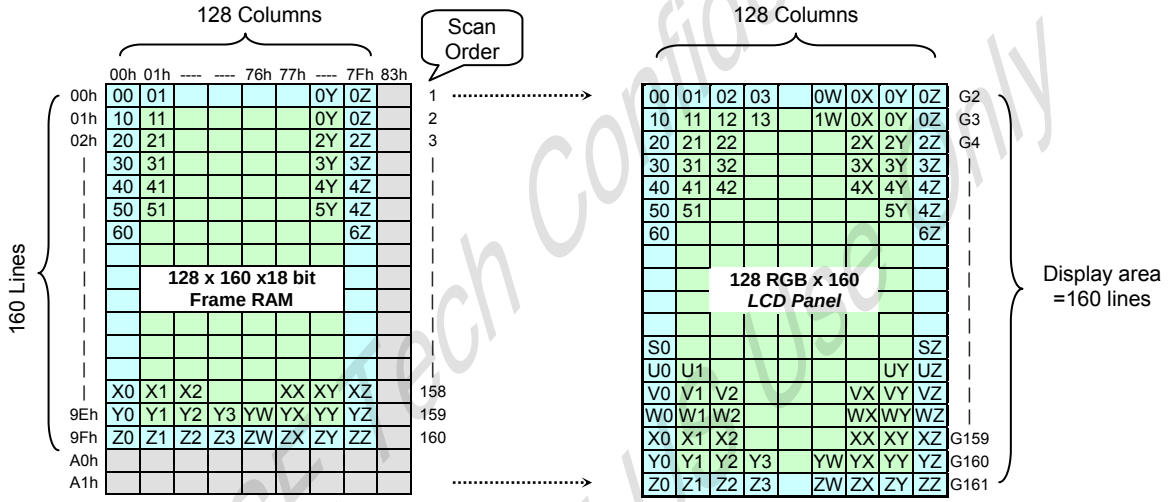
7.5.3. Normal Display On or Partial Mode On, Vertical Scroll Off

7.5.3.1 When using 128RGB x 160 resolution (GM1, GM0 = "00")

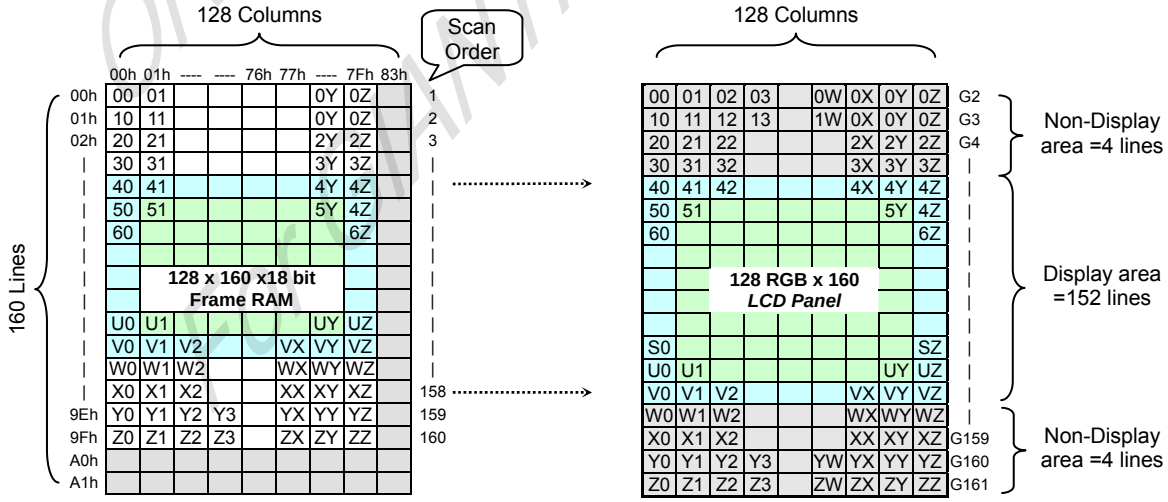
In this mode, contents of the frame memory within an area where column pointer is 00h to 7Fh and page pointer is 00h to 9Fh is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

(1) Example for Normal Display On (MX=MY=ML='0' ,SMX=SMY='0')



(2). Example for Partial Display On (PSL[7:0]=04h,PEL[7:0]=9Bh, MX=MV=ML='0' ,SMX=SMY='0')



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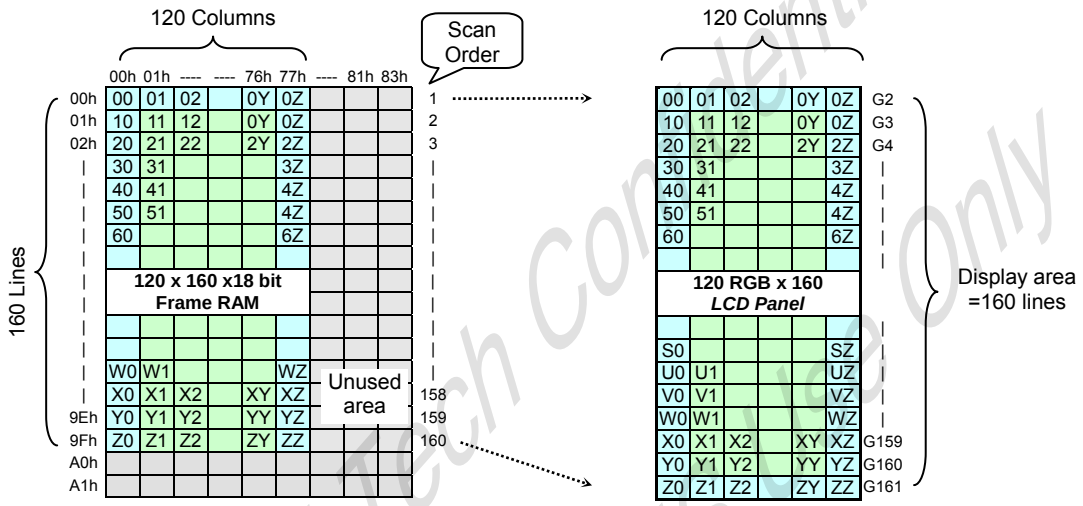
7.5.3.2 When using 120RGB x 160 resolution (GM1, GM0 = "01")

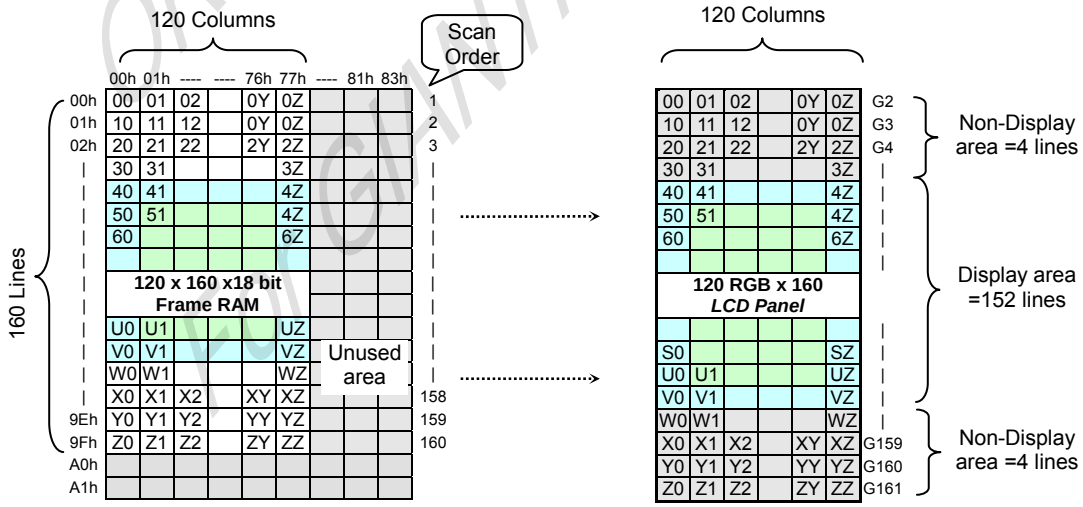
In this mode, contents of the frame memory within an area where column pointer is 00h to 77h and page pointer is 00h to 9Fh is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

(1) Example for Normal Display On (MX=MY=ML='0', SMX=SMY='0')



(2) Example for Partial Display On (PSL[7:0]=04h,PEL[7:0]=9Bh, MX=MV=ML='0', SMX=SMY='0')



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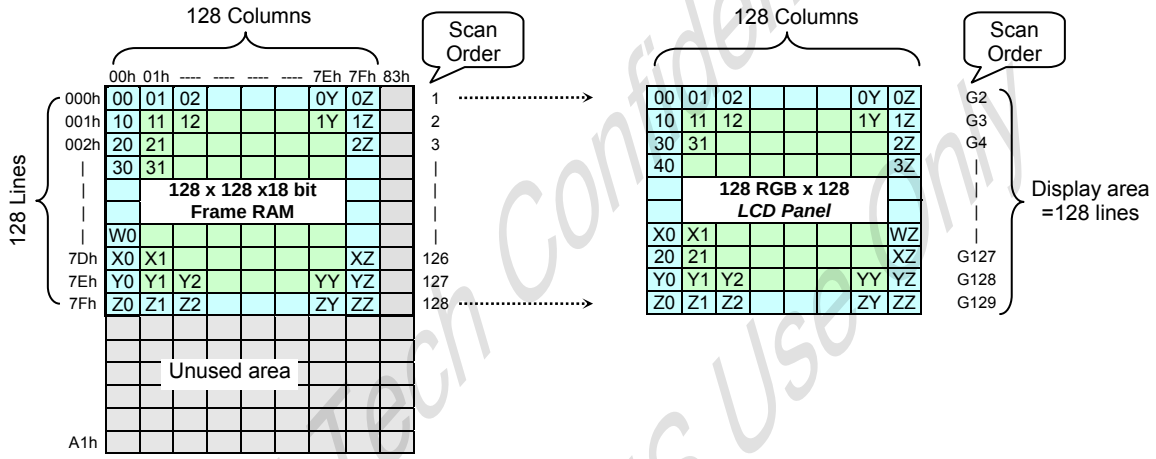
7.5.3.3 When using 128RGB x 128 resolution (GM1, GM0 = “10”)

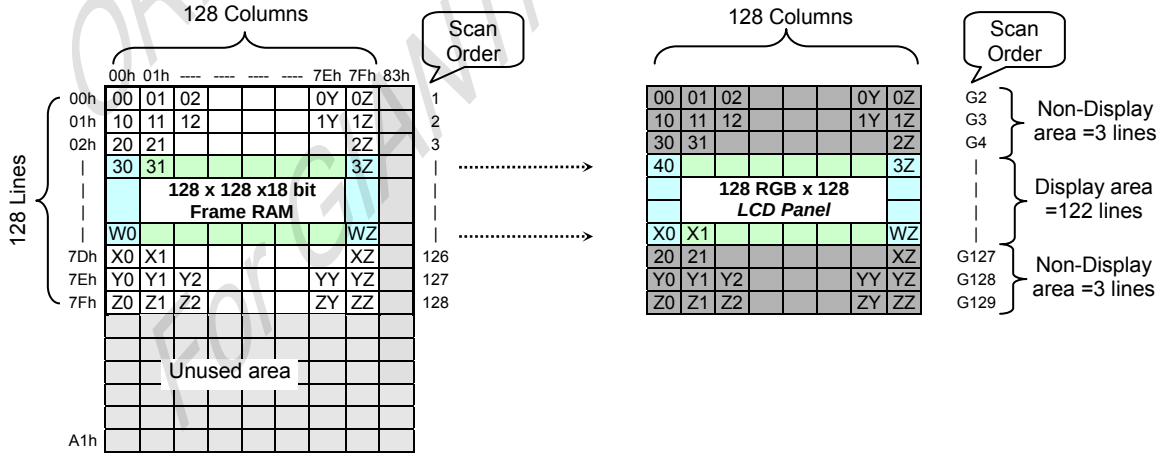
In this mode, contents of the frame memory within an area where column pointer is 00h to 7Fh and page pointer is 000h to 07Fh is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

(1) Example for Normal Display On (MX=MY=ML=’0’ ,SMX=SMY=’0’)



(2) Example for Partial Display On (PSL[7:0]=03h,PEL[7:0]=7Ah, MX=MV=ML=’0’ ,SMX=SMY=’0’)



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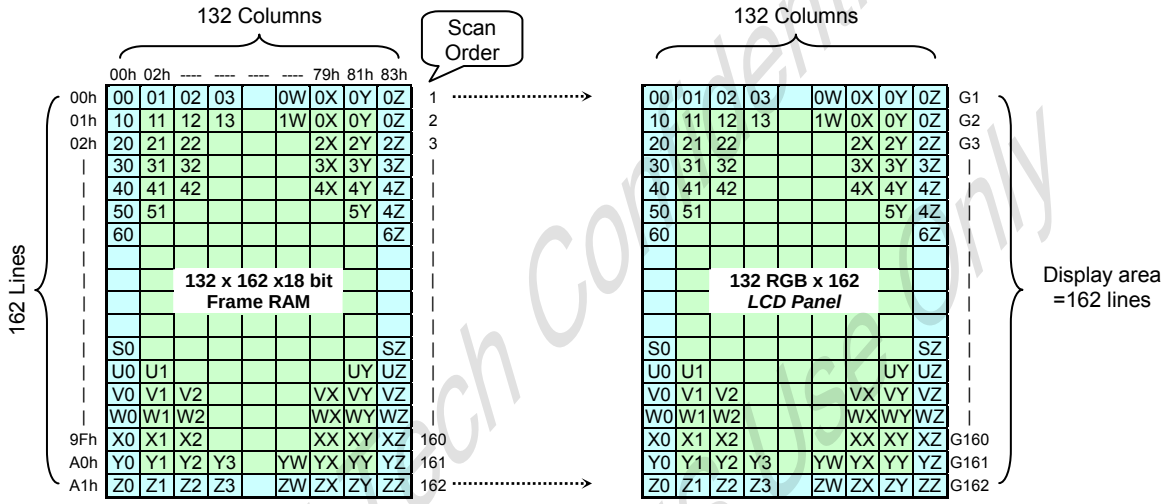
7.5.3.4 When using 132RGB x 162 resolution (GM1, GM0 = "11")

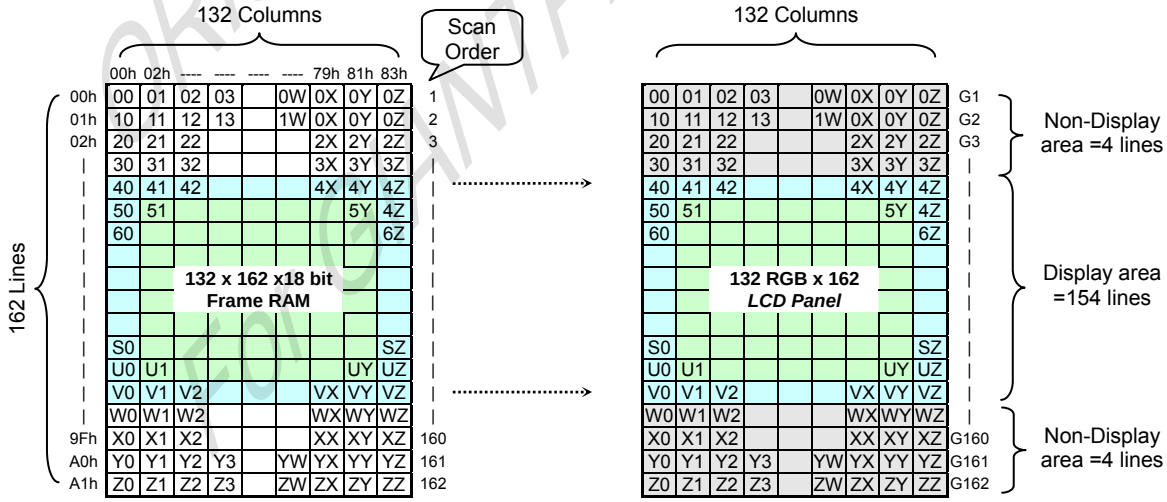
In this mode, contents of the frame memory within an area where column pointer is 00h to 83h and page pointer is 00h to A1h is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

(1) Example for Normal Display On (MX=MY=ML='0' ,SMX=SMY='0')



(2) Example for Partial Display On (PSL[7:0]=04h,PEL[7:0]=9Dh, MX=MV=ML='0' ,SMX=SMY='0')



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7.5.4. Vertical Scroll Mode

There is vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

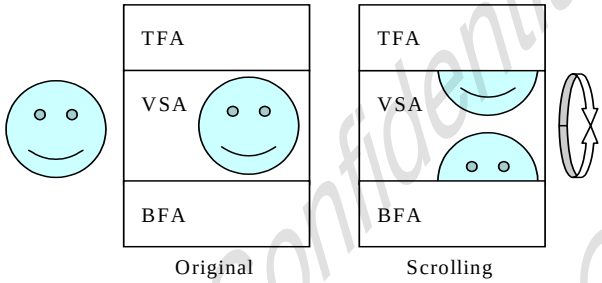

Fig. 7.5.4.1 Difference between Scrolling and original

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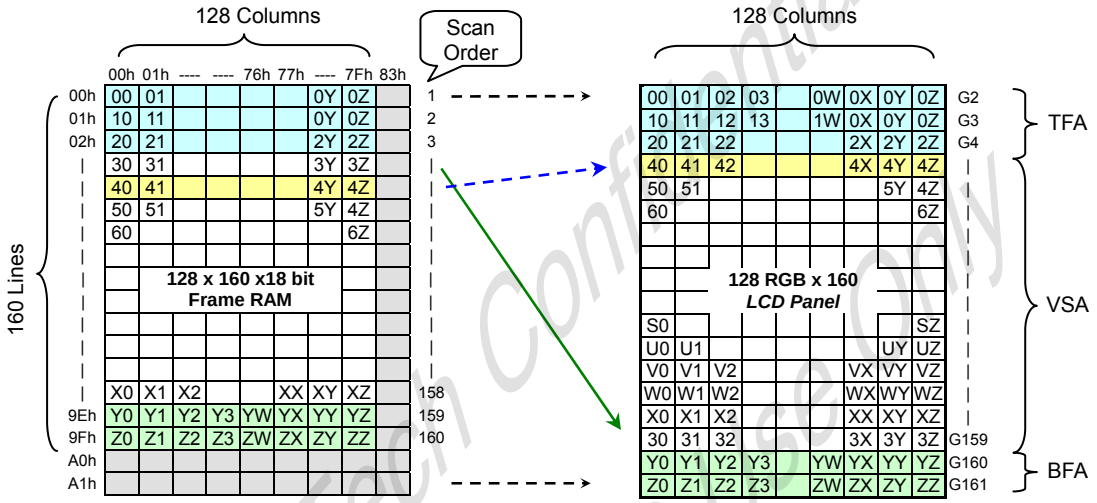
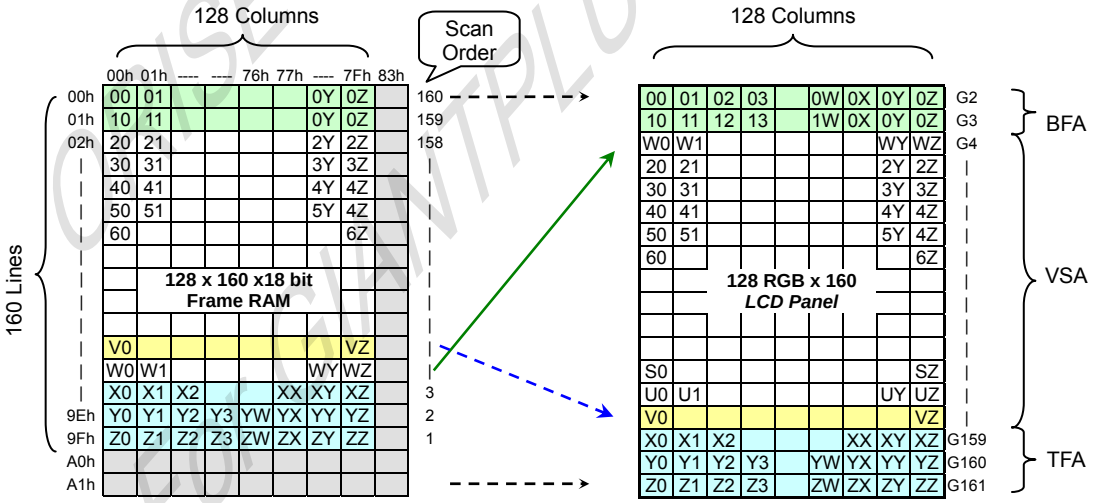
7.5.4.1 When using 128RGB x 160 resolution (GM1, GM0 = “00”)

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=160. In this case, scrolling is applied as shown below.

(1) Example for TFA =3, VSA=155, BFA=2, SSA=4, ML=0: Scrolling



(2) Example for TFA =3, VSA=155, BFA=2, SSA=4, ML=1: Scrolling: TFA and BFT are exchanged



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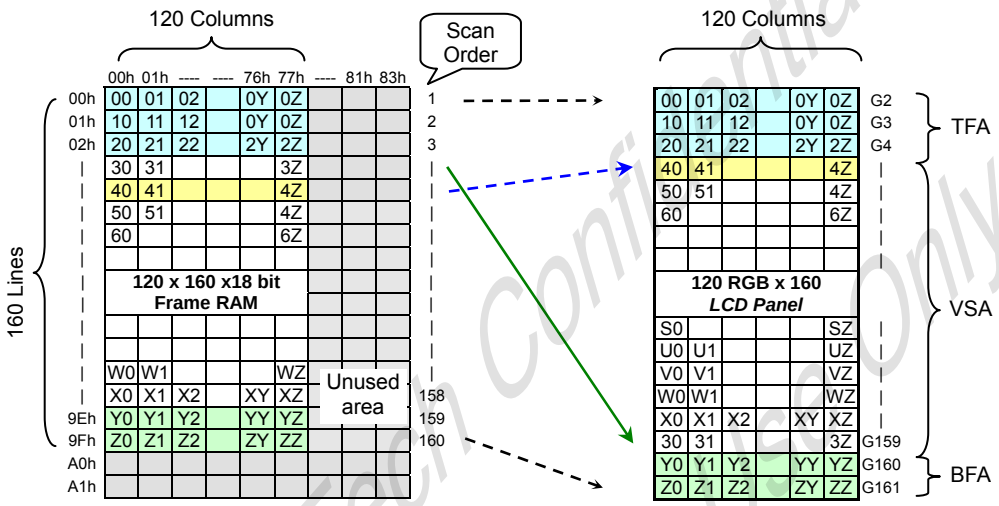
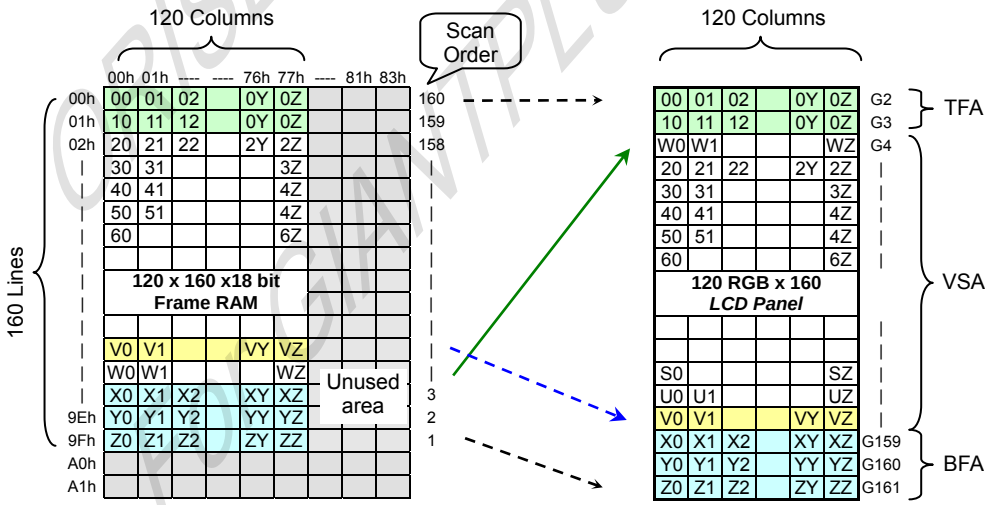
7.5.4.2 When using 120RGB x 160 resolution (GM1, GM0 = "01")

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=160. In this case, scrolling is applied as shown below.

(1) Example for TFA =3, VSA=155, BFA=2, SSA=4, ML=0: Scrolling



(2) Example for TFA =2, VSA=155, BFA=3, SSA=4, ML=1: Scrolling: TFA and BFT are exchanged



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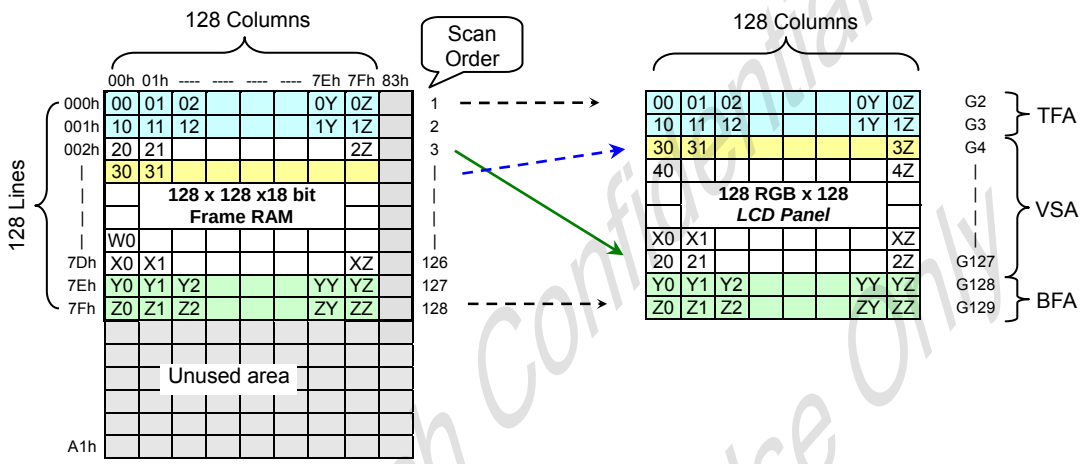
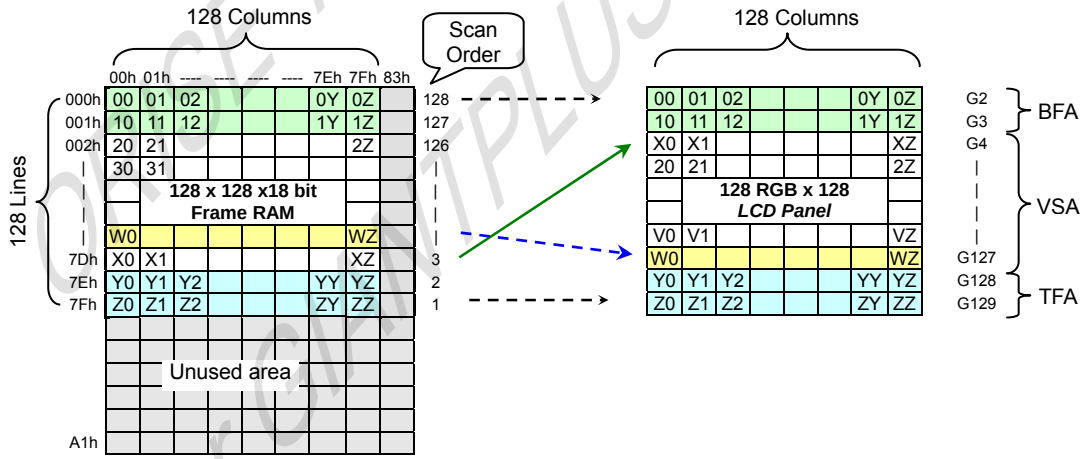
7.5.4.3 When using 128RGB x 128 resolution (GM1, GM0 = “10”)

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=128. In this case, scrolling is applied as shown below.

(1) Example for TFA =2, VSA=124, BFA=2, SSA=3, ML=0: Scrolling



(2) Example for TFA =2, VSA=124, BFA=2, SSA=4, ML=1: Scrolling: TFA and BFT are exchanged



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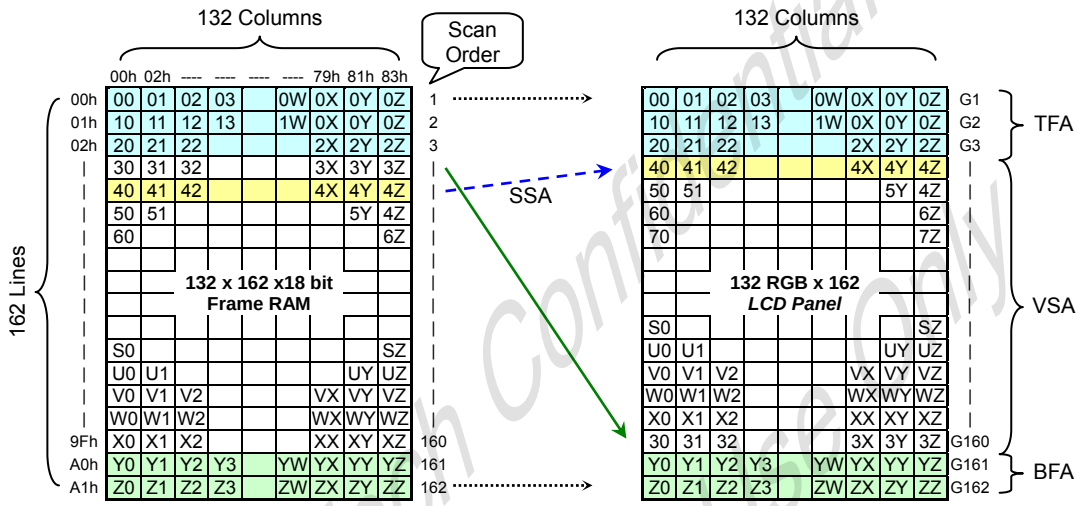
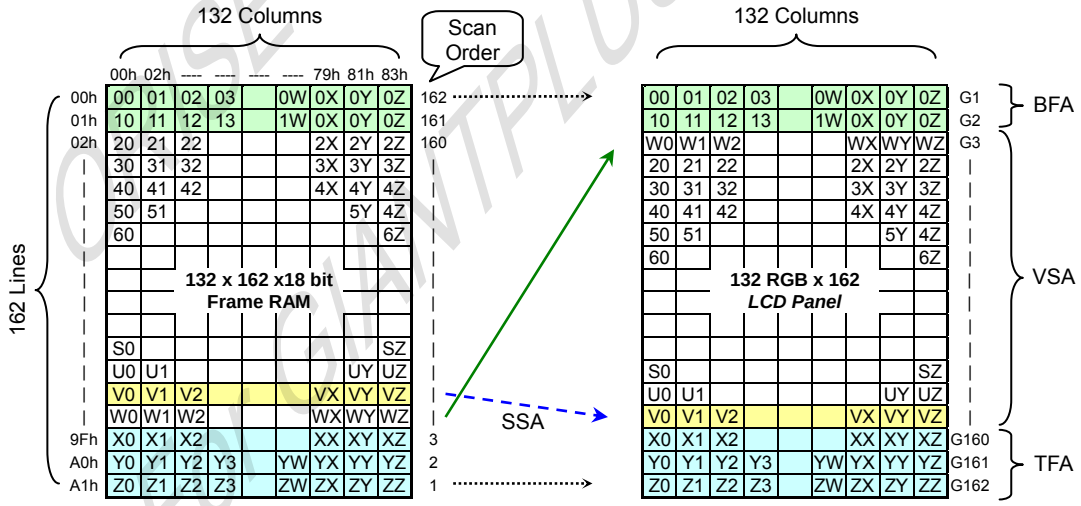
7.5.4.4 When using 132RGB x 162 resolution (GM1, GM0 = "11")

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=162. In this case, scrolling is applied as shown below.

(1) Example for TFA =3, VSA=157, BFA=2, SSA=4, ML=0: Scrolling



(2) Example for TFA =3, VSA=157, BFA=2, SSA=4, ML=1: Scrolling: TFA and BFT are exchanged



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7.5.5. Vertical Scroll Example

7.5.5.1 Vertical Scroll Example (GM1, GM0 = "00" & GM1, GM0="01")

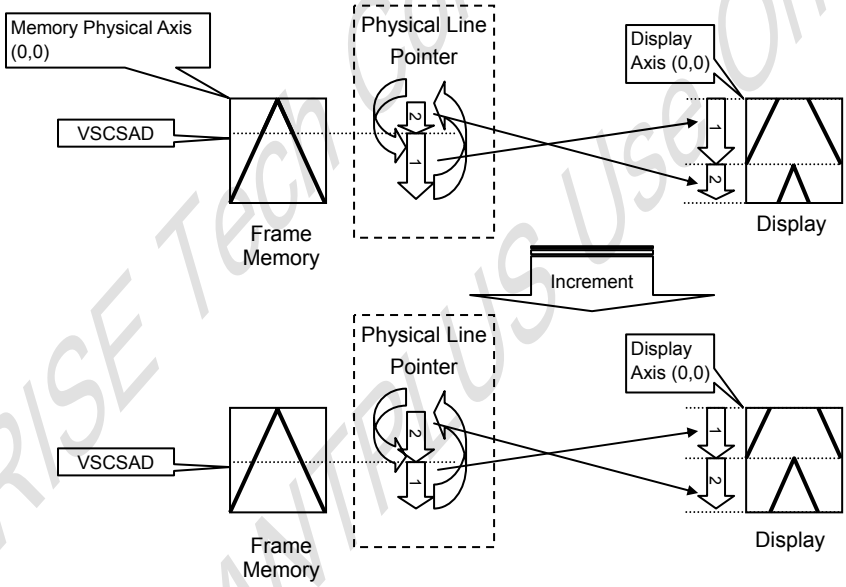
There are 2 types of vertical scrolling, which are determined by the commands " Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

Case 1: TFA + VSA + BFA≠160

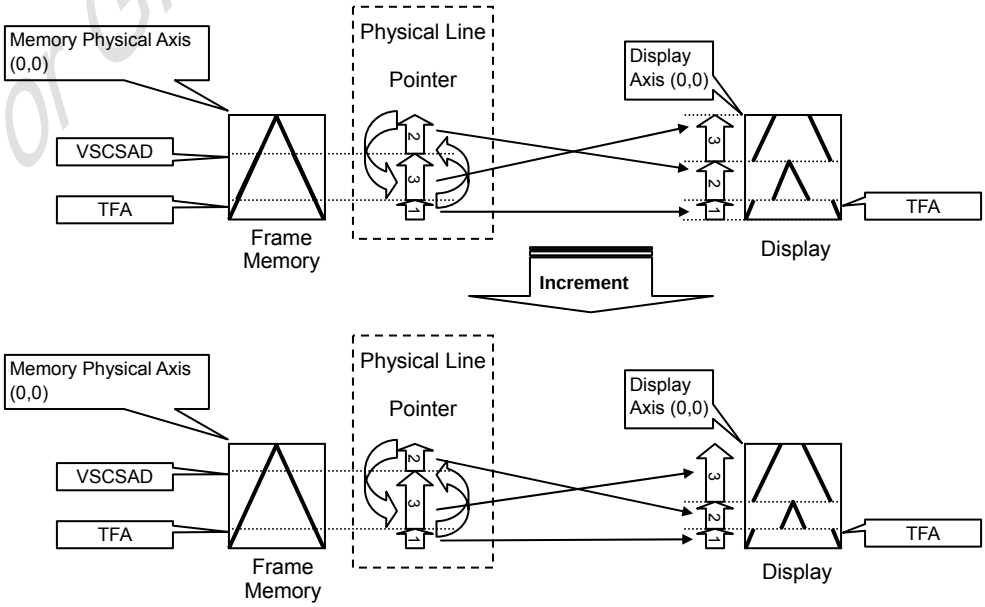
N/A. Do not set TFA + VSA + BFA≠160. In that case, unexpected picture will be shown.

Case 2: TFA + VSA + BFA=160 (Scrolling)

Example1) When MADCTR parameter ML="0", TFA=0, VSA=160, BFA=0 and VSCSAD=80.



Example2) When MADCTR parameter ML="1", TFA=30, VSA=130, BFA=0 and VSCSAD=80.



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7.5.5.2 Vertical Scroll Example (GM1, GM0 = "10")

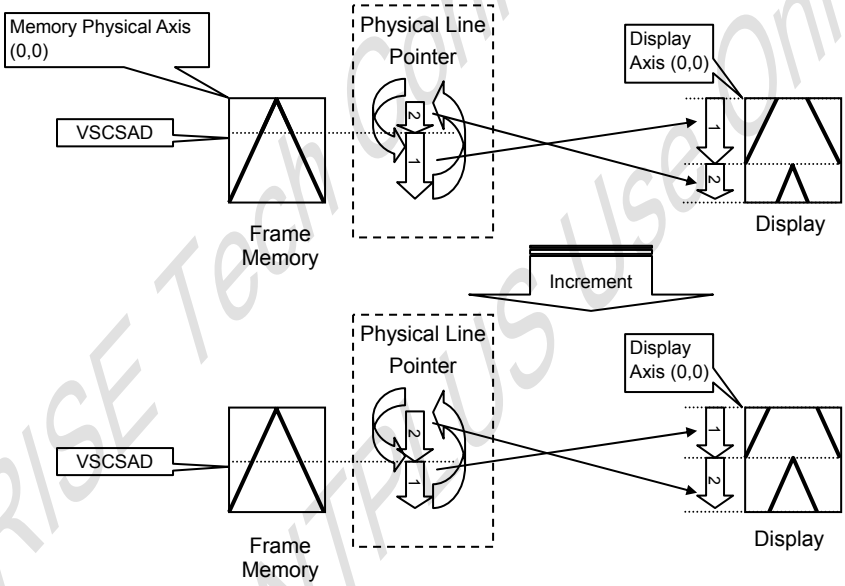
There are 2 types of vertical scrolling, which are determined by the commands " Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

Case 1: TFA + VSA + BFA≠128

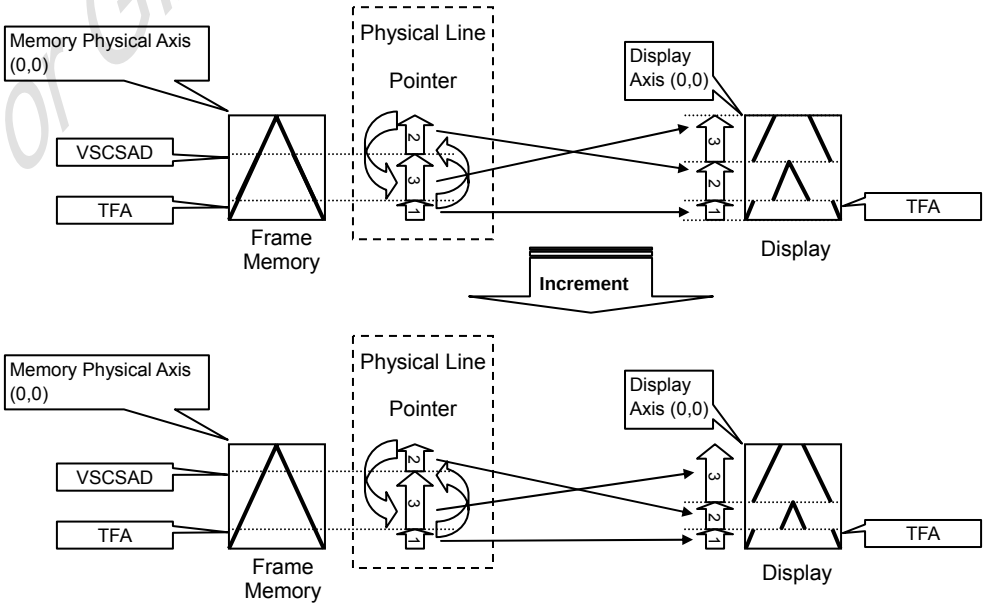
N/A. Do not set TFA + VSA + BFA≠128. In that case, unexpected picture will be shown.

Case 2: TFA + VSA + BFA=128 (Scrolling)

Example1) When MADCTR parameter ML="0", TFA=0, VSA=128, BFA=0 and VSCSAD=40.



Example2) When MADCTR parameter ML="1", TFA=30, VSA=98, BFA=0 and VSCSAD=40.



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7.5.5.3 Vertical Scroll Example (GM1, GM0 = "11")

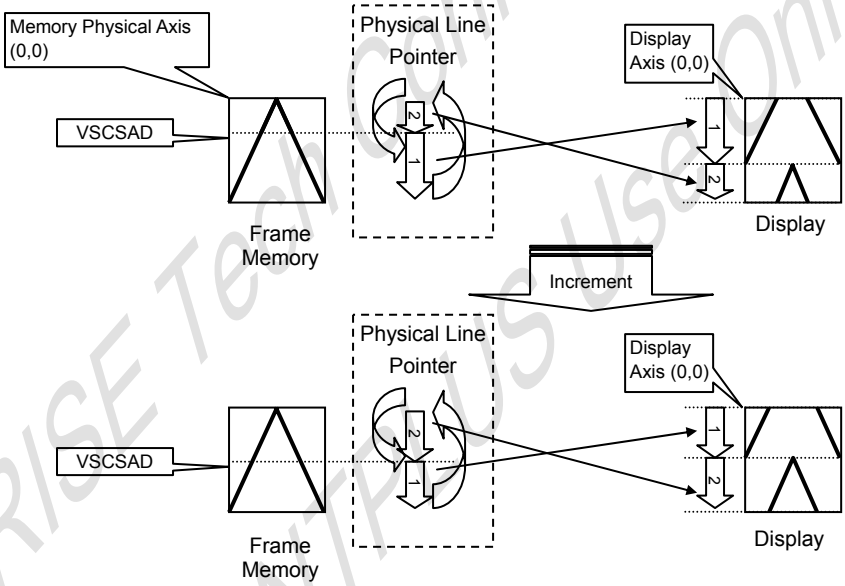
There are 2 types of vertical scrolling, which are determined by the commands " Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

Case 1: TFA + VSA + BFA≠162

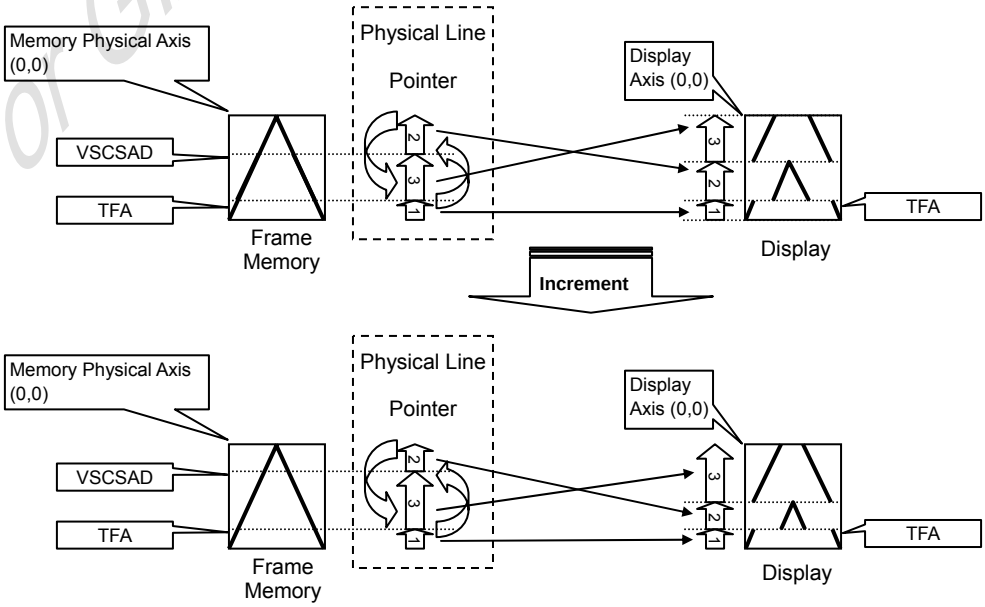
N/A. Do not set TFA + VSA + BFA≠162. In that case, unexpected picture will be shown.

Case 2: TFA + VSA + BFA=162 (Scrolling)

Example1) When MADCTR parameter ML="0", TFA=0, VSA=162, BFA=0 and VSCSAD=40.



Example2) When MADCTR parameter ML="1", TFA=30, VSA=132, BFA=0 and VSCSAD=40.



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7.6. Address Counter

The address counter sets the addresses of the display data RAM for writing and reading.

Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 8-8-8-bit), according to the data formats. As soon as this pixel-data information is complete the "Write access" is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=128 (7Fh) and Y=0 to Y=160 (9Fh). Addresses outside these ranges are not allowed. Before writing to the RAM a window must be defined into which will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=128 (7Fh), YE=160 (9Fh).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands "CASET, RASET" and "MADCTR" , define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Fig. 8.2.3 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data bust be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as Fig. 7.6.1 below:

Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to "Start Column (XS)"	Return to "Start Row (YS)"
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than "End Column (XE)"	Return to "Start Column (XS)"	Increment by 1
The Column counter value is larger than "End Column (XE)" and the Row counter value is larger than "End Row (YE)"	Return to "Start Column (XS)"	Return to "Start Row (YS)"

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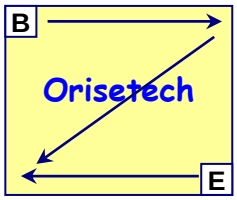
7.7. Memory Data Write/ Read Direction

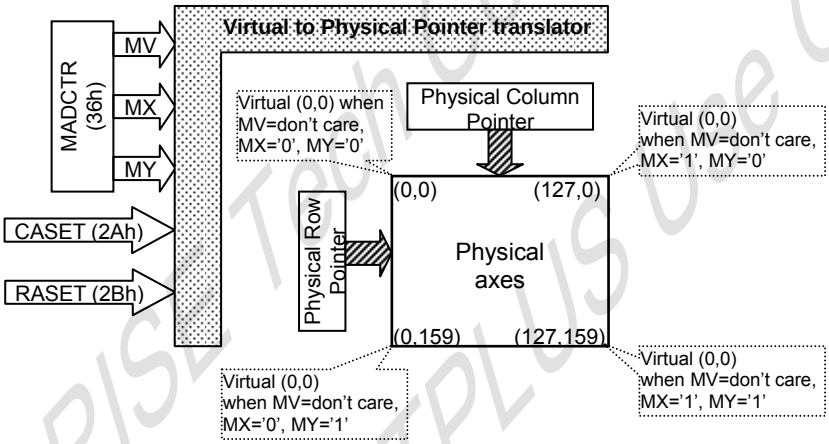
The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by "Memory Data Access Control" Command, bits B5 (MV), B6 (MX), B7 (MY) as described below.



Data Stream order is like in this figure

Fig. 7.7.1 Data streaming order

-When 128RGBx160 (GM='00')



MV	MX	MV	CASET	RASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Row Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (159-Physical Row Pointer)
0	1	0	Direct to (127-Physical Column Pointer)	Direct to Physical Row Pointer
0	1	1	Direct to (127-Physical Column Pointer)	Direct to (159-Physical Row Pointer)
1	0	0	Direct to Physical Row Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (159-Physical Row Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Row Pointer	Direct to (127-Physical Column Pointer)
1	1	1	Direct to (159-Physical Row Pointer)	Direct to (127-Physical Column Pointer)

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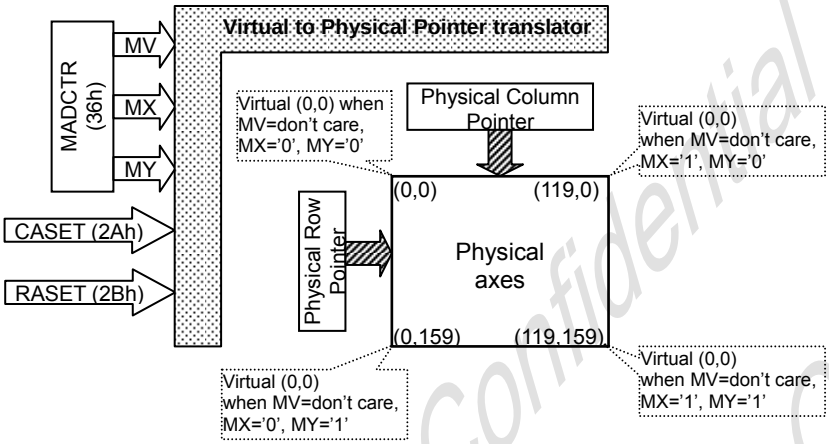
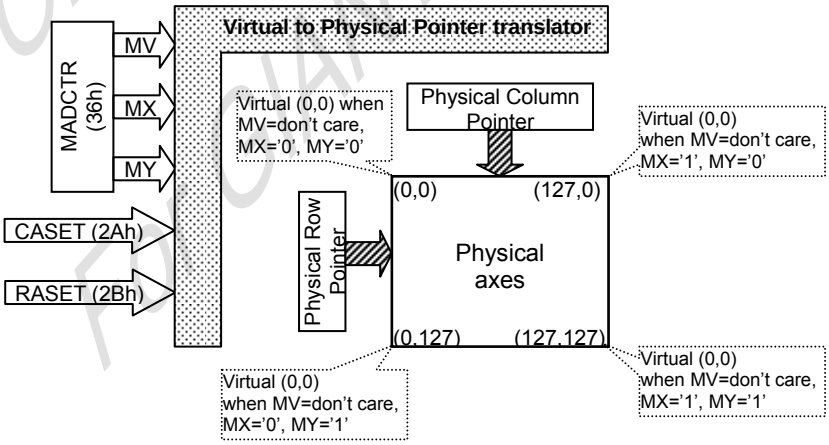
-When 120RGBx160 (GM='01')



MV	MX	MV	CASET	RASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Row Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (159-Physical Row Pointer)
0	1	0	Direct to (119-Physical Column Pointer)	Direct to Physical Row Pointer
0	1	1	Direct to (119-Physical Column Pointer)	Direct to (159-Physical Row Pointer)
1	0	0	Direct to Physical Row Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (159-Physical Row Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Row Pointer	Direct to (119-Physical Column Pointer)
1	1	1	Direct to (159-Physical Row Pointer)	Direct to (119-Physical Column Pointer)

-When 128RGBx128 (GM='10')



MV	MX	MV	CASET	RASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Row Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (127-Physical Row Pointer)
0	1	0	Direct to (127-Physical Column Pointer)	Direct to Physical Row Pointer
0	1	1	Direct to (127-Physical Column Pointer)	Direct to (127-Physical Row Pointer)
1	0	0	Direct to Physical Row Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (127-Physical Row Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Row Pointer	Direct to (127-Physical Column Pointer)
1	1	1	Direct to (127-Physical Row Pointer)	Direct to (127-Physical Column Pointer)

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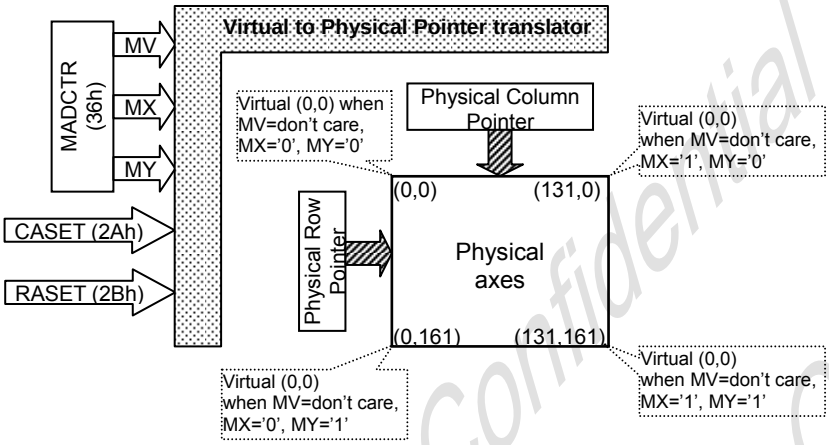
-When 132RGBx162 (GM='11')



MV	MX	MV	CASET	RASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Row Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (161-Physical Row Pointer)
0	1	0	Direct to (131-Physical Column Pointer)	Direct to Physical Row Pointer
0	1	1	Direct to (131-Physical Column Pointer)	Direct to (161-Physical Row Pointer)
1	0	0	Direct to Physical Row Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (161-Physical Row Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Row Pointer	Direct to (131-Physical Column Pointer)
1	1	1	Direct to (161-Physical Row Pointer)	Direct to (131-Physical Column Pointer)

Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7 (MY), B6 (MX), B5 (MV). The write order for each pixel unit is

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

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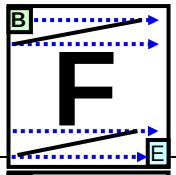
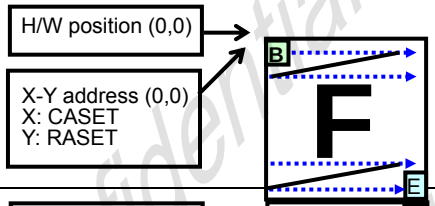
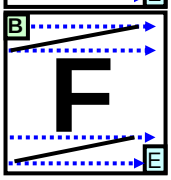
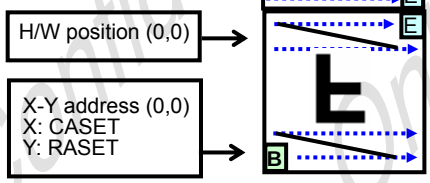
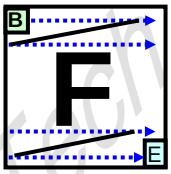
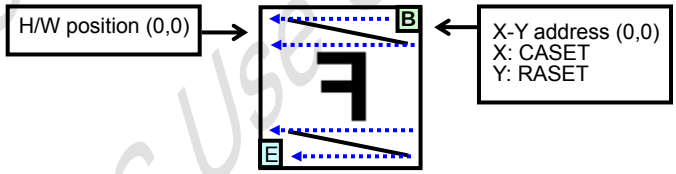
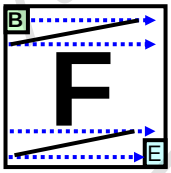
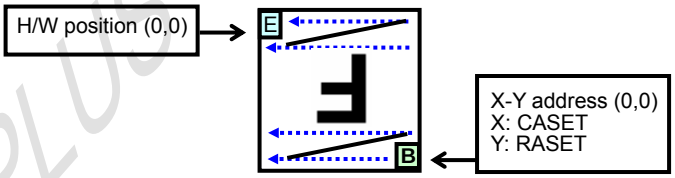
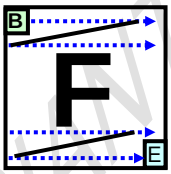
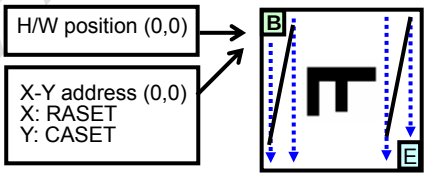
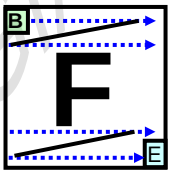
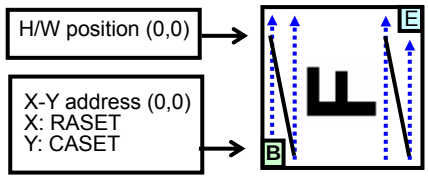
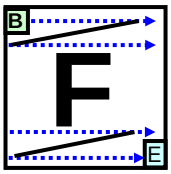
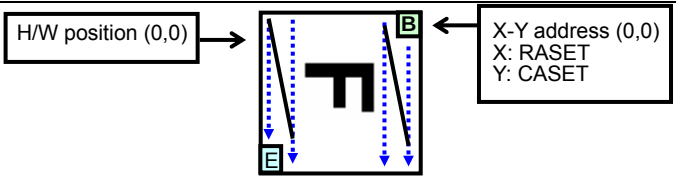
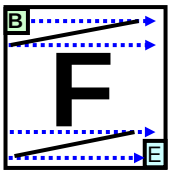
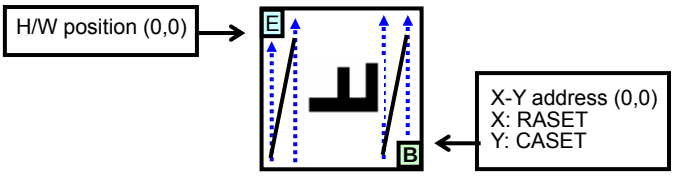
Frame Data Write Direction According to the MADCTR parameters (MV, MX and MY)

Display Data Direction	MADCTR Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

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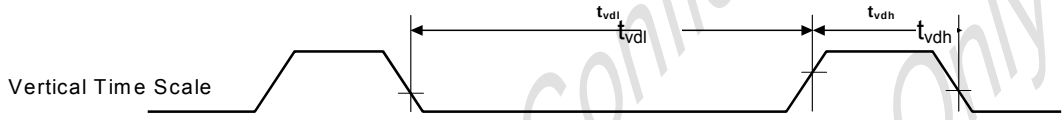
7.8. Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

7.8.1. Tearing Effect Line Modes

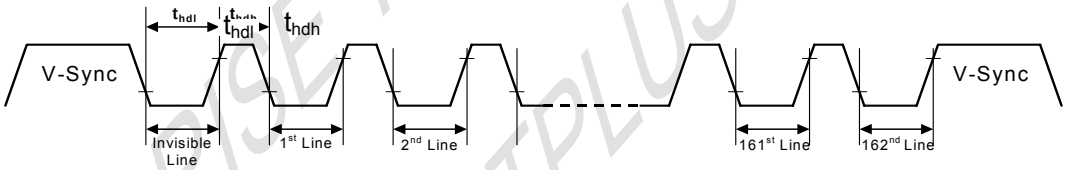
Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:



t_{vdh}= The LCD display is not updated from the Frame Memory

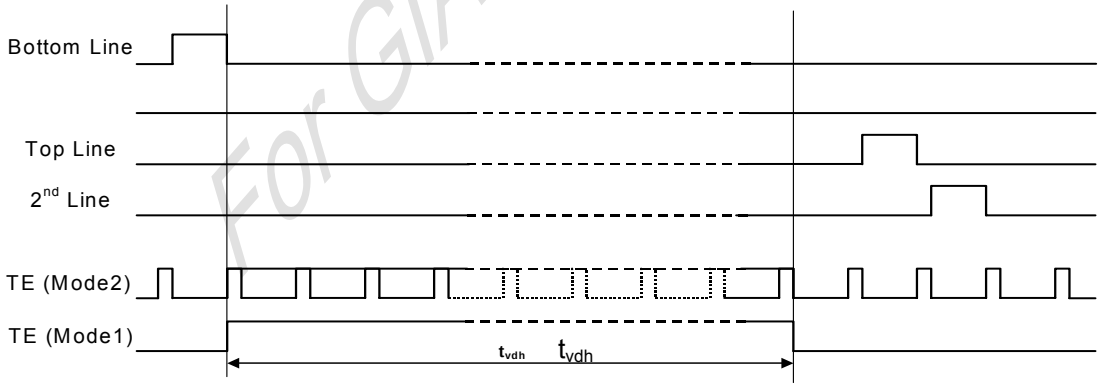
t_{vdl}= The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 162 H-sync pulses per field.



t_{hdh}= The LCD display is not updated from the Frame Memory

t_{hdl}= The LCD display is updated from the Frame Memory (except Invisible Line – see above)



Note: During Sleep In Mode, the Tearing Output Pin is active Low.

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7.8.2. Tearing Effect Line Timings

The Tearing Effect signal is described below:

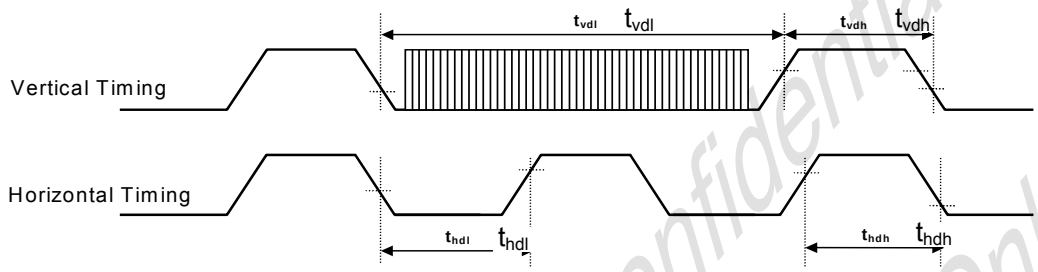

Table 7.8.1 AC characteristics of Tearing Effect Signal Idle Mode Off (Frame Rate = 60 Hz)

Symbol	Parameter	min	max	unit	description
t_{vdl}	Vertical Timing Low Duration	13	-	ms	
t_{vdh}	Vertical Timing High Duration	1000	-	μs	
t_{hdl}	Horizontal Timing Low Duration	33	-	μs	
t_{hdh}	Horizontal Timing High Duration	25	500	μs	

NOTE: The timings in Table 7.8.1 apply when MADCTR ML=0 and ML=1

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

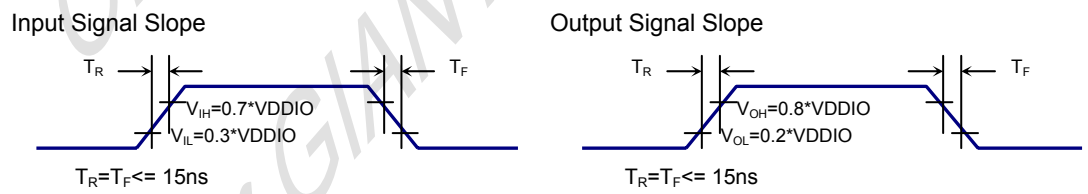

Fig. 7.1.2 Rising and Falling timing for Input and Output signal

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

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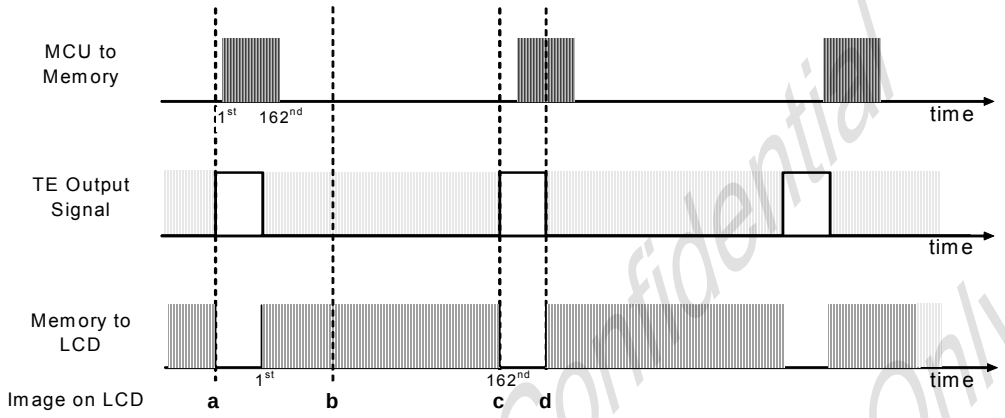
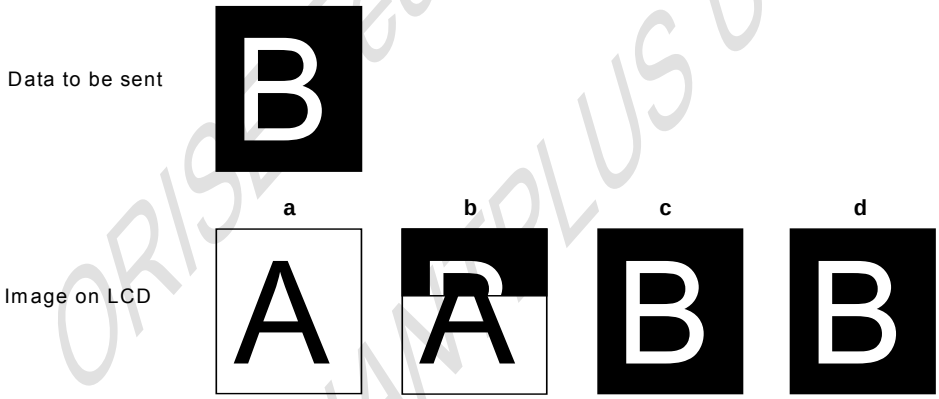
7.8.3. Example 1: MPU Write is faster than panel read.



Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



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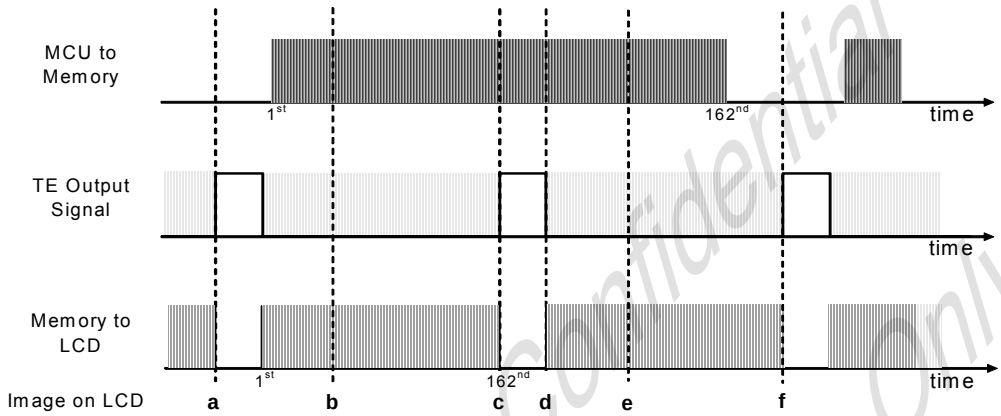
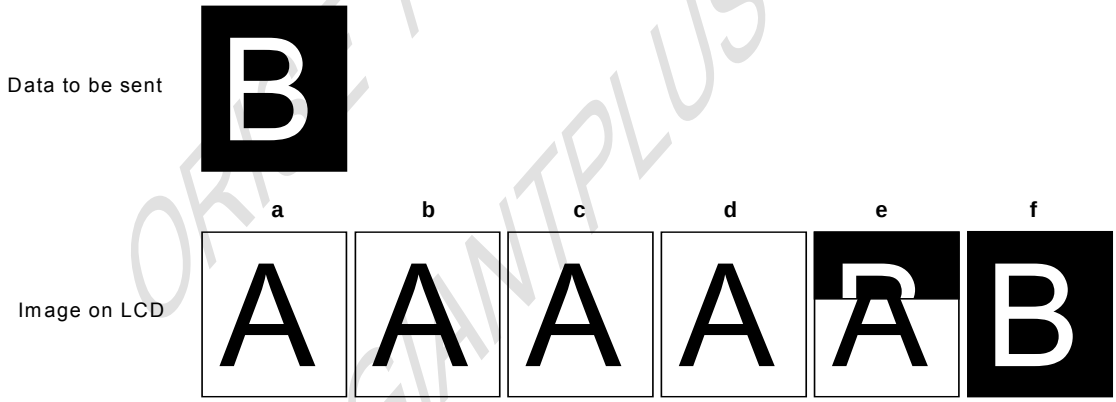
7.8.4. Example 2: MPU write is slower than panel read.



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer "catches" the MPU to Frame memory write position.



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7.9. Preset Values

ORISETECH has already set all preset values in SPFD54124B. Any of these preset values do not need customer's SW support.

7.10. Power ON/OFF Sequence

VDDIO and VDD can be applied in any order.

VDDIO and VDD can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VDD and VDDIO must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDIO or VDD can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

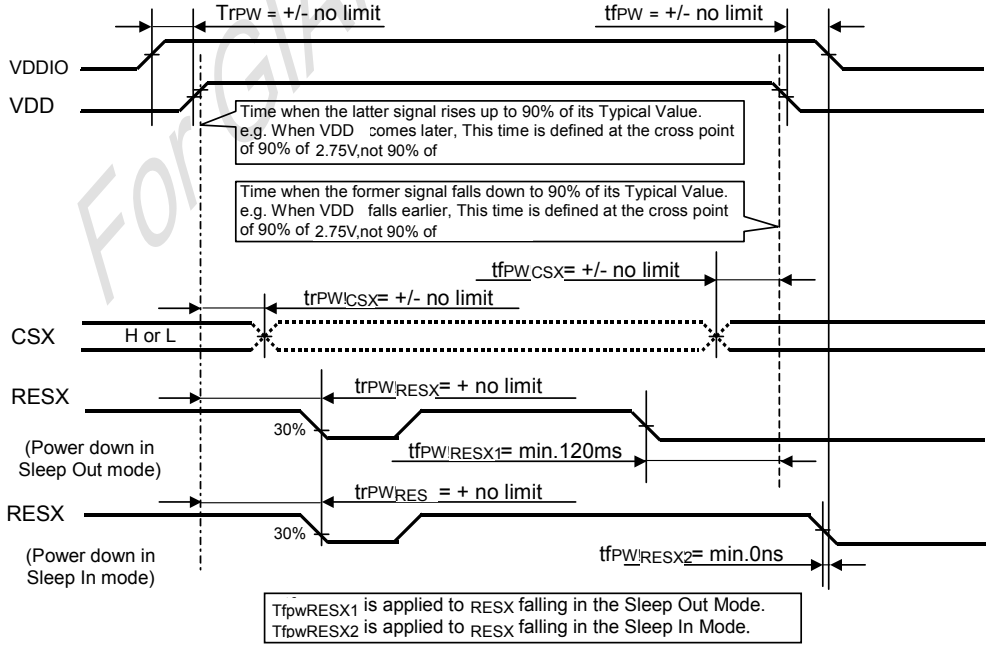
Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

If RESX line is not held stable by host during Power On Sequence, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below:

7.10.1. Case 1 – RESX Line is held High or Unstable by Host at Power On

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDD and VDDIO have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

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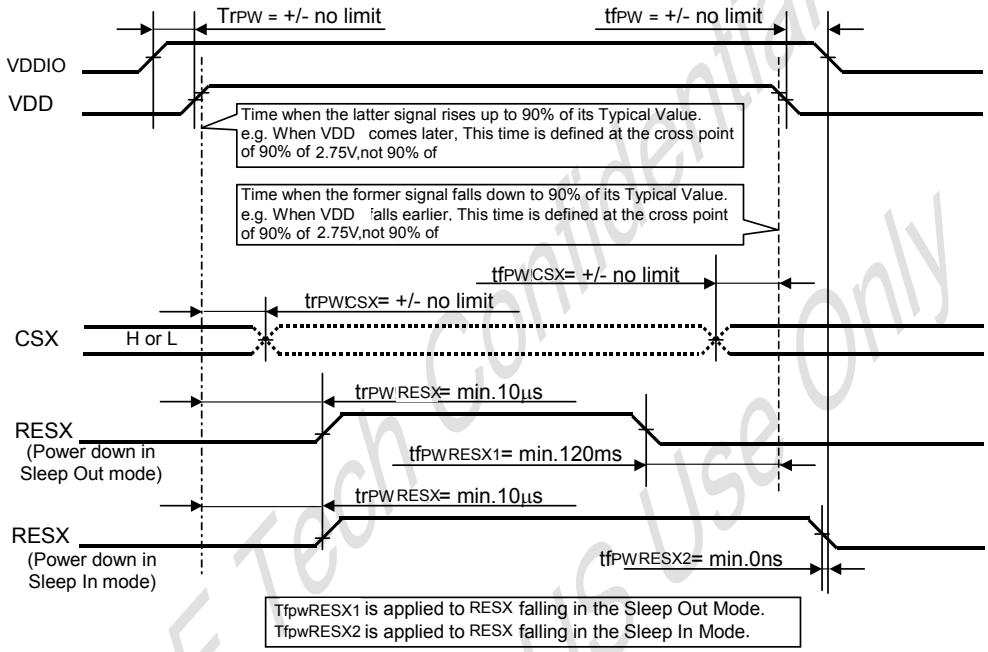
7.10.2. Case 2 – RESX Line is Held Low by Host at Power On

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10μsec after both VDD and VDDIO have been applied.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

7.10.3. Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface.

At an uncontrolled power off the display will go blank and there will not be any visible effects within (TBD) second on the display (blank display) and remains blank until "Power On Sequence" powers it up.

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7.11. Power Level Definition

7.11.1. Power Level

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

In this mode, the display is able to show maximum 262,144 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out.

In this mode part of the display is used with maximum 262,144 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out.

In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode

In this mode, the DC: DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDIO power supply. Contents of the memory are safe.

6. Power Off Mode

In this mode, both VDD and VDDIO are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

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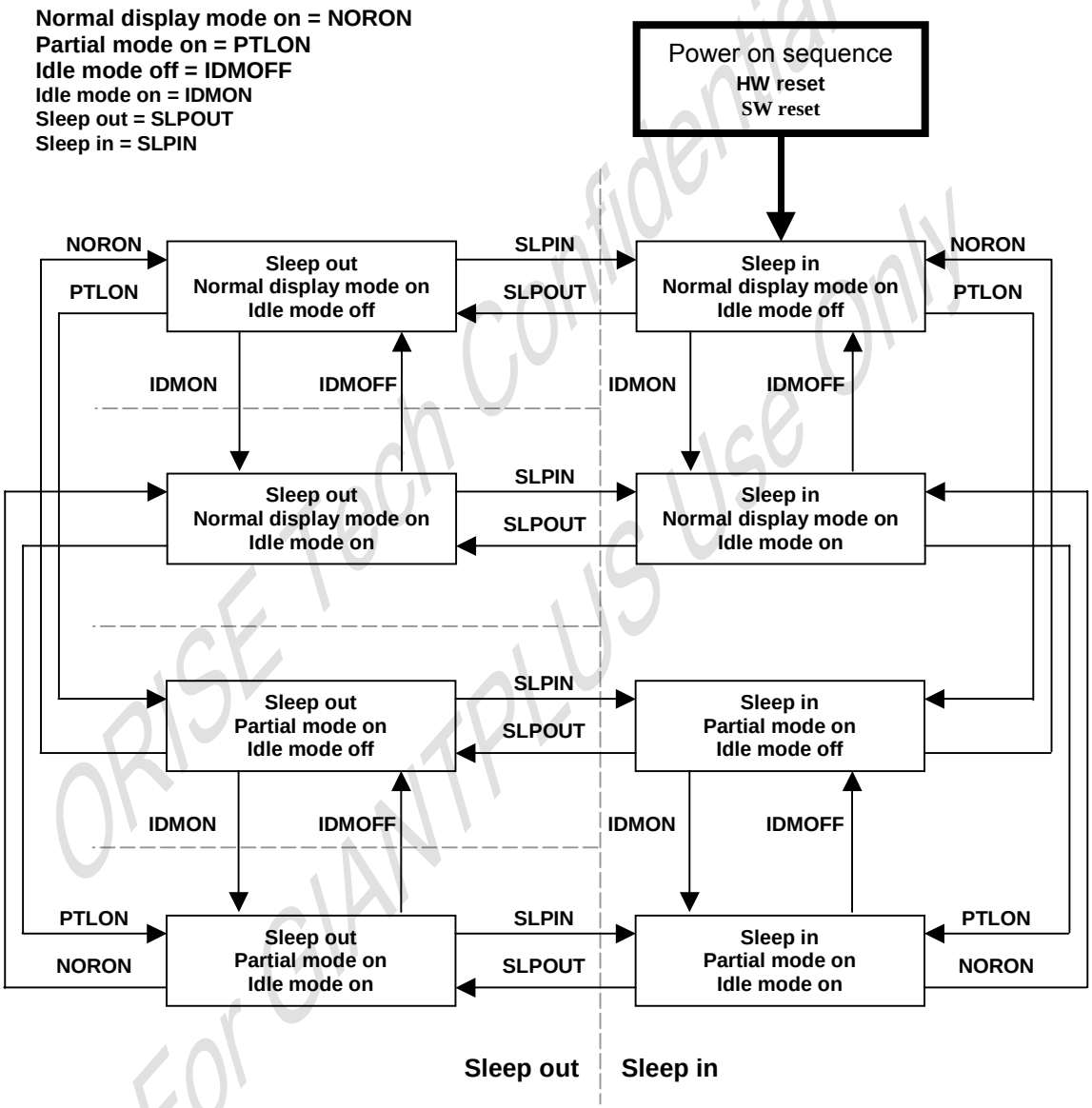
7.11.2. Power Flow Chart



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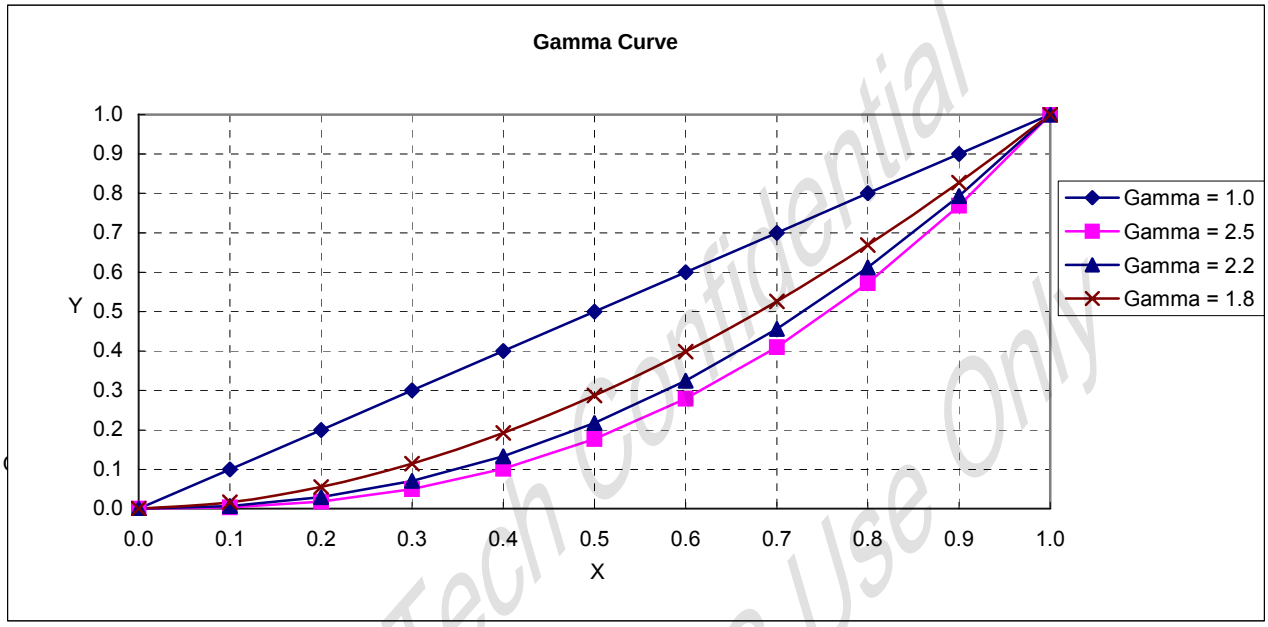
Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by this spec, when there is changing from one power mode to another power mode.

7.12. Gamma Curves



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7.13. Reset

7.13.1. Reset Value

7.13.1.1 Reset Table (Default Value, GM=00, 128RGB x 160)

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address (XS)	0000h	0000h	0000h
Column: End Address (XE)	007Fh	007Fh	007Fh (127d) (when MV=0) 009Fh (159d) (when MV=1)
Row: Start Address (YS)	0000h	0000h	0000h
Row: End Address (YE)	009Fh	009Fh	009Fh (159d) (when MV=0) 007Fh (127d) (when MV=1)
Gamma setting	GC0	GC0	GC0
RGB for 256, 4k and 65k Color Mode	See Section 6.14	See Section 6.14	No Change
Partial: Start Address (PSL)	0000h	0000h	0000h
Partial: End Address (PEL)	009Fh	009Fh	009Fh
Scroll: Vertical scrolling	Off	Off	Off
Scroll: Top Fixed Area (TFA)	0000h	0000h	0000h
Scroll: Scroll Area (VSA)	00A0h	00A0h	00A0h
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address (SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode *3)	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control (MY/MX/MV/ML/RGB)	0/0/0/0/0	0/0/0/0/0	No Change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDPM	08h	08h	08h
RDDMADCTR	00h	00h	No Change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID1	38h	38h	38h
ID2	NV Value	NV Value	NV Value
ID3	NV Value	NV Value	NV Value

Notes 1. There will be no abnormal visible effects on the display when S/W or H/W Reset is applied.

Notes:2. Powered-On Reset finishes within 10μs after both VDD & VDDIO are applied.

Notes:3. TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

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7.13.1.2 Reset Table (GM=01, 120RGB x 160)

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address (XS)	0000h	0000h	0000h
Column: End Address (XE)	0077h	0077h	0077h (119d) (when MV=0) 009Fh (159d) (when MV=1)
Row: Start Address (YS)	0000h	0000h	0000h
Row: End Address (YE)	009Fh	009Fh	009Fh (159d) (when MV=0) 0077h (119d) (when MV=1)
Gamma setting	GC0	GC0	GC0
RGB for 256, 4k and 65k Color Mode	See Section 6.14	See Section 6.14	No Change
Partial: Start Address (PSL)	0000h	0000h	0000h
Partial: End Address (PEL)	009Fh	009Fh	009Fh
Scroll: Vertical scrolling	Off	Off	Off
Scroll: Top Fixed Area (TFA)	0000h	0000h	0000h
Scroll: Scroll Area (VSA)	00A0h	00A0h	00A0h
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address (SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode *3)	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control (MY/MX/MV/ML/RGB)	0/0/0/0/0	0/0/0/0/0	No Change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDPM	08h	08h	08h
RDDMADCTR	00h	00h	No Change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID1	NV Value	NV Value	NV Value
ID2	NV Value	NV Value	NV Value
ID3	NV Value	NV Value	NV Value

Notes 1. There will be no abnormal visible effects on the display when S/W or H/W Reset is applied.

Notes:2. Powered-On Reset finishes within 10µs after both VDD & VDDIO are applied.

Notes:3. TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

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7.13.1.3 Reset Table (GM=10, 128RGB x 128)

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address (XS)	0000h	0000h	0000h
Column: End Address (XE)	007Fh	007Fh	007Fh (127d) (when MV=0) 007Fh (127d) (when MV=1)
Row: Start Address (YS)	0000h	0000h	0000h
Row: End Address (YE)	007Fh	007Fh	007Fh (127d) (when MV=0) 007Fh (127d) (when MV=1)
Gamma setting	GC0	GC0	GC0
RGB for 256, 4k and 65k Color Mode	See Section 6.14	See Section 6.14	No Change
Partial: Start Address (PSL)	0000h	0000h	0000h
Partial: End Address (PEL)	007Fh	007Fh	007Fh
Scroll: Vertical scrolling	Off	Off	Off
Scroll: Top Fixed Area (TFA)	0000h	0000h	0000h
Scroll: Scroll Area (VSA)	0080h	0080h	0080h
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address (SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode *3)	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control (MY/MX/MV/ML/RGB)	0/0/0/0/0	0/0/0/0/0	No Change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDPM	08h	08h	08h
RDDMADCTR	00h	00h	No Change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID1	38h	38h	38h
ID2	NV Value	NV Value	NV Value
ID3	NV Value	NV Value	NV Value

Notes 1. There will be no abnormal visible effects on the display when S/W or H/W Reset is applied.

Notes:2. Powered-On Reset finishes within 10µs after both VDD & VDDIO are applied.

Notes:3. TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

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7.13.1.4 Reset Table (GM=11, 132RGB x 162)

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address (XS)	0000h	0000h	0000h
Column: End Address (XE)	0083h	0083h	0083h (131d) (when MV=0) 00A1h (161d) (when MV=1)
Row: Start Address (YS)	0000h	0000h	0000h
Row: End Address (YE)	00A1h	00A1h	00A1h (161d) (when MV=0) 0083h (131d) (when MV=1)
Gamma setting	GC0	GC0	GC0
RGB for 256, 4k and 65k Color Mode	See Section 6.14	See Section 6.14	No Change
Partial: Start Address (PSL)	0000h	0000h	0000h
Partial: End Address (PEL)	00A1h	00A1h	00A1h
Scroll: Vertical scrolling	Off	Off	Off
Scroll: Top Fixed Area (TFA)	0000h	0000h	0000h
Scroll: Scroll Area (VSA)	00A2h	00A2h	00A2h
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address (SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode *3)	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control (MY/MX/MV/ML/RGB)	0/0/0/0/0	0/0/0/0/0	No Change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDPM	08h	08h	08h
RDDMADCTR	00h	00h	No Change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID1	38h	38h	38h
ID2	NV Value	NV Value	NV Value
ID3	NV Value	NV Value	NV Value

Notes 1. There will be no abnormal visible effects on the display when S/W or H/W Reset is applied.

Notes:2. Powered-On Reset finishes within 10µs after both VDD & VDDIO are applied.

Notes:3. TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

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7.13.2. Module Input/Output Pins

7.13.2.1 Output or Bi-directional (I/O) Pins

Output or Bi-directional pins	After Power On	After Hardware Reset	After Software Reset
TE	Low	Low	Low
D7 to D0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)

Note: There will be no output from D7-D0 during Power On/Off sequence, Hardware Reset and Software Reset.

7.13.2.2 Input Pins

Input pins	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
RESX	See 6.10	Input valid	Input valid	Input valid	See 6.10
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D7 to D0	Input invalid	Input valid	Input valid	Input valid	Input invalid
P/SX	Input invalid	Input valid	Input valid	Input valid	Input invalid

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7.13.3. Reset Timing

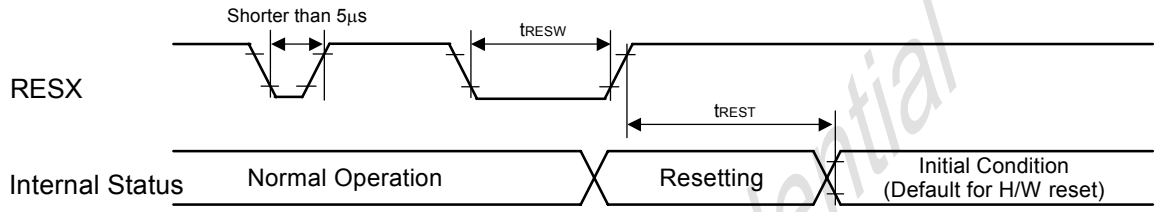


Table 7.13.3.1 Reset input timing

VSS=0V, VDDIO=1.6V to 3.6V, VDD=2.6V to 3.6V,Ta = -30 to 70°C)

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	μs
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

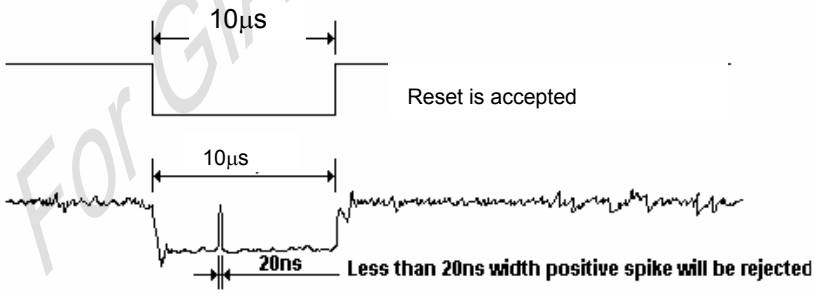
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 10μs	Reset
Between 5μs and 10μs	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, ID2 and VCOMOF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

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7.14. Colour Depth Conversion Look Up Tables

7.14.1. 4096 and 65536 Colour to 262,144 Colour

Colour	Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W Reset		RGBSET Parameter	Look Up Table Input Data	
		4k Colour	65k Colour		4k Colour	65k Colour
RED	$R_{005}R_{004}$ R_{003} R_{002} R_{001} R_{000}	000000	000000	1	0000	00000
	$R_{015}R_{014}$ R_{013} R_{012} R_{011} R_{010}	000100	000010	2	0001	00001
	$R_{025}R_{024}$ R_{023} R_{022} R_{021} R_{020}	001000	000100	3	0010	00010
	$R_{035}R_{034}$ R_{033} R_{032} R_{031} R_{030}	001100	000110	4	0011	00011
	$R_{045}R_{044}$ R_{043} R_{042} R_{041} R_{040}	010001	001000	5	0100	00100
	$R_{055}R_{054}$ R_{053} R_{052} R_{051} R_{050}	010101	001010	6	0101	00101
	$R_{065}R_{064}$ R_{063} R_{062} R_{061} R_{060}	011001	001100	7	0110	00110
	$R_{075}R_{074}$ R_{073} R_{072} R_{071} R_{070}	011101	001110	8	0111	00111
	$R_{085}R_{084}$ R_{083} R_{082} R_{081} R_{080}	100010	010000	9	1000	01000
	$R_{095}R_{094}$ R_{093} R_{092} R_{091} R_{090}	100110	010010	10	1001	01001
	$R_{105}R_{104}$ R_{103} R_{102} R_{101} R_{100}	101010	010100	11	1010	01010
	$R_{115}R_{114}$ R_{113} R_{112} R_{111} R_{110}	101110	010110	12	1011	01011
	$R_{125}R_{124}$ R_{123} R_{122} R_{121} R_{120}	110011	011000	13	1100	01100
	$R_{135}R_{134}$ R_{133} R_{132} R_{131} R_{130}	110111	011010	14	1101	01101
	$R_{145}R_{144}$ R_{143} R_{142} R_{141} R_{140}	111011	011100	15	1110	01110
	$R_{155}R_{154}$ R_{153} R_{152} R_{151} R_{150}	111111	011110	16	1111	01111
	$R_{165}R_{164}$ R_{163} R_{162} R_{161} R_{160}	Not Used	100001	17	Not Used	10000
	$R_{175}R_{174}$ R_{173} R_{172} R_{171} R_{170}		100011	18		10001
	$R_{185}R_{184}$ R_{183} R_{182} R_{181} R_{180}		100101	19		10010
	$R_{195}R_{194}$ R_{193} R_{192} R_{191} R_{190}		100111	20		10011
	$R_{205}R_{204}$ R_{203} R_{202} R_{201} R_{200}		101001	21		10100
	$R_{215}R_{214}$ R_{213} R_{212} R_{211} R_{210}		101011	22		10101
	$R_{225}R_{224}$ R_{223} R_{222} R_{221} R_{220}		101101	23		10110
	$R_{235}R_{234}$ R_{233} R_{232} R_{231} R_{230}		101111	24		10111
	$R_{245}R_{244}$ R_{243} R_{242} R_{241} R_{240}		110001	25		11000
	$R_{255}R_{254}$ R_{253} R_{252} R_{251} R_{250}		110011	26		11001
	$R_{265}R_{264}$ R_{263} R_{262} R_{261} R_{260}		110101	27		11010
	$R_{275}R_{274}$ R_{273} R_{272} R_{271} R_{270}		110111	28		11011
	$R_{285}R_{284}$ R_{283} R_{282} R_{281} R_{280}		111001	29		11100
	$R_{295}R_{294}$ R_{293} R_{292} R_{291} R_{290}		111011	30		11101
	$R_{305}R_{304}$ R_{303} R_{302} R_{301} R_{300}		111101	31		11110
	$R_{315}R_{314}$ R_{313} R_{312} R_{311} R_{310}		111111	32		11111

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Colour	Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W Reset		RGBSET Parameter	Look Up Table Input Data	
		4k Colour	65k Colour		4k Colour	65k Colour
GREEN	G_{005} G_{004} G_{003} G_{002} G_{001} G_{000}	000000	000000	33	0000	000000
	G_{015} G_{014} G_{013} G_{012} G_{011} G_{010}	000100	000001	34	0001	000001
	G_{025} G_{024} G_{023} G_{022} G_{021} G_{020}	001000	000010	35	0010	000010
	G_{035} G_{034} G_{033} G_{032} G_{031} G_{030}	001100	000011	36	0011	000011
	G_{045} G_{044} G_{043} G_{042} G_{041} G_{040}	010001	000100	37	0100	000100
	G_{055} G_{054} G_{053} G_{052} G_{051} G_{050}	010101	000101	38	0101	000101
	G_{065} G_{064} G_{063} G_{062} G_{061} G_{060}	011001	000110	39	0110	000110
	G_{075} G_{074} G_{073} G_{072} G_{071} G_{070}	011101	000111	40	0111	000111
	G_{085} G_{084} G_{083} G_{082} G_{081} G_{080}	100010	001000	41	1000	001000
	G_{095} G_{094} G_{093} G_{092} G_{091} G_{090}	100110	001001	42	1001	001001
	G_{105} G_{104} G_{103} G_{102} G_{101} G_{100}	101010	001010	43	1010	001010
	G_{115} G_{114} G_{113} G_{112} G_{111} G_{110}	101110	001011	44	1011	001011
	G_{125} G_{124} G_{123} G_{122} G_{121} G_{120}	110011	001100	45	1100	001100
	G_{135} G_{134} G_{133} G_{132} G_{131} G_{130}	110111	001101	46	1101	001101
	G_{145} G_{144} G_{143} G_{142} G_{141} G_{140}	111011	001110	47	1110	001110
	G_{155} G_{154} G_{153} G_{152} G_{151} G_{150}	111111	001111	48	1111	001111
	G_{165} G_{164} G_{163} G_{162} G_{161} G_{160}	Not Used	010000	49	Not Used	010000
	G_{175} G_{174} G_{173} G_{172} G_{171} G_{170}		010001	50		010001
	G_{185} G_{184} G_{183} G_{182} G_{181} G_{180}		010010	51		010010
	G_{195} G_{194} G_{193} G_{192} G_{191} G_{190}		010011	52		010011
	G_{205} G_{204} G_{203} G_{202} G_{201} G_{200}		010100	53		010100
	G_{215} G_{214} G_{213} G_{212} G_{211} G_{210}		010101	54		010101
	G_{225} G_{224} G_{223} G_{222} G_{221} G_{220}		010110	55		010110
	G_{235} G_{234} G_{233} G_{232} G_{231} G_{230}		010111	56		010111
	G_{245} G_{244} G_{243} G_{242} G_{241} G_{240}		011000	57		011000
	G_{255} G_{254} G_{253} G_{252} G_{251} G_{250}		011001	58		011001
	G_{265} G_{264} G_{263} G_{262} G_{261} G_{260}		011010	59		011010
	G_{275} G_{274} G_{273} G_{272} G_{271} G_{270}		011011	60		011011
	G_{285} G_{284} G_{283} G_{282} G_{281} G_{280}		011100	61		011100
	G_{295} G_{294} G_{293} G_{292} G_{291} G_{290}		011101	62		011101
	G_{305} G_{304} G_{303} G_{302} G_{301} G_{300}		011110	63		011110
	G_{315} G_{314} G_{313} G_{312} G_{311} G_{310}		011111	64		011111

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Colour	Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W Reset		RGBSET parameter	Look Up Table Input Data	
		4k Colour	65k Colour		4k Colour	65k Colour
GREEN	G_{325} G_{324} G_{323} G_{322} G_{321} G_{320}	Not Used	100000	65	Not Used	100000
	G_{335} G_{334} G_{333} G_{332} G_{331} G_{330}		100001	66		100001
	G_{345} G_{344} G_{343} G_{342} G_{341} G_{340}		100010	67		100010
	G_{355} G_{354} G_{353} G_{352} G_{351} G_{350}		100011	68		100011
	G_{365} G_{364} G_{363} G_{362} G_{361} G_{360}		100100	69		100100
	G_{375} G_{374} G_{373} G_{372} G_{371} G_{370}		100101	70		100101
	G_{385} G_{384} G_{383} G_{382} G_{381} G_{380}		100110	71		100110
	G_{395} G_{394} G_{393} G_{392} G_{391} G_{390}		100111	72		100111
	G_{405} G_{404} G_{403} G_{402} G_{401} G_{400}		101000	73		101000
	G_{415} G_{414} G_{413} G_{412} G_{411} G_{410}		101001	74		101001
	G_{425} G_{424} G_{423} G_{422} G_{421} G_{420}		101010	75		101010
	G_{435} G_{434} G_{433} G_{432} G_{431} G_{430}		101011	76		101011
	G_{445} G_{444} G_{443} G_{442} G_{441} G_{440}		101100	77		101100
	G_{455} G_{454} G_{453} G_{452} G_{451} G_{450}		101101	78		101101
	G_{465} G_{464} G_{463} G_{462} G_{461} G_{460}		101110	79		101110
	G_{475} G_{474} G_{473} G_{472} G_{471} G_{470}		101111	80		101111
	G_{485} G_{484} G_{483} G_{482} G_{481} G_{480}		110000	81		110000
	G_{495} G_{494} G_{493} G_{492} G_{491} G_{490}		110001	82		110001
	G_{505} G_{504} G_{503} G_{502} G_{501} G_{500}		110010	83		110010
	G_{515} G_{514} G_{513} G_{512} G_{511} G_{510}		110011	84		110011
	G_{525} G_{524} G_{523} G_{522} G_{521} G_{520}		110100	85		110100
	G_{535} G_{534} G_{533} G_{532} G_{531} G_{530}		110101	86		110101
	G_{545} G_{544} G_{543} G_{542} G_{541} G_{540}		110110	87		110110
	G_{555} G_{554} G_{553} G_{552} G_{551} G_{550}		110111	88		110111
	G_{565} G_{564} G_{563} G_{562} G_{561} G_{560}		111000	89		111000
	G_{575} G_{574} G_{573} G_{572} G_{571} G_{570}		111001	90		111001
	G_{585} G_{584} G_{583} G_{582} G_{581} G_{580}		111010	91		111010
	G_{595} G_{594} G_{593} G_{592} G_{591} G_{590}		111011	92		111011
	G_{605} G_{604} G_{603} G_{602} G_{601} G_{600}		111100	93		111100
	G_{615} G_{614} G_{613} G_{612} G_{611} G_{610}		111101	94		111101
	G_{625} G_{624} G_{623} G_{622} G_{621} G_{620}		111110	95		111110
	G_{635} G_{634} G_{633} G_{632} G_{631} G_{630}		111111	96		111111

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Colour	Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W Reset		RGBSET parameter	Look Up Table Input Data	
		4k Colour	65k Colour		4k Colour	65k Colour
BLUE	$B_{005}B_{004}$ B_{003} B_{002} B_{001} B_{000}	000000	000000	97	0000	00000
	$B_{015}B_{014}$ B_{013} B_{012} B_{011} B_{010}	000100	000011	98	0001	00001
	$B_{025}B_{024}$ B_{023} B_{022} B_{021} B_{020}	001000	000101	99	0010	00010
	$B_{035}B_{034}$ B_{033} B_{032} B_{031} B_{030}	001100	000111	100	0011	00011
	$B_{045}B_{044}$ B_{043} B_{042} B_{041} B_{040}	010001	001001	101	0100	00100
	$B_{055}B_{054}$ B_{053} B_{052} B_{051} B_{050}	010101	001011	102	0101	00101
	$B_{065}B_{064}$ B_{063} B_{062} B_{061} B_{060}	011001	001101	103	0110	00110
	$B_{075}B_{074}$ B_{073} B_{072} B_{071} B_{070}	011101	001111	104	0111	00111
	$B_{085}B_{084}$ B_{083} B_{082} B_{081} B_{080}	100010	010001	105	1000	01000
	$B_{095}B_{094}$ B_{093} B_{092} B_{091} B_{090}	100110	010011	106	1001	01001
	$B_{105}B_{104}$ B_{103} B_{102} B_{101} B_{100}	101010	010101	107	1010	01010
	$B_{115}B_{114}$ B_{113} B_{112} B_{111} B_{110}	101110	010111	108	1011	01011
	$B_{125}B_{124}$ B_{123} B_{122} B_{121} B_{120}	110011	011001	109	1100	01100
	$B_{135}B_{134}$ B_{133} B_{132} B_{131} B_{130}	110111	011011	110	1101	01101
	$B_{145}B_{144}$ B_{143} B_{142} B_{141} B_{140}	111011	011101	111	1110	01110
	$B_{155}B_{154}$ B_{153} B_{152} B_{151} B_{150}	111111	011111	112	1111	01111
	$B_{165}B_{164}$ B_{163} B_{162} B_{161} B_{160}	Not Used	100001	113	Not Used	10000
	$B_{175}B_{174}$ B_{173} B_{172} B_{171} B_{170}		100011	114		10001
	$B_{185}B_{184}$ B_{183} B_{182} B_{181} B_{180}		100101	115		10010
	$B_{195}B_{194}$ B_{193} B_{192} B_{191} B_{190}		100111	116		10011
	$B_{205}B_{204}$ B_{203} B_{202} B_{201} B_{200}		101001	117		10100
	$B_{215}B_{214}$ B_{213} B_{212} B_{211} B_{210}		101011	118		10101
	$B_{225}B_{224}$ B_{223} B_{222} B_{221} B_{220}		101101	119		10110
	$B_{235}B_{234}$ B_{233} B_{232} B_{231} B_{230}		101111	120		10111
	$B_{245}B_{244}$ B_{243} B_{242} B_{241} B_{240}		110001	121		11000
	$B_{255}B_{254}$ B_{253} B_{252} B_{251} B_{250}		110011	122		11001
	$B_{265}B_{264}$ B_{263} B_{262} B_{261} B_{260}		110101	123		11010
	$B_{275}B_{274}$ B_{273} B_{272} B_{271} B_{270}		110111	124		11011
	$B_{285}B_{284}$ B_{283} B_{282} B_{281} B_{280}		111001	125		11100
	$B_{295}B_{294}$ B_{293} B_{292} B_{291} B_{290}		111011	126		11101
	$B_{305}B_{304}$ B_{303} B_{302} B_{301} B_{300}		111101	127		11110
	$B_{315}B_{314}$ B_{313} B_{312} B_{311} B_{310}		111111	128		11111

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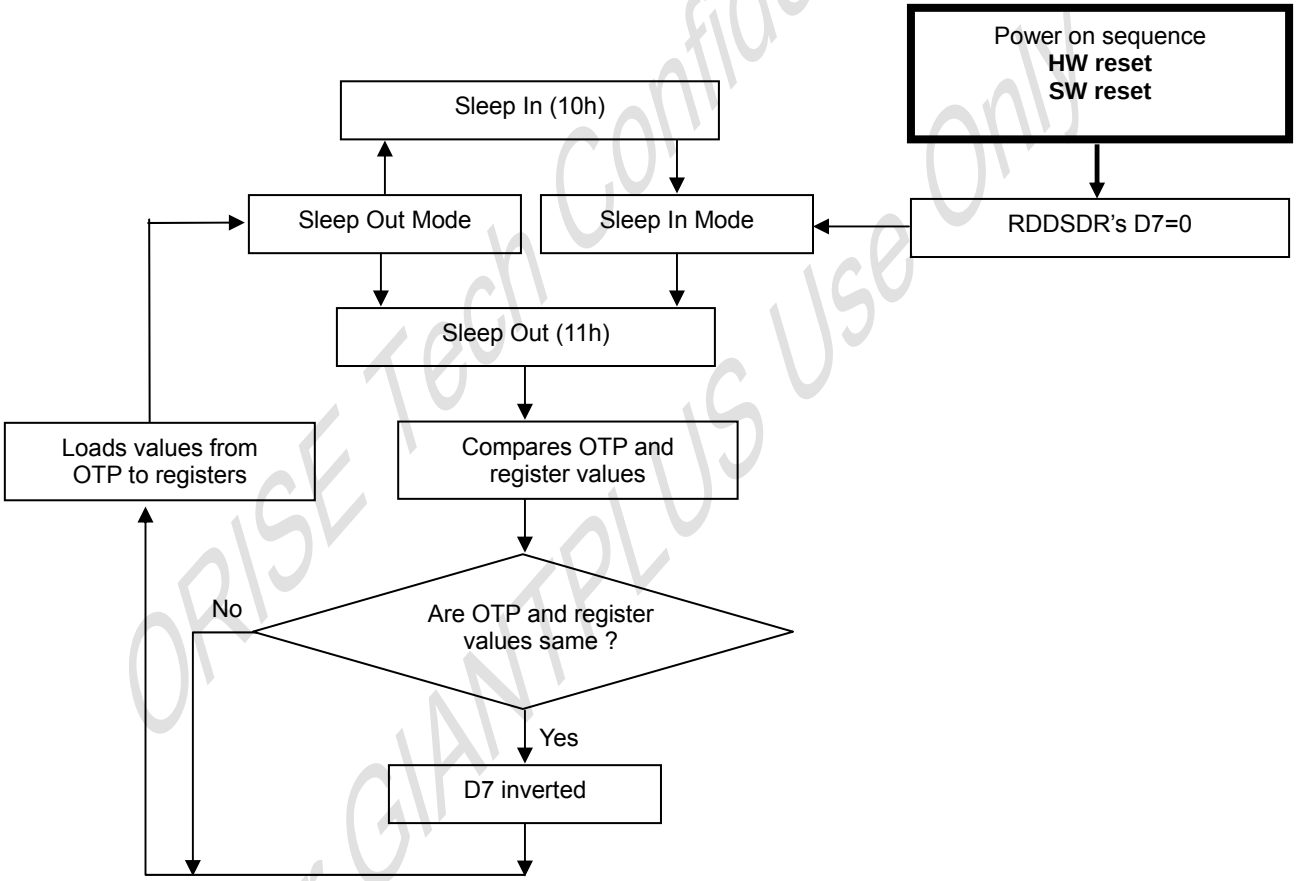
7.15. Sleep Out-Command and Self-Diagnostic Functions of the Display Module

7.15.1. Register Loading Detection

Sleep Out-command is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from OTP (one-time programming memory) to registers of the display controller is working properly.

There are compared factory values of the OTP and register values of the display controller by the display controller. If those both values (OTP and register values) are same, there is inverted (=increased by 1) a bit in "Read Display Self-Diagnostic Result (0Fh)" (=RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= increased by 1).

The flow chart for this internal function is following:



Note: There is not compared and loaded register values, which can be changed by user (00h to AFh and DAh to DDh), by the display module.

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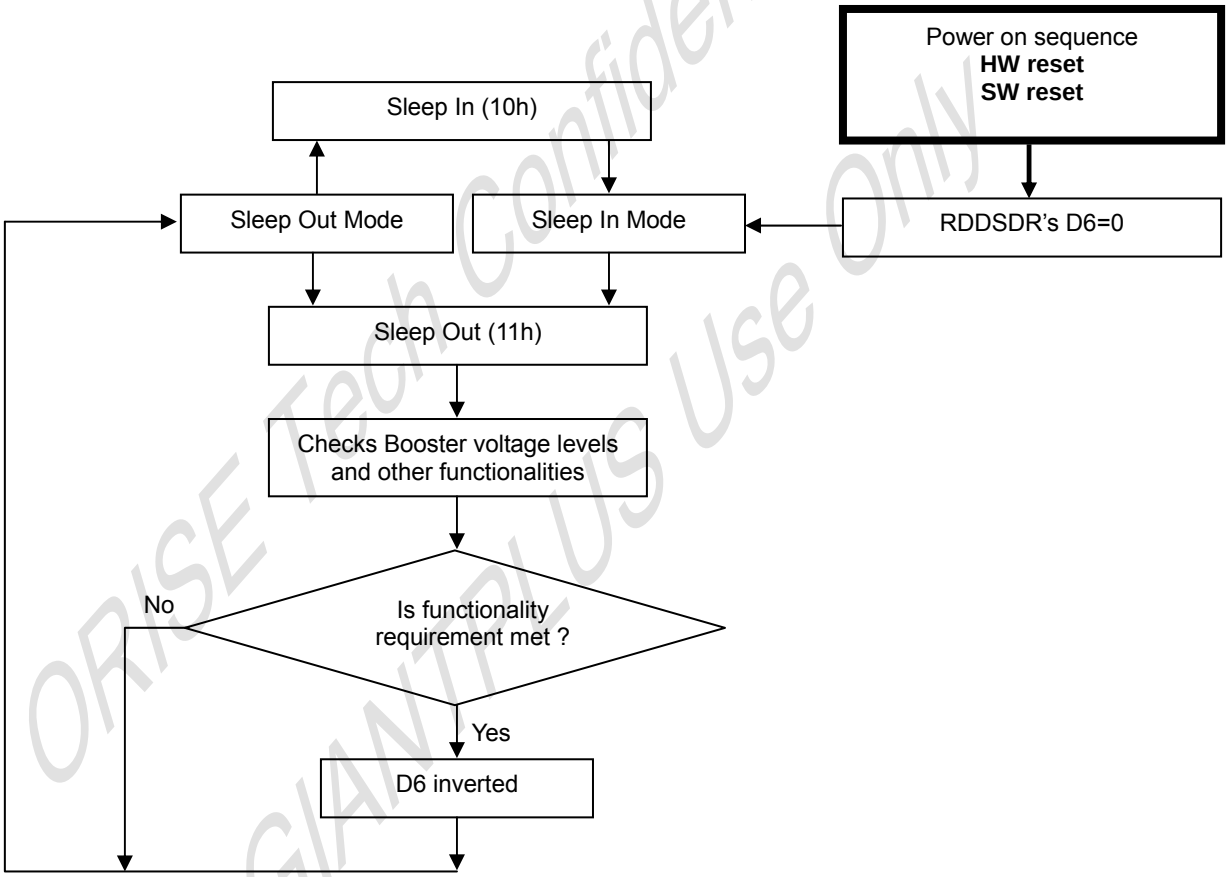
7.15.2. Functionality Detection

Sleep Out-command is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (only Booster voltage level). If functionality requirement is met, there is inverted (= increased by 1) a bit in "Read Display Self- Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1).

The flow chart for this internal function is following:



Note: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out –command is sent in Sleep Out -mode.

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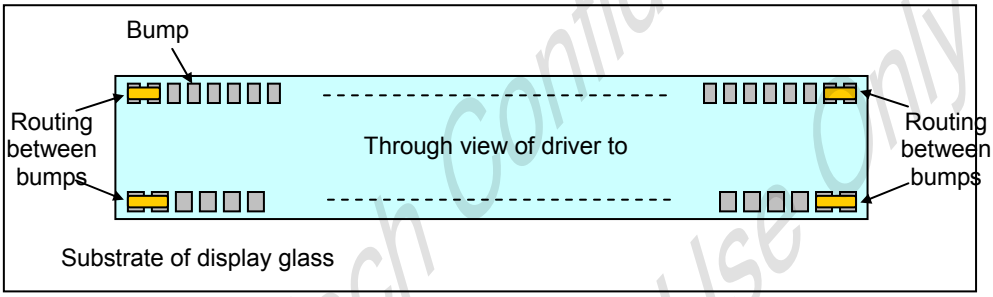
7.15.3. Chip Attachment Detection

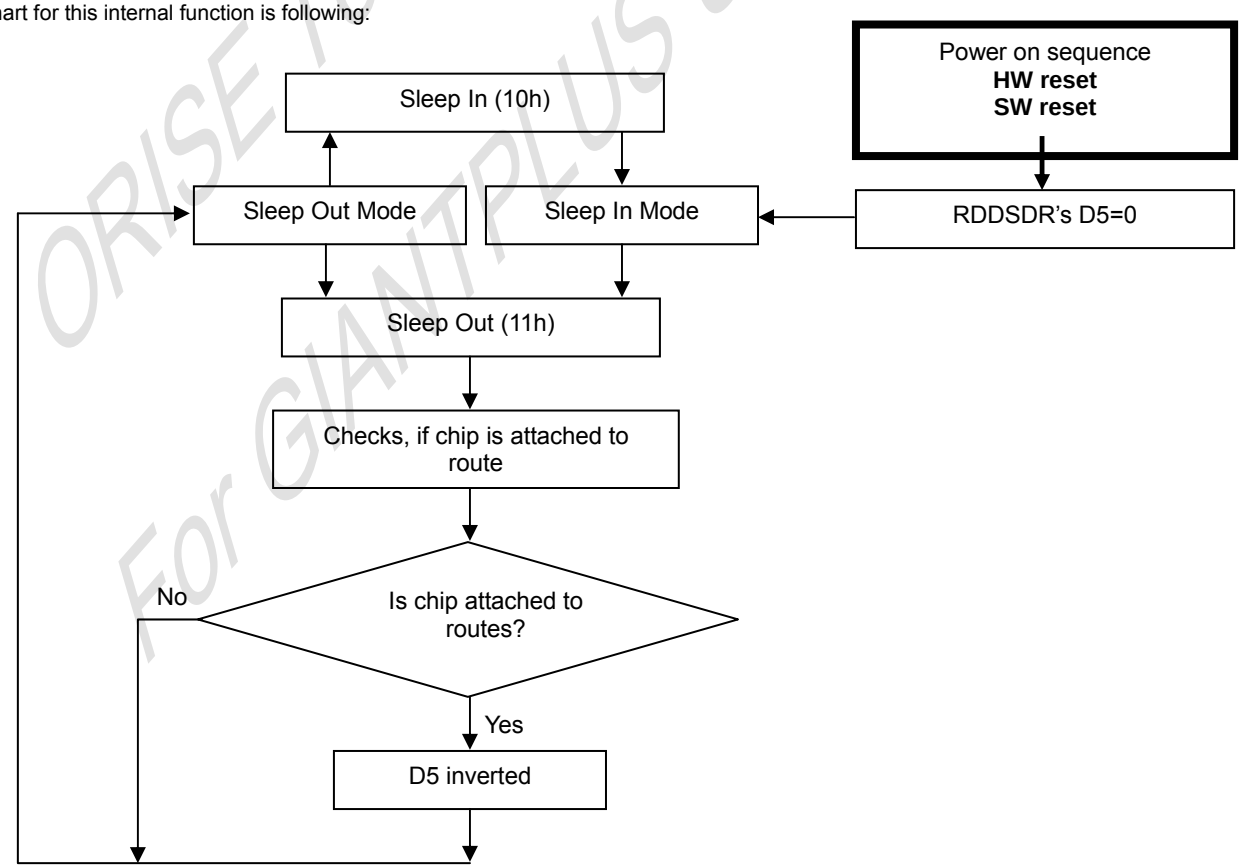
Sleep Out-command is a trigger for an internal function of the display module, which indicates, if a chip or chips (e.g. driver, etc.) of the display module is/are attached to the circuit route of a flex foil or display glass ITO.

There is inverted (= increased by 1) a bit in command "Read Display Self- Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of this command is D5), if the chip or chips is/are attached to the circuit route of the flex or display glass. If this chip is or those chips are not attached to the circuit route of the flex or display glass, this bit (D5) is not inverted (= increased by 1).

The following figure is for reference purposes; how this chip attachment can be implemented e.g. there are connected together 2 bumps via route of ITO or the flex foil on 4 corners of the driver (chip).



The flow chart for this internal function is following:



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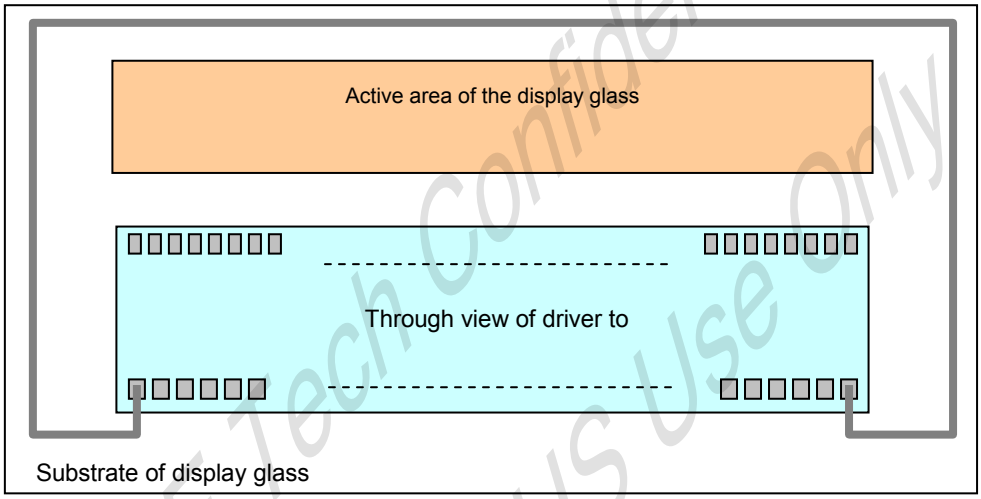
7.15.4. Display Glass Break Detection

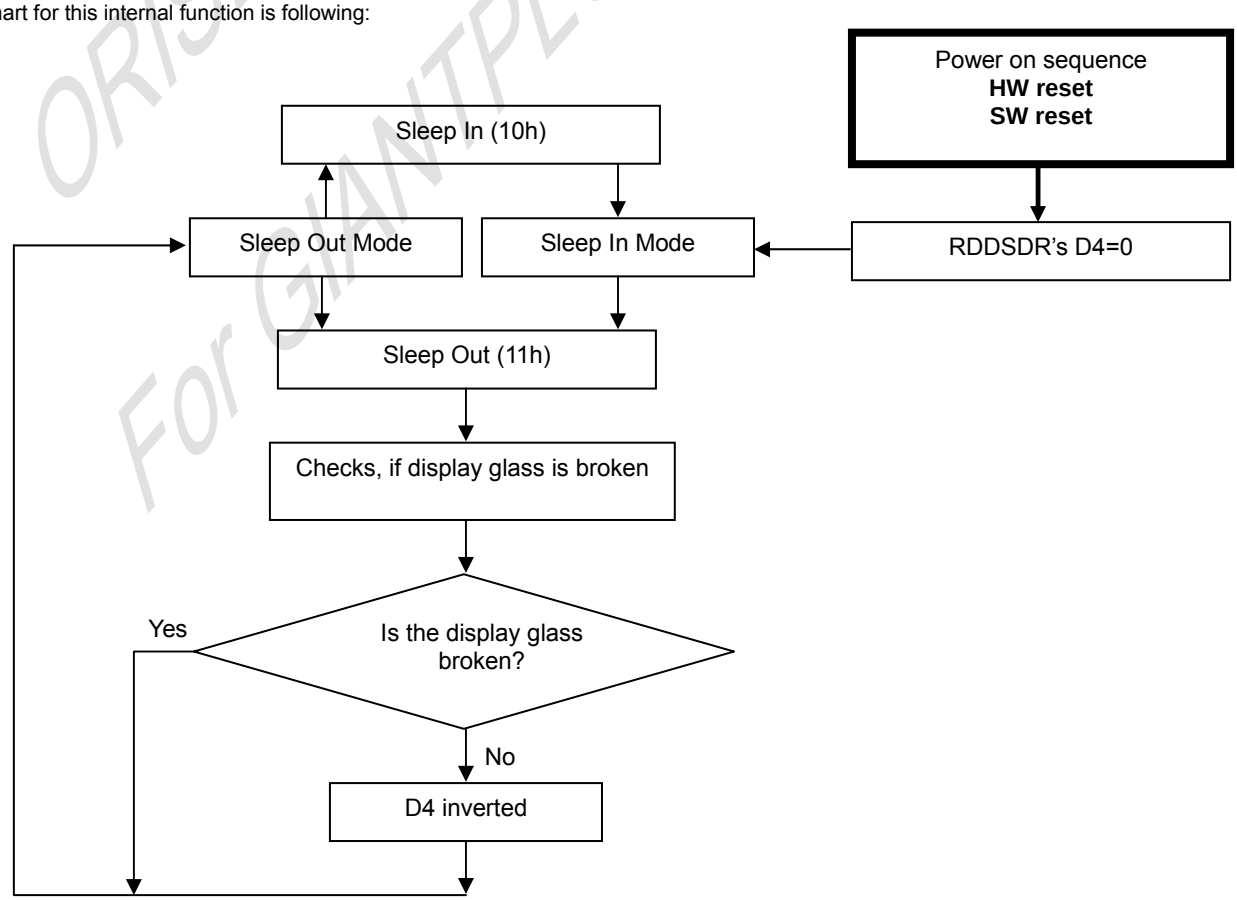
Sleep Out-command is a trigger for an internal function of the display module, which indicates, if the display glass of the display module is broken or not.

There is inverted (= increased by 1) a bit in “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D4), if the display glass is not broken. If this display glass is broken, this bit (D4) is not inverted (= increased by 1).

The following figure is a reference, how this glass break detection can be implemented e.g. there is connected together 2 bumps via route of ITO. This route of ITO is the nearest route of the edge of the display glass.



The flow chart for this internal function is following:



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7.16. Oscillator

The chip has on-chip oscillator that does not require external components. This oscillator output signal is used for system clock generation for internal display operation.

7.17. System Colck Generator

The timing generator produces the various signals to dirver the internal circuitty. Internal chip operation is not affected by operations on the data bus.

7.18. Instruction Decoder and Register

The instruction decoder indentifies command words arriving at the interface and routes the following data bytes to their destination. The command set can be found in " Command" section.

7.19. Source Driver

The source driver block includes 132x3 source outputs (S1 to S396), which should be connected directly to the TFT-LCD. The source output signals are generated in the data processing block after the data is read out of the RAM and latched, which represent the simulatance selected rows.

7.20. Gate Driver

The gate dirver block include 160 chanel gate output (G1 to G162) which should be connected directly to the TFT-LCD.

7.20.1. Gate Driver

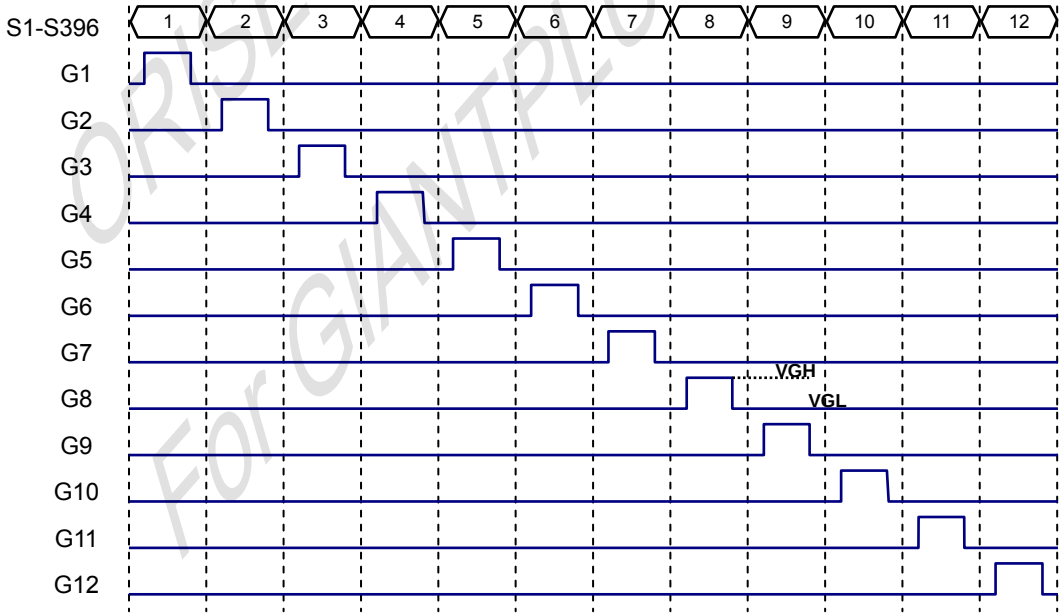

Fig. 7.20.1 Gate Driver Output Option 1

7.21. γ -CORRECTION FUNCTION

The SPFD54124B adopts true 6-bit OP-AMP with adjustable γ -correction function to display in 262,144 colors. The adjustable γ -correction can be set by 14 groups of registers to determine eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers. Each register group can be set independently to other register groups.

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8. ELECTRICAL SPECIFICATIONS

8.1. DC CharacteristicAC Characteristic

(VDD=2.6V~3.6V, VDDIO = 1.6V~3.6V, Ta = -40℃ ~ 85℃)

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Power & Operation Voltage							
Analog Operating voltage	VDD	Operating Voltage	2.6	2.78	3.6	V	
Logic Operating voltage	VDDIO	I/O supply voltage-	1.6	1.8/2.78	3.6	V	
Digital Operating voltage	VCC	Digital supply voltage	2.6		3.6	V	
Gate Driver High voltage	VGH		10.0		13.5	V	
Gate Driver Low voltage	VGL		-11.5		-9.0	V	
Driver Supply voltage		|VGH-VGL|	19		30	V	
Input / Output							
Logic High level input voltage	VIH		0.7VDDIO	-	VDDIO	V	
Logic Low level input voltage	VIL	-	VSS	-	0.3VDDIO	V	
Logic High level output voltage	VOH	IOH = -1.0mA	0.8VDDIO	-	VDDIO	V	
Logic Low level output voltage	VOL	IOL = +1.0mA	VSS	-	0.2VDDIO	V	
Logic High level input current	IIH				1	μA	
Logic Low level input current	IIL		-1			μA	
Logic Input leakage current	IIL	VIN = VDDIO or VSS	-0.1	-	+0.1	μA	
VCOM Operation							
VCOM High voltage	VCOMH	Ccom=12nF	2.5		5.0	V	
VCOM Low voltage	VCOML	Ccom=12nF	-2.5		0.0	V	
VCOM Amplitude voltage	VCOMA	|VCOMH-VCOML|	4.0		6.0	V	
Source Driver							
Source output range	VSout		0.1		AVDD-0.1	V	
Gamma reference voltage	GVDD		3.0		5.0	V	
Source output settling time	Tr	Below with 99% precision		15	20	μs	
Output deviation voltage (Source output channel)	V,dev	Sout >=4.2V, Sout<=0.8V			20	mV	
		4.2V>Sout>0.8V			15	mV	
Output offset voltage	V_{OFSET}				35	mv	
Booster Operation							
Internal reference voltage	V_{REF}				1	%	
1st Booster (VDDx2) voltage	AVDD		4.95 *6)		6.0 *7)	V	
1st Booster (VDDx2) Drop voltage	VDDx2,drop	I_{AVDD} = 1mA (include Panel loading)			5%	%	
Linear range	V_{Linear}		0.2		AVDD-0.2	V	

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8.2. AC timing Characteristics

8.2.1. Parallel Interface Characteristics 18, 16 ,9 or 8-bits bus (8080-series MCU)

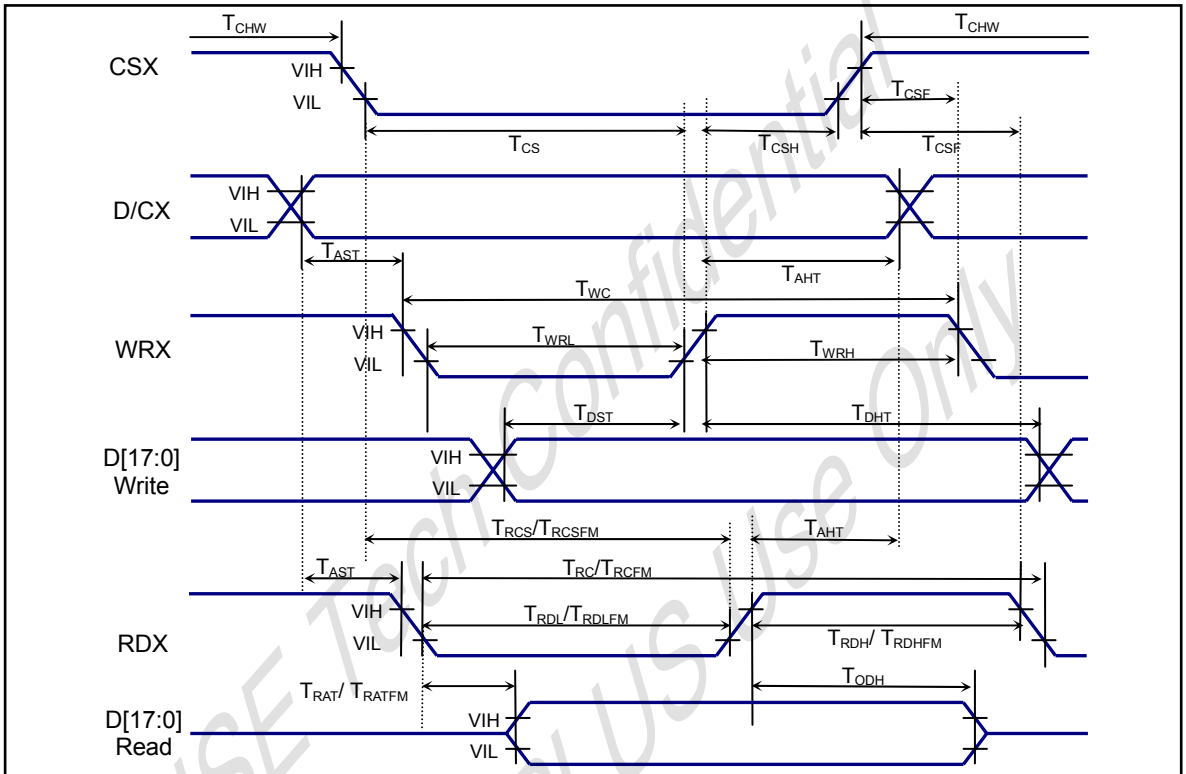

Fig. 8.2.1.1 Parallel Interface characteristics (8080-Series MCU)

Table 8.2.1.1: AC Characteristics for Parallel Interface18, 16, 9, 8-bits bus (8080-series MCU)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
D/CX	T_{AST}	Address setup time	10		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select "H" pulse width	0		ns	-(3-transfer for one pixel)
	T_{CS}	Chip select setup time (Write)	35		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	100		ns	
	T_{WRH}	Control pulse "H" duration	35		ns	
	T_{WRL}	Control pulse "L" duration	35		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	90		ns	
	T_{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For maximum C_L=30pF For minimum C_L=8pF
	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)		40	ns	
	T_{RATFM}	Read access time (FM)		340	ns	
	T_{ODH}	Output disable time	20	80	ns	

Note 1: VDDIO=1.6 to 3.6V, VDD=2.6 to 3.6V, AGND=DGND=0V, Ta=-30 to 70℃ (to +85℃ no damage)

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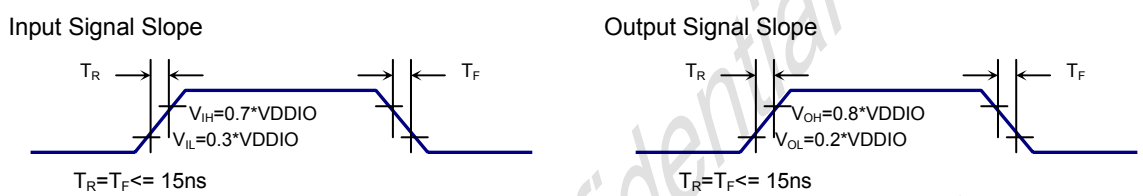

Fig. 8.2.1.2 Rising and Falling timing for Input and Output signal

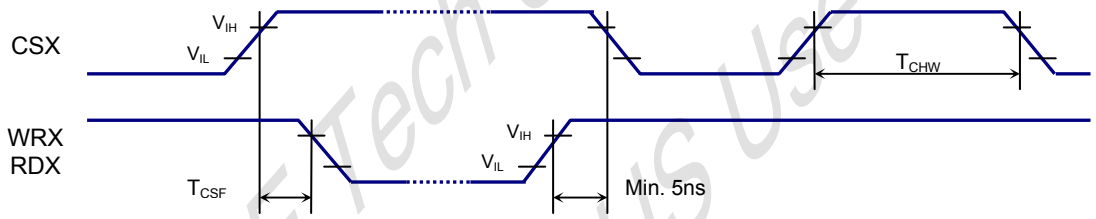

Fig.8.2.1.3 Chip selection (CSX) timing

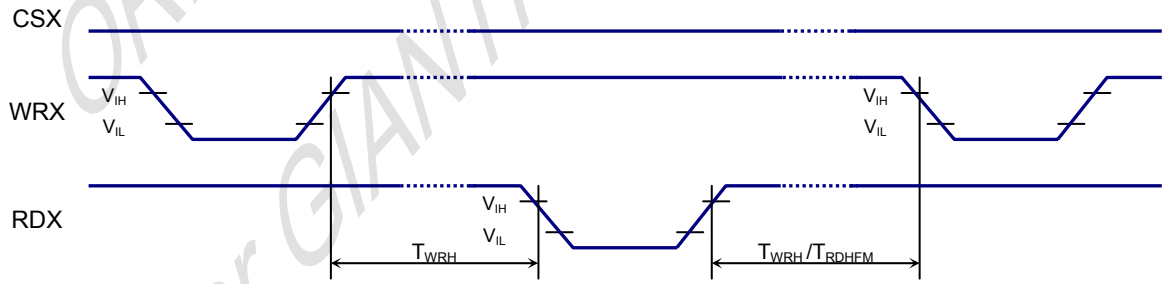

Fig. 8.2.1.4 Write to read and Read to write timing

NOTE: The input signal rise time and fall time (Tr, Tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDDIO for Input signals.

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8.3. Parallel Interface Characteristics 18, 16 ,9 or 8-bits bus (6800-series MCU)

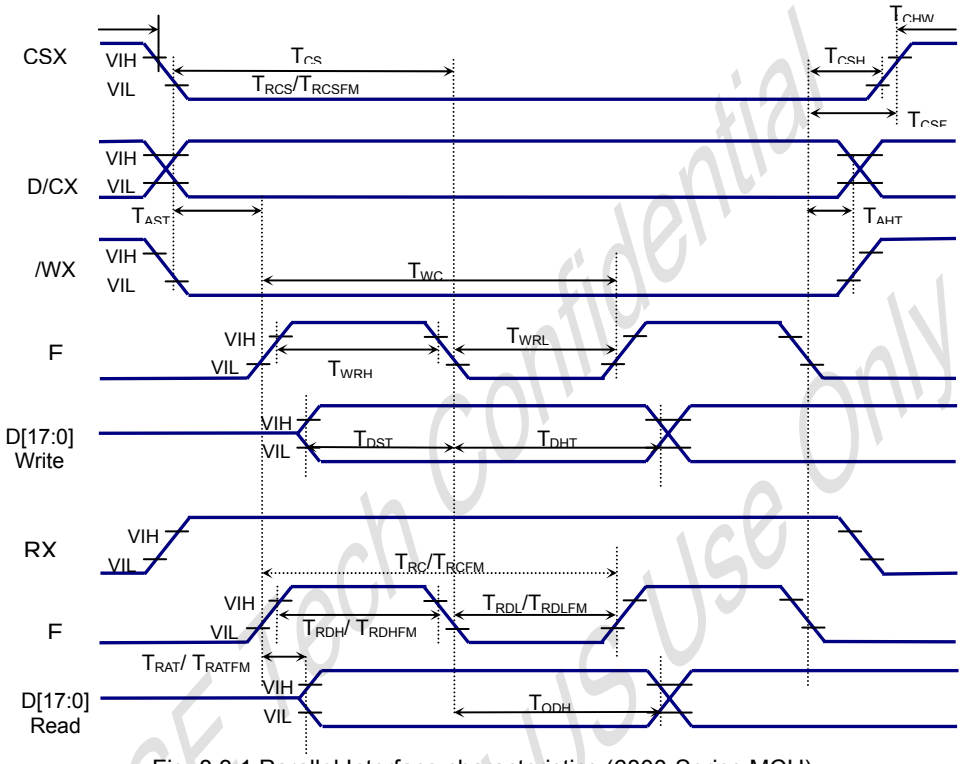

Fig. 8.3.1 Parallel Interface characteristics (6800-Series MCU)

Table 8.3.1: AC Characteristics for Parallel Interface 18, 16, 9, 8-bits bus (6800-series MCU)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
D/CX	T_{AST}	Address setup time	10		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select "H" pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	35		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	100		ns	
	T_{WRH}	Control pulse "H" duration	35		ns	
	T_{WRL}	Control pulse "L" duration	35		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	90		ns	
	T_{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For maximum C_L=30pF For minimum C_L=8pF
	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)		40	ns	
	T_{RATFM}	Read access time (FM)		340	ns	
	T_{ODH}	Output disable time	20	80	ns	

Note 1: VDDIO=1.6 to 3.6V, VDD=2.6 to 3.6V, AGND=DGND=0V, Ta=-30 to 70℃ (to +85℃ no damage)

Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDDIO for Input signals.

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8.4. Serial Interface Characteristics (3-pin Serial)

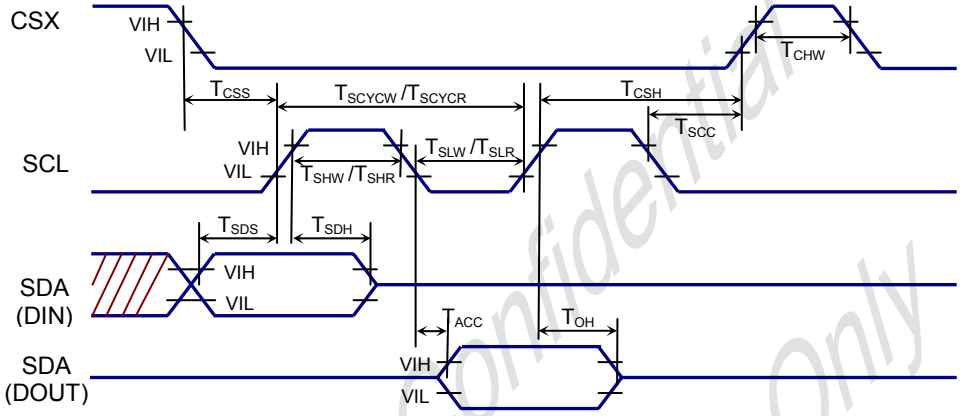

Fig. 8.4.1 3-pin Serial Interface Characteristics

Table 8.4.1: 3-pin Serial Interface Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time	60		ns	
	T_{CSH}	Chip select hold time	65		ns	
	T_{SCC}	Chip select setup time	20		ns	
	T_{CHW}	Chip select setup time	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	100		ns	-
	T_{SHW}	SCL "H" pulse width (Write)	35		ns	
	T_{SLW}	SCL "L" pulse width (Write)	35		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN) (DOUT)	T_{SDS}	Data setup time	30		ns	
	T_{SDH}	Data hold time	30		ns	
	T_{ACC}	Access time	10		ns	For maximum C_L=30pF For minimum C_L=8pF
	T_{OH}	Output disable time	15		ns	

Note 1: VDDIO=1.6 to 3.6V, VDD=2.6 to 3.6V, AGND=DGND=0V, Ta=-30 to 70℃ (to +85℃ no damage)

Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDDIO for Input signals.

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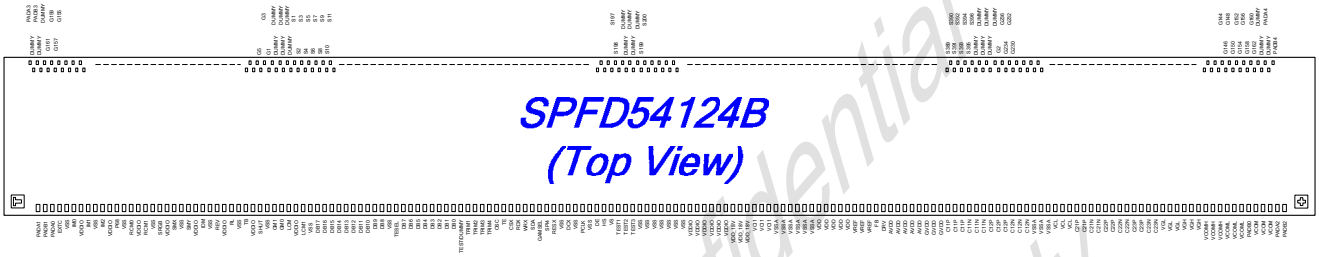
9. CHIP INFORMATION

9.1. PAD Assignment



Coordinates origin: Pad Left-bottom side

9.2. PAD Dimension

Item	PAD No.	Size		Unit
		X	Y	
Chip Size	-	13500	700	μm
Chip thickness	-	400		
Pad pitch	176~760	22	-	
	1, 2, 174, 175	64	-	
	3~173	80	-	
Bumped pad size	176~760	21	96	
	3~173	55	96	
	1, 2, 174, 175	50	96	

Note1: Chip size included scribe line.

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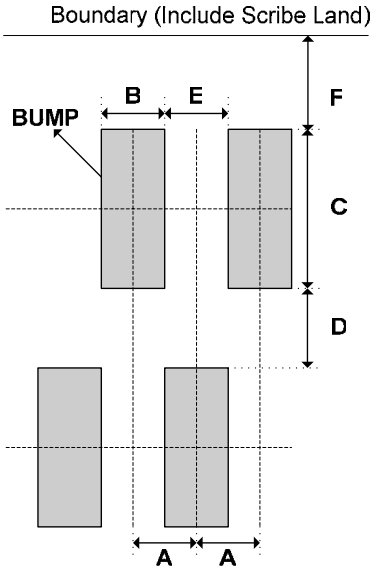
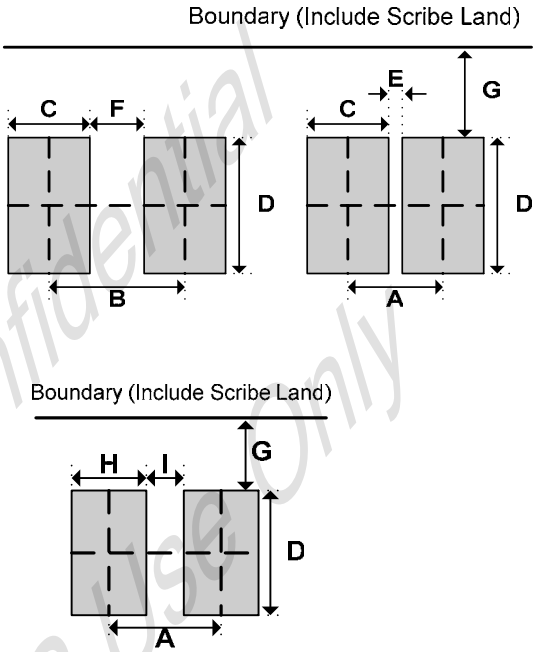
9.3. Bump Dimension

9.3.1. Output Pads



Item	Sumbol	Size
Bump Pitch	A	22 um
Bump Width	B	21 um
Bump height	C	96 um
Bump space 1	D	35 um
Bump space 2	E	23 um
Bump area	BxC	2016 um^2
Chip boundary	F	45-70 um

9.3.2. Input Pads



Item	Sumbol	Size
Bump Pitch	A	64 um
Bump Pitch	B	80 um
Bump Width	C	55 um
Bump height	D	96 um
Bump space 1	E	9 um
Bump space 2	F	25um
Bump area	CxD	5280 um^2
Chip boundary	G	45-70 um
Bump Width	H	50
Bump space 3	I	14

9.4. Bump Characteristics

Item	Standard	Note
Bump Hardness	75Hv	±25Hv
Bump Height	15μm	±3μm
Co-planarity (in Chip)	R≦ 2μm	R : Max-Min
Roughness (in Bump)	R≦ 2μm	R : Max-Min
Bump Size	“X” ± 4μm x “Y” ± 4μm	X/Y: bump size
Shear Force	>4.5g/mil^2	

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9.5. PAD Locations

PAD No.	PAD Name	X	Y
1	PADA1	246	78
2	PADB1	310	78
3	PADA0	390	78
4	EXTC	470	78
5	VSS	550	78
6	IM0	630	78
7	VDDIO	710	78
8	IM1	790	78
9	VSS	870	78
10	IM2	950	78
11	VDDIO	1030	78
12	P68	1110	78
13	VSS	1190	78
14	RCM0	1270	78
15	VDDIO	1350	78
16	RCM1	1430	78
17	VSS	1510	78
18	SRGB	1590	78
19	VDDIO	1670	78
20	SMX	1750	78
21	VSS	1830	78
22	SMY	1910	78
23	VDDIO	1990	78
24	IDM	2070	78
25	VSS	2150	78
26	REV	2230	78
27	VDDIO	2310	78
28	RL	2390	78
29	VSS	2470	78
30	TB	2550	78
31	VDDIO	2630	78
32	SHUT	2710	78
33	VSS	2790	78
34	GM1	2870	78
35	GM0	2950	78
36	LCM0	3030	78
37	VDDIO	3110	78
38	LCM1	3190	78
39	VSS	3270	78
40	DB17	3350	78
41	DB16	3430	78
42	DB15	3510	78
43	DB14	3590	78
44	DB13	3670	78
45	DB12	3750	78
46	DB11	3830	78
47	DB10	3910	78
48	DB9	3990	78
49	DB8	4070	78
50	VSS	4150	78
51	TESEL	4230	78
52	DB7	4310	78
53	DB6	4390	78
54	DB5	4470	78
55	DB4	4550	78

PAD No.	PAD Name	X	Y
56	DB3	4630	78
57	DB2	4710	78
58	DB1	4790	78
59	DB0	4870	78
60	TEST/DUMMY	4950	78
61	TRIM1	5030	78
62	TRIM2	5110	78
63	TRIM3	5190	78
64	TRIM4	5270	78
65	OSC	5350	78
66	TE	5430	78
67	CSX	5510	78
68	RDX	5590	78
69	WRX	5670	78
70	SDA	5750	78
71	GAMSEL	5830	78
72	SPI4	5910	78
73	RESX	5990	78
74	VSS	6070	78
75	DCX	6150	78
76	VSS	6230	78
77	PCLK	6310	78
78	VSS	6390	78
79	DE	6470	78
80	HS	6550	78
81	VS	6630	78
82	TEST1	6710	78
83	TEST2	6790	78
84	TEST3	6870	78
85	VSS	6950	78
86	VSS	7014	78
87	VSS	7078	78
88	VSS	7142	78
89	VSS	7206	78
90	VSS	7270	78
91	VSS	7334	78
92	VDDIO	7414	78
93	VDDIO	7478	78
94	VDDIO	7542	78
95	VDDIO	7606	78
96	VDDIO	7670	78
97	VDDIO	7734	78
98	VDD_18V	7814	78
99	VDD_18V	7878	78
100	VDD_18V	7942	78
101	VCI1	8022	78
102	VCI1	8086	78
103	VCI1	8150	78
104	VSSA	8230	78
105	VSSA	8294	78
106	VSSA	8358	78
107	VSSA	8422	78
108	VSSA	8486	78
109	VSSA	8550	78
110	VDD	8630	78

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PAD No.	PAD Name	X	Y
111	VDD	8694	78
112	VDD	8758	78
113	VDD	8822	78
114	VDD	8886	78
115	VREF	8966	78
116	VREF	9030	78
117	VREF	9094	78
118	FB	9174	78
119	DRV	9254	78
120	VDDA	9334	78
121	VDDA	9398	78
122	VDDA	9462	78
123	VDDA	9526	78
124	VDDA	9590	78
125	GVDD	9670	78
126	GVDD	9734	78
127	GVDD	9798	78
128	C11P	9878	78
129	C11P	9942	78
130	C11P	10006	78
131	C11N	10086	78
132	C11N	10150	78
133	C11N	10214	78
134	C12P	10294	78
135	C12P	10358	78
136	C12P	10422	78
137	C12N	10502	78
138	C12N	10566	78
139	C12N	10630	78
140	VSSA	10710	78
141	VSSA	10774	78
142	VSSA	10838	78
143	VCL	10918	78
144	VCL	10982	78
145	VCL	11046	78
146	C21P	11126	78
147	C21P	11190	78
148	C21N	11270	78
149	C21N	11334	78
150	C22P	11414	78
151	C22P	11478	78
152	C22N	11558	78
153	C22N	11622	78
154	C23P	11702	78
155	C23P	11766	78
156	C23N	11846	78
157	C23N	11910	78
158	VGL	11990	78
159	VGL	12054	78
160	VGL	12118	78
161	VGH	12198	78
162	VGH	12262	78
163	VGH	12326	78
164	VCOMH	12406	78
165	VCOMH	12470	78
166	VCOMH	12534	78

PAD No.	PAD Name	X	Y
167	VCOML	12614	78
168	VCOML	12678	78
169	VCOML	12742	78
170	PADB0	12822	78
171	VCOM	12902	78
172	VCOM	12966	78
173	VCOM	13030	78
174	PADA2	13110	78
175	PADB2	13174	78
176	PADB4	13134	542
177	DUMMY	13112	411
178	PADA4	13090	542
179	DUMMY	13068	411
180	DUMMY	13046	542
181	G162	13024	411
182	G160	13002	542
183	G158	12980	411
184	G156	12958	542
185	G154	12936	411
186	G152	12914	542
187	G150	12892	411
188	G148	12870	542
189	G146	12848	411
190	G144	12826	542
191	G142	12804	411
192	G140	12782	542
193	G138	12760	411
194	G136	12738	542
195	G134	12716	411
196	G132	12694	542
197	G130	12672	411
198	G128	12650	542
199	G126	12628	411
200	G124	12606	542
201	G122	12584	411
202	G120	12562	542
203	G118	12540	411
204	G116	12518	542
205	G114	12496	411
206	G112	12474	542
207	G110	12452	411
208	G108	12430	542
209	G106	12408	411
210	G104	12386	542
211	G102	12364	411
212	G100	12342	542
213	G98	12320	411
214	G96	12298	542
215	G94	12276	411
216	G92	12254	542
217	G90	12232	411
218	G88	12210	542
219	G86	12188	411
220	G84	12166	542
221	G82	12144	411
222	G80	12122	542

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PAD No.	PAD Name	X	Y
223	G78	12100	411
224	G76	12078	542
225	G74	12056	411
226	G72	12034	542
227	G70	12012	411
228	G68	11990	542
229	G66	11968	411
230	G64	11946	542
231	G62	11924	411
232	G60	11902	542
233	G58	11880	411
234	G56	11858	542
235	G54	11836	411
236	G52	11814	542
237	G50	11792	411
238	G48	11770	542
239	G46	11748	411
240	G44	11726	542
241	G42	11704	411
242	G40	11682	542
243	G38	11660	411
244	G36	11638	542
245	G34	11616	411
246	G32	11594	542
247	G30	11572	411
248	G28	11550	542
249	G26	11528	411
250	G24	11506	542
251	G22	11484	411
252	G20	11462	542
253	G18	11440	411
254	G16	11418	542
255	G14	11396	411
256	G12	11374	542
257	G10	11352	411
258	G8	11330	542
259	G6	11308	411
260	G4	11286	542
261	G2	11264	411
262	DUMMY	11242	542
263	DUMMY	11220	411
264	DUMMY	11198	542
265	DUMMY	11176	411
266	DUMMY	11154	542
267	DUMMY	11132	411
268	S396	11110	542
269	S395	11088	411
270	S394	11066	542
271	S393	11044	411
272	S392	11022	542
273	S391	11000	411
274	S390	10978	542
275	S389	10956	411
276	S388	10934	542
277	S387	10912	411
278	S386	10890	542

PAD No.	PAD Name	X	Y
279	S385	10868	411
280	S384	10846	542
281	S383	10824	411
282	S382	10802	542
283	S381	10780	411
284	S380	10758	542
285	S379	10736	411
286	S378	10714	542
287	S377	10542	411
288	S376	10670	542
289	S375	10648	411
290	S374	10626	542
291	S373	10604	411
292	S372	10582	542
293	S371	10560	411
294	S370	10538	542
295	S369	10516	411
296	S368	10494	542
297	S367	10472	411
298	S366	10450	542
299	S365	10428	411
300	S364	10406	542
301	S363	10384	411
302	S362	10362	542
303	S361	10340	411
304	S360	10318	542
305	S359	10296	411
306	S358	10274	542
307	S357	10252	411
308	S356	10230	542
309	S355	10208	411
310	S354	10186	542
311	S353	10164	411
312	S352	10142	542
313	S351	10120	411
314	S350	10098	542
315	S349	10076	411
316	S348	10054	542
317	S347	10032	411
318	S346	10010	542
319	S345	9988	411
320	S344	9966	542
321	S343	9944	411
322	S342	9922	542
323	S341	9900	411
324	S340	9878	542
325	S339	9856	411
326	S338	9834	542
327	S337	9812	411
328	S336	9790	542
329	S335	9768	411
330	S334	9746	542
331	S333	9724	411
332	S332	9702	542
333	S331	9680	411
334	S330	9658	542

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PAD No.	PAD Name	X	Y
335	S329	9636	411
336	S328	9614	542
337	S327	9592	411
338	S326	9570	542
339	S325	9548	411
340	S324	9526	542
341	S323	9504	411
342	S322	9482	542
343	S321	9460	411
344	S320	9438	542
345	S319	9416	411
346	S318	9394	542
347	S317	9372	411
348	S316	9350	542
349	S315	9328	411
350	S314	9306	542
351	S313	9284	411
352	S312	9262	542
353	S311	9240	411
354	S310	9218	542
355	S309	9196	411
356	S308	9174	542
357	S307	9152	411
358	S306	9130	542
359	S305	9108	411
360	S304	9086	542
361	S303	9064	411
362	S302	9042	542
363	S301	9020	411
364	S300	8998	542
365	S299	8976	411
366	S298	8954	542
367	S297	8932	411
368	S296	8910	542
369	S295	8888	411
370	S294	8866	542
371	S293	8844	411
372	S292	8822	542
373	S291	8800	411
374	S290	8778	542
375	S289	8756	411
376	S288	8734	542
377	S287	8712	411
378	S286	8690	542
379	S285	8668	411
380	S284	8646	542
381	S283	8624	411
382	S282	8602	542
383	S281	8580	411
384	S280	8558	542
385	S279	8536	411
386	S278	8514	542
387	S277	8492	411
388	S276	8470	542
389	S275	8448	411
390	S274	8426	542

PAD No.	PAD Name	X	Y
391	S273	8404	411
392	S272	8382	542
393	S271	8360	411
394	S270	8338	542
395	S269	8316	411
396	S268	8294	542
397	S267	8272	411
398	S266	8250	542
399	S265	8228	411
400	S264	8206	542
401	S263	8184	411
402	S262	8162	542
403	S261	8140	411
404	S260	8118	542
405	S259	8096	411
406	S258	8074	542
407	S257	8052	411
408	S256	8030	542
409	S255	8008	411
410	S254	7986	542
411	S253	7964	411
412	S252	7942	542
413	S251	7920	411
414	S250	7898	542
415	S249	7876	411
416	S248	7854	542
417	S247	7832	411
418	S246	7810	542
419	S245	7788	411
420	S244	7766	542
421	S243	7744	411
422	S242	7722	542
423	S241	7700	411
424	S240	7678	542
425	S239	7656	411
426	S238	7634	542
427	S237	7612	411
428	S236	7590	542
429	S235	7568	411
430	S234	7546	542
431	S233	7524	411
432	S232	7502	542
433	S231	7480	411
434	S230	7458	542
435	S229	7436	411
436	S228	7414	542
437	S227	7392	411
438	S226	7370	542
439	S225	7348	411
440	S224	7326	542
441	S223	7304	411
442	S222	7282	542
443	S221	7260	411
444	S220	7238	542
445	S219	7216	411
446	S218	7194	542

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PAD No.	PAD Name	X	Y
447	S217	7172	411
448	S216	7150	542
449	S215	7128	411
450	S214	7106	542
451	S213	7084	411
452	S212	7062	542
453	S211	7040	411
454	S210	7018	542
455	S209	6996	411
456	S208	6974	542
457	S207	6952	411
458	S206	6930	542
459	S205	6908	411
460	S204	6886	542
461	S203	6864	411
462	S202	6842	542
463	S201	6820	411
464	S200	6798	542
465	S199	6776	411
466	DUMMY	6754	542
467	DUMMY	6732	411
468	DUMMY	6710	542
469	DUMMY	6688	411
470	DUMMY	6666	542
471	S198	6644	411
472	S197	6622	542
473	S196	6600	411
474	S195	6578	542
475	S194	6556	411
476	S193	6534	542
477	S192	6512	411
478	S191	6490	542
479	S190	6468	411
480	S189	6446	542
481	S188	6424	411
482	S187	6402	542
483	S186	6380	411
484	S185	6358	542
485	S184	6336	411
486	S183	6314	542
487	S182	6292	411
488	S181	6270	542
489	S180	6248	411
490	S179	6226	542
491	S178	6204	411
492	S177	6182	542
493	S176	6160	411
494	S175	6138	542
495	S174	6116	411
496	S173	6094	542
497	S172	6072	411
498	S171	6050	542
499	S170	6028	411
500	S169	6006	542
501	S168	5984	411
502	S167	5962	542

PAD No.	PAD Name	X	Y
503	S166	5940	411
504	S165	5918	542
505	S164	5896	411
506	S163	5874	542
507	S162	5852	411
508	S161	5830	542
509	S160	5808	411
510	S159	5786	542
511	S158	5764	411
512	S157	5742	542
513	S156	5720	411
514	S155	5698	542
515	S154	5676	411
516	S153	5654	542
517	S152	5632	411
518	S151	4110	542
519	S150	5588	411
520	S149	5566	542
521	S148	5544	411
522	S147	5522	542
523	S146	5500	411
524	S145	5478	542
525	S144	5456	411
526	S143	5434	542
527	S142	5422	411
528	S141	5390	542
529	S140	5368	411
530	S139	5346	542
531	S138	5324	411
532	S137	5302	542
533	S136	5280	411
534	S135	5258	542
535	S134	5236	411
536	S133	5214	542
537	S132	5192	411
538	S131	5170	542
539	S130	5148	411
540	S129	5126	542
541	S128	5104	411
542	S127	5082	542
543	S126	5060	411
544	S125	5038	542
545	S124	5016	411
546	S123	4994	542
547	S122	4972	411
548	S121	4950	542
549	S120	4928	411
550	S119	4906	542
551	S118	4884	411
552	S117	4862	542
553	S116	4840	411
554	S115	4818	542
555	S114	4796	411
556	S113	4774	542
557	S112	4752	411
558	S111	4730	542

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PAD No.	PAD Name	X	Y
559	S110	4708	411
560	S109	4686	542
561	S108	4664	411
562	S107	4642	542
563	S106	4620	411
564	S105	4598	542
565	S104	4576	411
566	S103	4554	542
567	S102	4532	411
568	S101	4510	542
569	S100	4488	411
570	S99	4466	542
571	S98	4444	411
572	S97	4422	542
573	S96	4400	411
574	S95	4378	542
575	S94	4356	411
576	S93	4334	542
577	S92	4312	411
578	S91	4290	542
579	S90	4268	411
580	S89	4246	542
581	S88	4224	411
582	S87	4202	542
583	S86	4180	411
584	S85	4158	542
585	S84	4136	411
586	S83	4114	542
587	S82	4092	411
588	S81	4070	542
589	S80	4048	411
590	S79	4026	542
591	S78	4004	411
592	S77	3982	542
593	S76	3960	411
594	S75	3938	542
595	S74	3916	411
596	S73	3894	542
597	S72	3872	411
598	S71	3850	542
599	S70	3828	411
600	S69	3806	542
601	S68	3784	411
602	S67	3762	542
603	S66	3740	411
604	S65	3718	542
605	S64	3696	411
606	S63	3674	542
607	S62	3652	411
608	S61	3630	542
609	S60	3608	411
610	S59	3586	542
611	S58	3564	411
612	S57	3542	542
613	S56	3520	411
614	S55	3498	542

PAD No.	PAD Name	X	Y
615	S54	3476	411
616	S53	3454	542
617	S52	3432	411
618	S51	3410	542
619	S50	3388	411
620	S49	3366	542
621	S48	3344	411
622	S47	3322	542
623	S46	3300	411
624	S45	3278	542
625	S44	3256	411
626	S43	3234	542
627	S42	3212	411
628	S41	3190	542
629	S40	3168	411
630	S39	3146	542
631	S38	3124	411
632	S37	3102	542
633	S36	3080	411
634	S35	3058	542
635	S34	3036	411
636	S33	3014	542
637	S32	2992	411
638	S31	2970	542
639	S30	2948	411
640	S29	2926	542
641	S28	2904	411
642	S27	2882	542
643	S26	2860	411
644	S25	2838	542
645	S24	2816	411
646	S23	2794	542
647	S22	2772	411
648	S21	2750	542
649	S20	2728	411
650	S19	2706	542
651	S18	2684	411
652	S17	2662	542
653	S16	2640	411
654	S15	2618	542
655	S14	2596	411
656	S13	2574	542
657	S12	2552	411
658	S11	2530	542
659	S10	2508	411
660	S9	2486	542
661	S8	2464	411
662	S7	2442	542
663	S6	2420	411
664	S5	2398	542
665	S4	2376	411
666	S3	2354	542
667	S2	2332	411
668	S1	2310	542
669	DUMMY	2288	411
670	DUMMY	2266	542

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PAD No.	PAD Name	X	Y
671	DUMMY	2244	411
672	DUMMY	2222	542
673	DUMMY	2200	411
674	DUMMY	2178	542
675	G1	2156	411
676	G3	2134	542
677	G5	2112	411
678	G7	2090	542
679	G9	2068	411
680	G11	2046	542
681	G13	2024	411
682	G15	2002	542
683	G17	1980	411
684	G19	1958	542
685	G21	1936	411
686	G23	1914	542
687	G25	1892	411
688	G27	1870	542
689	G29	1848	411
690	G31	1826	542
691	G33	1804	411
692	G35	1782	542
693	G37	1760	411
694	G39	1738	542
695	G41	1716	411
696	G43	1694	542
697	G45	1672	411
698	G47	1650	542
699	G49	1628	411
700	G51	1606	542
701	G53	1584	411
702	G55	1562	542
703	G57	1540	411
704	G59	1518	542
705	G61	1496	411
706	G63	1474	542
707	G65	1452	411
708	G67	1430	542
709	G69	1408	411
710	G71	1386	542
711	G73	1364	411
712	G75	1342	542
713	G77	1320	411
714	G79	1298	542
715	G81	1276	411
716	G83	1254	542
717	G85	1232	411
718	G87	1210	542
719	G89	1188	411
720	G91	1166	542

PAD No.	PAD Name	X	Y
721	G93	1144	411
722	G95	1122	542
723	G97	1100	411
724	G99	1078	542
725	G101	1056	411
726	G103	1034	542
727	G105	1012	411
728	G107	990	542
729	G109	968	411
730	G111	946	542
731	G113	924	411
732	G115	902	542
733	G117	880	411
734	G119	858	542
735	G121	836	411
736	G123	814	542
737	G125	792	411
738	G127	770	542
739	G129	748	411
740	G131	726	542
741	G133	704	411
742	G135	682	542
743	G137	660	411
744	G139	638	542
745	G141	616	411
746	G143	594	542
747	G145	572	411
748	G147	550	542
749	G149	528	411
750	G151	506	542
751	G153	484	411
752	G155	462	542
753	G157	440	411
754	G159	418	542
755	G161	396	411
756	DUMMY	374	542
757	DUMMY	352	411
758	PADB3	330	542
759	DUMMY	308	411
760	PADA3	286	542

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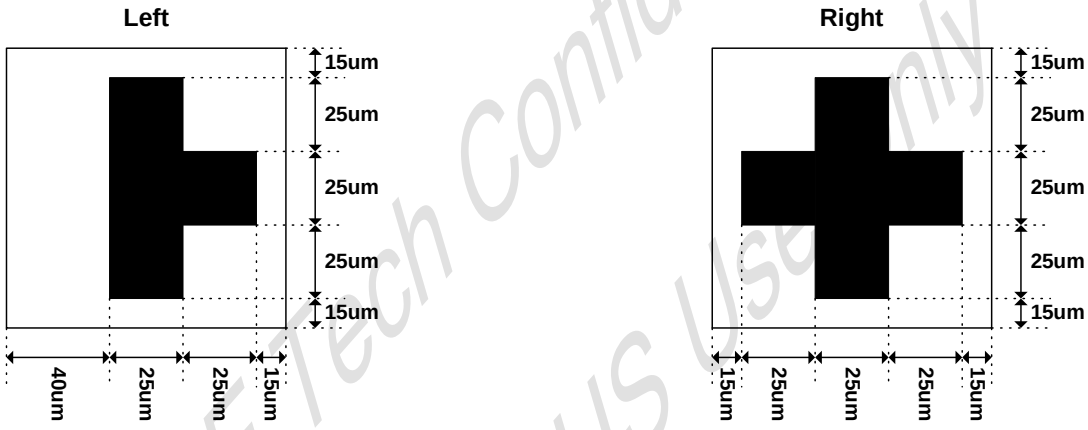
9.6. Alignment Mark

--Alignment Mark coordinate

Left (95, 107.5)

Right (13337.5, 107.5)

--Alignment Mark size



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9.7. Wiring Resistance

	Name	Wiring Resistance		Name	Wiring Resistance		Name	Wiring Resistance
1	PADA1	Open	71	GAMSEL	200 ohm	141	VSSA	10 ohm
2	PADB1	Open	72	SPI4	200 ohm	142	VSSA	
3	PADA0	Note1*(200 ohm)	73	RESX	200 ohm	143	VCL	20 ohm
4	EXTC	200 ohm	74	VSS	Open	144	VCL	
5	VSS	Open	75	DCX	100 ohm	145	VCL	
6	IM0	200 ohm	76	VSS	Open	146	C21P	5 ohm
7	VDDIO	Open	77	PCLK	100 ohm	147	C21P	
8	IM1	200 ohm	78	VSS	Open	148	C21N	5 ohm
9	VSS	Open	79	DE	100 ohm	149	C21N	
10	IM2	200 ohm	80	HS	100 ohm	150	C22P	5 ohm
11	VDDIO	Open	81	VS	100 ohm	151	C22P	
12	P68	200 ohm	82	TEST1	Open	152	C22N	5 ohm
13	VSS	Open	83	TEST2	Open	153	C22N	
14	RCM0	200 ohm	84	TEST3	Open	154	C23P	5 ohm
15	VDDIO	Open	85	VSS		155	C23P	
16	RCM1	200 ohm	86	VSS		156	C23N	5 ohm
17	VSS	Open	87	VSS		157	C23N	
18	SRGB	200 ohm	88	VSS		158	VGL	10 ohm
19	VDDIO	Open	89	VSS		159	VGL	
20	SMX	200 ohm	90	VSS		160	VGL	
21	VSS	Open	91	VSS	5 ohm	161	VGH	30 ohm
22	SMY	200 ohm	92	VDDIO		162	VGH	
23	VDDIO	Open	93	VDDIO		163	VGH	
24	IDM	200 ohm	94	VDDIO		164	VCOMH	30 ohm
25	VSS	Open	95	VDDIO		165	VCOMH	
26	REV	200 ohm	96	VDDIO		166	VCOMH	
27	VDDIO	Open	97	VDDIO	10 ohm	167	VCOML	30 ohm
28	RL	200 ohm	98	VDD_18V		168	VCOML	
29	VSS	Open	99	VDD_18V		169	VCOML	
30	TB	200 ohm	100	VDD_18V	10 ohm	170	PADB0	Note1*(200 ohm)
31	VDDIO	Open	101	VCI1		171	VCOM	10 ohm
32	SHUT	200 ohm	102	VCI1		172	VCOM	
33	VSS	Open	103	VCI1	10 ohm	173	VCOM	
34	GM1	200 ohm	104	VSSA		174	PADA2	Open
35	GM0	200 ohm	105	VSSA		175	PADB2	Open
36	LCM0	200 ohm	106	VSSA		176	TEST/Dummy	Open
37	VDDIO	200 ohm	107	VSSA		177	TEST/Dummy	Open
38	LCM1	Open	108	VSSA		178	TEST/Dummy	Open
39	VSS	Open	109	VSSA	10 ohm	179	TEST/Dummy	Open
40	DB17	100 ohm	110	VDD		180	PADB4	Open
41	DB16	100 ohm	111	VDD		181	DUMMY	Open
42	DB15	100 ohm	112	VDD		182	PADA4	Open
43	DB14	100 ohm	113	VDD		183	DUMMY	Open
44	DB13	100 ohm	114	VDD	5 ohm	184	DUMMY	Open
45	DB12	100 ohm	115	VREF		185		
46	DB11	100 ohm	116	VREF		186		
47	DB10	100 ohm	117	VREF	10 ohm	187		
48	DB9	100 ohm	118	TEST	Open	188		
49	DB8	100 ohm	119	TESTCLK	Open	189		
50	VSS	Open	120	VDDA		190		
51	TESEL	100 ohm	121	VDDA		191		
52	DB7	100 ohm	122	VDDA		192		
53	DB6	100 ohm	123	VDDA	20 ohm	193		
54	DB5	100 ohm	124	VDDA		194		
55	DB4	100 ohm	125	GVDD		195		
56	DB3	100 ohm	126	GVDD		196		
57	DB2	100 ohm	127	GVDD	20 ohm	197		
58	DB1	100 ohm	128	C11P		198		
59	DB0	100 ohm	129	C11P	5 ohm	199		
60	TEST/Dummy	Open	130	C11P		200		
61	TRIM1	Open	131	C11N		201		
62	TRIM2	Open	132	C11N		202		
63	TRIM3	Open	133	C11N	5 ohm	203		
64	TRIM4	Open	134	C12P		204		
65	OSC	200 ohm	135	C12P		205		
66	TE	100 ohm	136	C12P	5 ohm	206		
67	CSX	100 ohm	137	C12N		207		
68	RDX	100 ohm	138	C12N		208		
69	WRX	100 ohm	139	C12N	5 ohm	209		
70	SDA	100 ohm	140	VSSA	10 ohm	210		

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11. REVISION HISTORY

Date	Revision #	Description	Page
APR. 26, 2007	0.6	Modify Chip Size	212
APR. 04, 2007	0.5	1. Modify the operation voltage range of VDD and VDDIO VDD1 → 1.6V~3.6V VDD → 2.6V~3.6V 2. Modify "VCI" → "VDD" 3. Modify "VDD1" → "VDDIO"	31,33 40,42 197 6 147-155 207-211
JAN. 09, 2007	0.4	1. Add PAD Dimension 2. Add Bump Dimension 3. Add Bump Characteristics	212 213 213
NOV. 15, 2006	0.3	Change Title From 9.PAD Location to 9. CHIP INFORMATION	214
NOV. 13, 2006	0.2	Add Ordering Information	6
JUN. 22, 2006	0.1	Original	221

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